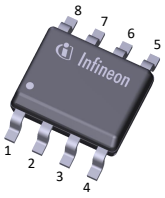
MOSFET

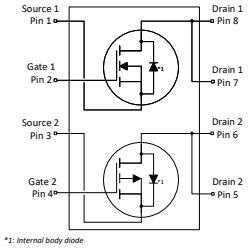
PG-DSO-8

OptiMOS™ 3 Power-Transistors, 30 V



Features

- Complementary N- and P-channel
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS\ (n\text{-}channel)}$	30	V
$R_{DS(on),max\ (n\text{-}channel)}$	15	mΩ
$I_{D\ (n\text{-}channel)}$	10.2	A
$V_{DS\ (p\text{-}channel)}$	-30	V
$R_{DS(on),max\ (p\text{-}channel)}$	23.3	mΩ
$I_{D\ (p\text{-}channel)}$	-8.8	A

Hal Pb RoHS

Type/Ordering Code	Package	Marking	Related Links
ISA150233C03LMDS	PG-DSO-8	1523C03L	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	10.2 6.5 5.8 7.6	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=90 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	41	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	28	mJ	I_D=10.2 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	2.5 1.4	W	T_C=25 °C T_A=25 °C, R_{thJA}=90 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2 for n-channel. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

Table 3 Maximum ratings (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [5]	I_D	-	-	-8.8 -5.6 -5.1 -6.6	A	V_{GS}=-10 V, T_C=25 °C V_{GS}=-10 V, T_C=100 °C V_{GS}=-4.5 V, T_C=100 °C V_{GS}=-10 V, T_A=25 °C, R_{THJA}=90 °C/W [6]
Pulsed drain current [7]	$I_{D,pulse}$	-	-	-35	A	T_C=25 °C
Avalanche energy, single pulse [8]	E_{AS}	-	-	28	mJ	I_D=-8.8 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-	-	±20	V	-
Power dissipation	P_{tot}	-	-	2.5 1.4	W	T_C=25 °C T_A=25 °C, R_{thJA}=90 °C/W [6]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

[5] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 17 for p-channel. De-rating will be required based on the actual environmental conditions.

[6] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

7) See Diagram 18 for more detailed information

8) See Diagram 28 for more detailed information

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	R_{thJC}	-	-	50	°C/W	-
Thermal resistance, junction - ambient, minimal footprint, steady state	R_{thJA}	-	-	150	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area, steady state [9)]	R_{thJA}	-	-	90	°C/W	-

[9)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 5 Static characteristics (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	-	2.7	V	V_{DS}=V_{GS}, I_D=1000 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	12 14	15.0 18.7	mΩ	V_{GS}=10 V, I_D=10.2 A V_{GS}=4.5 V, I_D=9 A
Gate resistance	R_G	-	1.1	-	Ω	-
Transconductance [10)]	g_{fs}	13	27	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=10.2 A

10) Defined by design. Not subject to production test.

Table 6 Static characteristics (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-30	-	-	V	V_{GS}=0 V, I_D=-1 mA
Gate threshold voltage	$V_{GS(th)}$	-1.1	-	-2.7	V	V_{DS}=V_{GS}, I_D=-1000 µA
Zero gate voltage drain current	I_{DSS}	-	-0.1 -10	-1 -100	µA	V_{DS}=-30 V, V_{GS}=0 V, T_j=25 °C V_{DS}=-30 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	V_{GS}=-20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	18 23	23.3 27.7	mΩ	V_{GS}=-10 V, I_D=-8.8 A V_{GS}=-4.5 V, I_D=-8.2 A
Gate resistance	R_G	-	3.0	-	Ω	-
Transconductance [11)]	g_{fs}	10	21	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=-8.8 A

11) Defined by design. Not subject to production test.

Table 7 Dynamic characteristics (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [12)]	C_{iss}	-	1000	1300	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance [12)]	C_{oss}	-	330	430	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	28	49	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	7.6	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=10.2 A, $R_{G,ext}$=1.6 Ω

Table 7 Dynamic characteristics (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Rise time	t_r	-	3.3	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=10.2 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	7.5	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=10.2 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	4.0	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=10.2 A, $R_{G,ext}$=1.6 Ω
Gate to source charge	Q_{gs}	-	2.9	-	nC	V_{DD}=15 V, I_D=10.2 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	1.6	-	nC	V_{DD}=15 V, I_D=10.2 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	1.6	-	nC	V_{DD}=15 V, I_D=10.2 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	2.9	-	nC	V_{DD}=15 V, I_D=10.2 A, V_{GS}=0 to 4.5 V
Gate charge total [12)]	Q_g	-	6.7	10.1	nC	V_{DD}=15 V, I_D=10.2 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.9	-	V	V_{DD}=15 V, I_D=10.2 A, V_{GS}=0 to 4.5 V
Gate charge total [12)]	Q_g	-	14	19	nC	V_{DD}=15 V, I_D=10.2 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	7.4	-	nC	V_{DS}=15 V, V_{GS}=0 V

[12)] Defined by design. Not subject to production test.

Table 8 Dynamic characteristics (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [13)]	C_{iss}	-	1800	2300	pF	V_{GS}=0 V, V_{DS}=-15 V, f=1 MHz
Output capacitance [13)]	C_{oss}	-	790	1000	pF	V_{GS}=0 V, V_{DS}=-15 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	55	96	pF	V_{GS}=0 V, V_{DS}=-15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	V_{DD}=-15 V, V_{GS}=-4.5 V, I_D=-8.8 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	8.5	-	ns	V_{DD}=-15 V, V_{GS}=-4.5 V, I_D=-8.8 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	13	-	ns	V_{DD}=-15 V, V_{GS}=-4.5 V, I_D=-8.8 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	6.7	-	ns	V_{DD}=-15 V, V_{GS}=-4.5 V, I_D=-8.8 A, $R_{G,ext}$=1.6 Ω
Gate to source charge	Q_{gs}	-	-5.1	-	nC	V_{DD}=-15 V, I_D=-8.8 A, V_{GS}=0 to -4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	-2.9	-	nC	V_{DD}=-15 V, I_D=-8.8 A, V_{GS}=0 to -4.5 V
Gate to drain charge	Q_{gd}	-	-2.9	-	nC	V_{DD}=-15 V, I_D=-8.8 A, V_{GS}=0 to -4.5 V
Switching charge	Q_{sw}	-	-5.2	-	nC	V_{DD}=-15 V, I_D=-8.8 A, V_{GS}=0 to -4.5 V
Gate charge total [13)]	Q_g	-	-12	-18	nC	V_{DD}=-15 V, I_D=-8.8 A, V_{GS}=0 to -4.5 V

Table 8 Dynamic characteristics (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate plateau voltage	$V_{plateau}$	-	-2.9	-	V	V_{DD}=-15 V, I_D=-8.8 A, V_{GS}=0 to -4.5 V
Gate charge total [13)]	Q_g	-	-24	-32	nC	V_{DD}=-15 V, I_D=-8.8 A, V_{GS}=0 to -10 V
Output charge	Q_{oss}	-	-17	-	nC	V_{DS}=-15 V, V_{GS}=0 V

13) Defined by design. Not subject to production test.

Table 9 Reverse diode (n-channel)

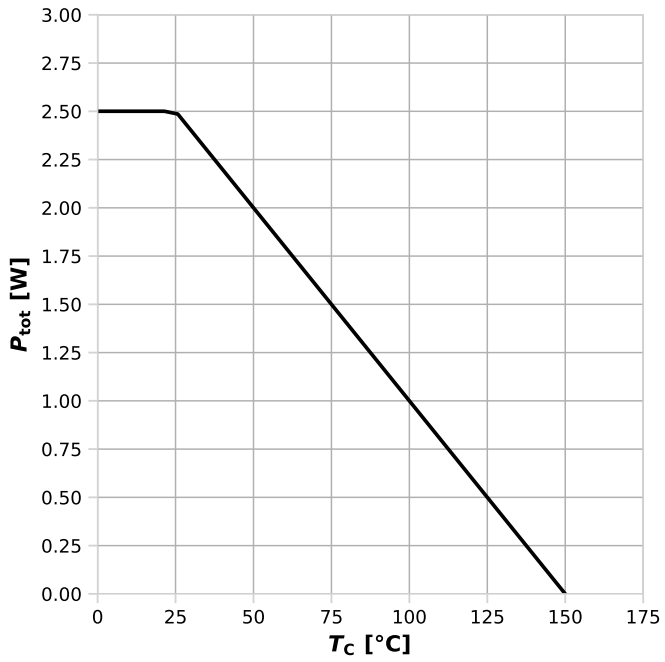
Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	3.2	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	41	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.87	1.0	V	V_{GS}=0 V, I_F=10.2 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	15	-	ns	V_R=15 V, I_F=10.2 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	5.4	-	nC	V_R=15 V, I_F=10.2 A, di_F/dt=100 A/µs

Table 10 Reverse diode (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-3.3	A	T_A=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	-35	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	-0.89	-1.0	V	V_{GS}=0 V, I_F=-8.8 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	22	-	ns	V_R=-15 V, I_F=-8.8 A, di_F/dt=-100 A/µs
Reverse recovery charge	Q_{rr}	-	11	-	nC	V_R=-15 V, I_F=-8.8 A, di_F/dt=-100 A/µs

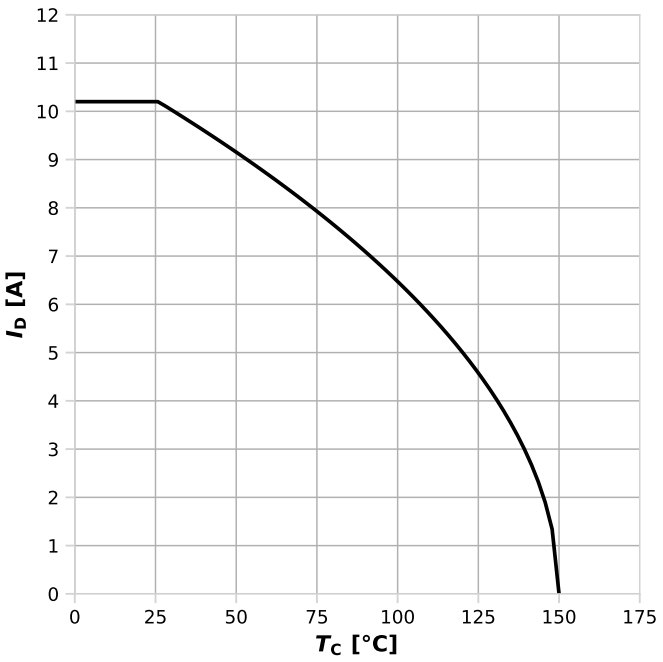
4 Electrical characteristics diagrams

Diagram 1: Power dissipation (n-channel)



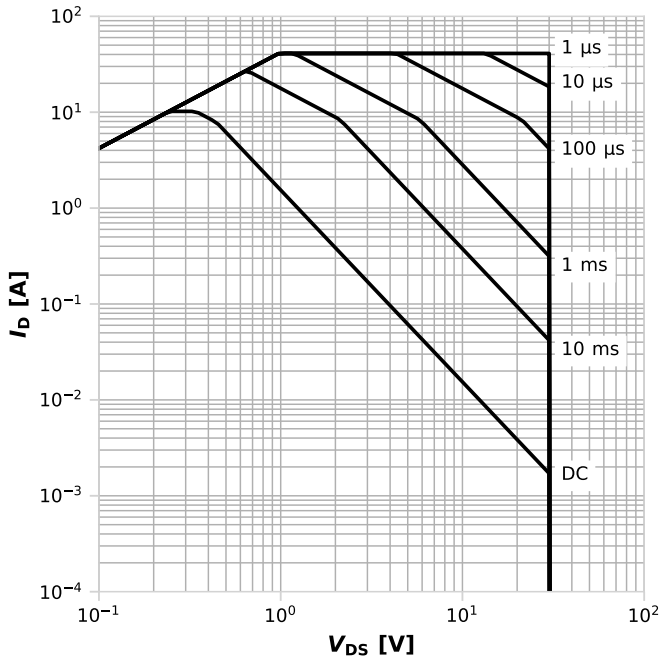
P_{tot}=f(T_C)

Diagram 2: Drain current (n-channel)



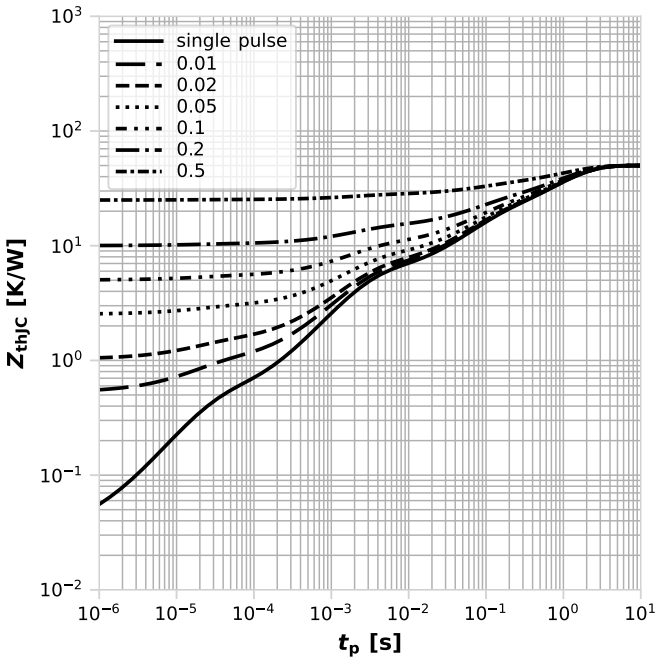
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area (n-channel)



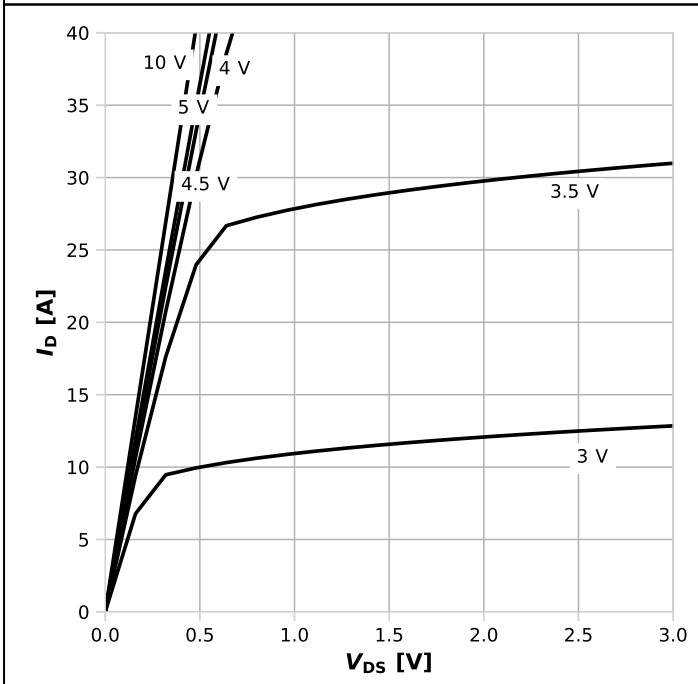
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance (n-channel)



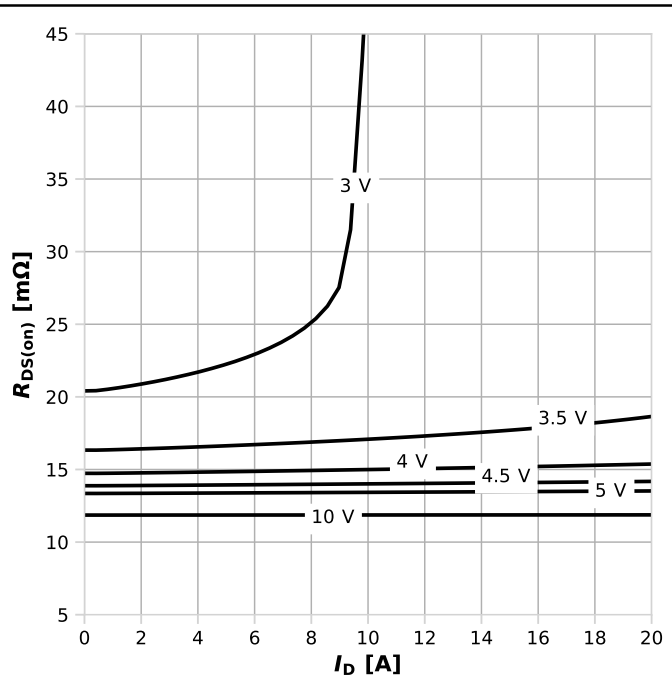
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics (n-channel)



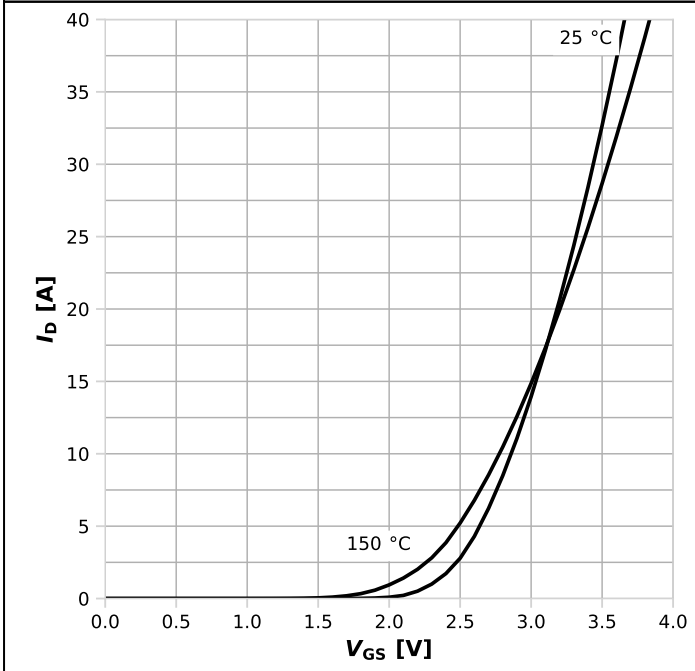
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance (n-channel)



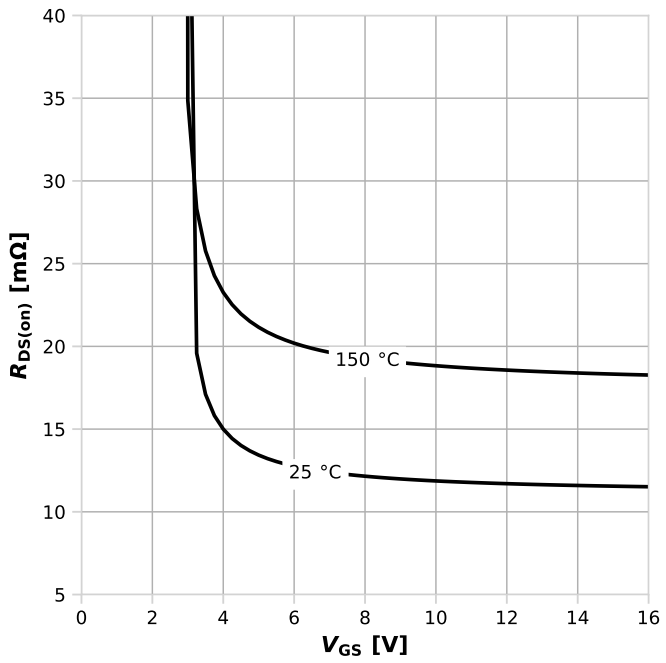
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics (n-channel)



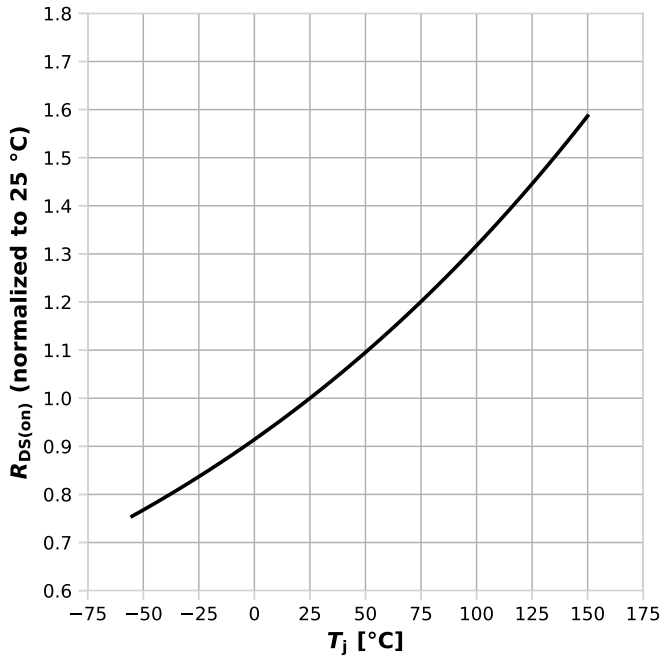
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance (n-channel)



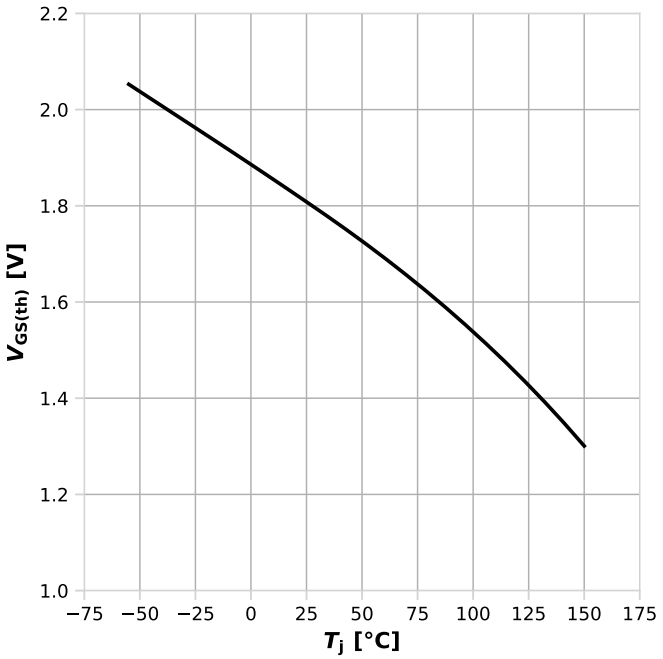
$R_{DS(on)}$=f(V_{GS}), I_D=10.2 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance (n-channel)



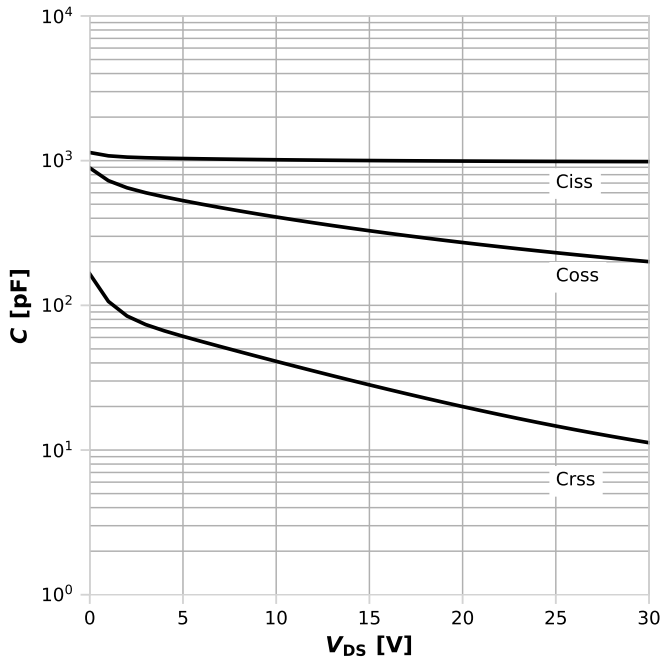
$R_{DS(on)}$=f(T_j), I_D=10.2 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage (n-channel)



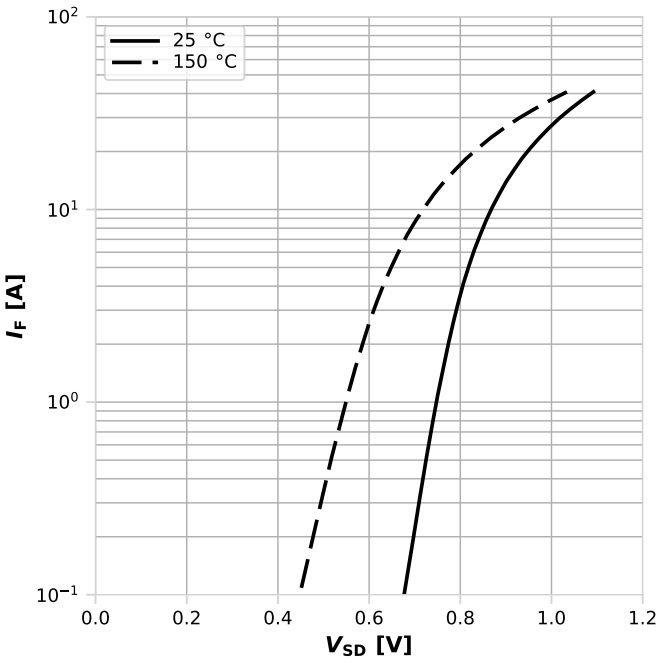
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances (n-channel)



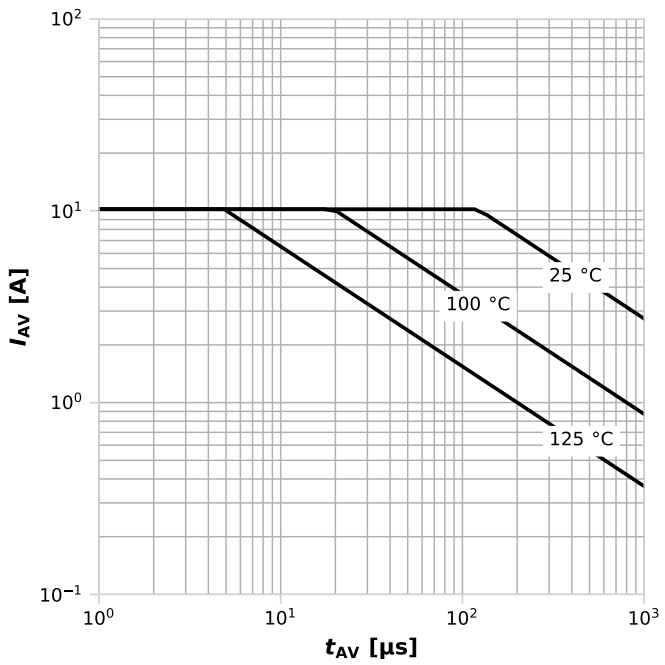
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode (n-ch.)



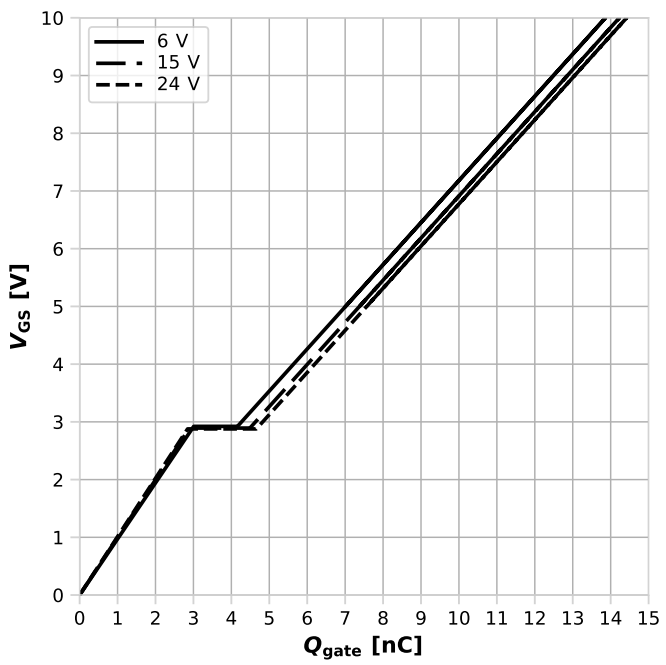
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics (n-channel)



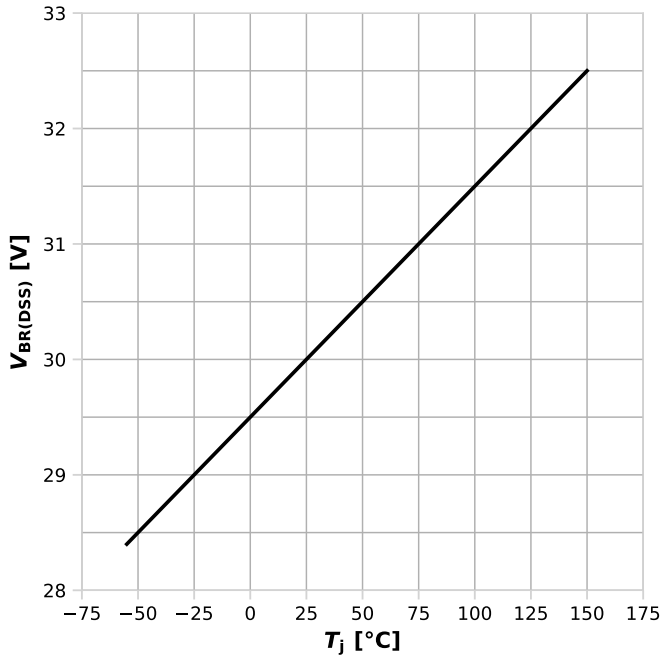
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge (n-channel)



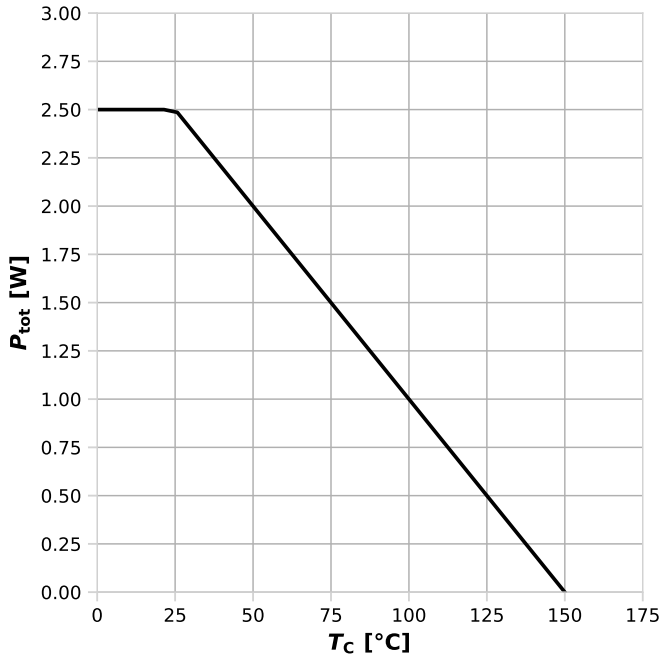
V_{GS}=f(Q_{gate}), I_D=10.2 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage (n-channel)



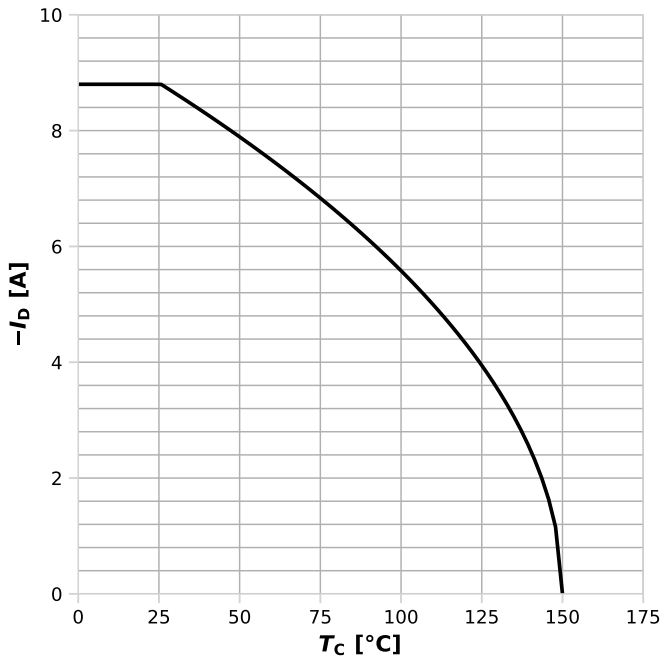
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 16: Power dissipation (p-channel)



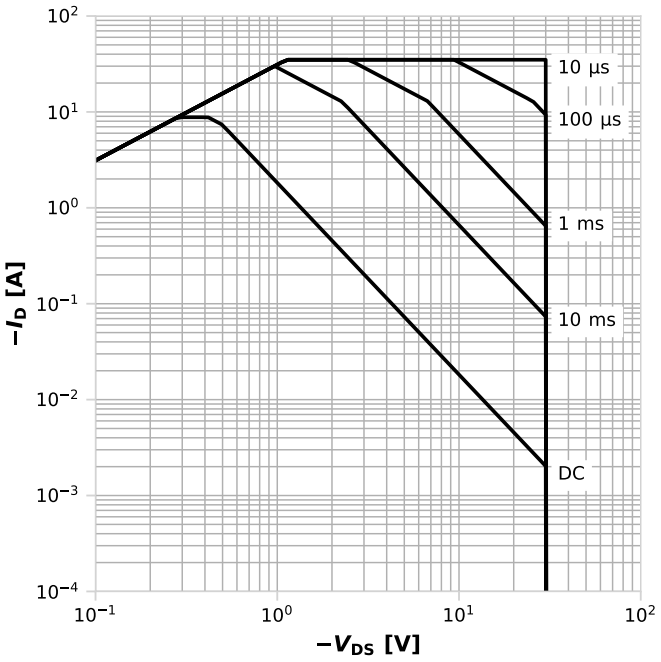
P_{tot}=f(T_C)

Diagram 17: Drain current (p-channel)



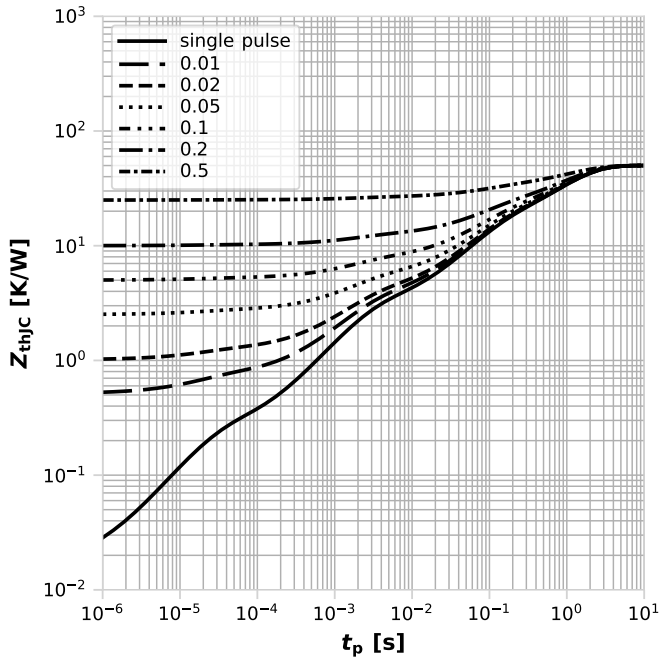
I_D=f(T_C); $|V_{GS}|$≥10 V

Diagram 18: Safe operating area (p-channel)



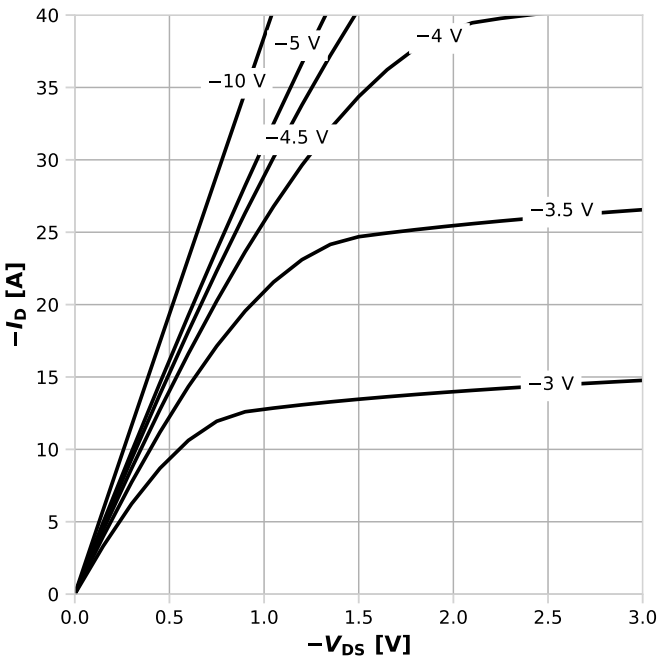
I_D=f(V_{DS}); T_C=125 °C; D=0; parameter: t_p

Diagram 19: Max. transient thermal impedance (p-channel)



Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 20: Typ. output characteristics (p-channel)



I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

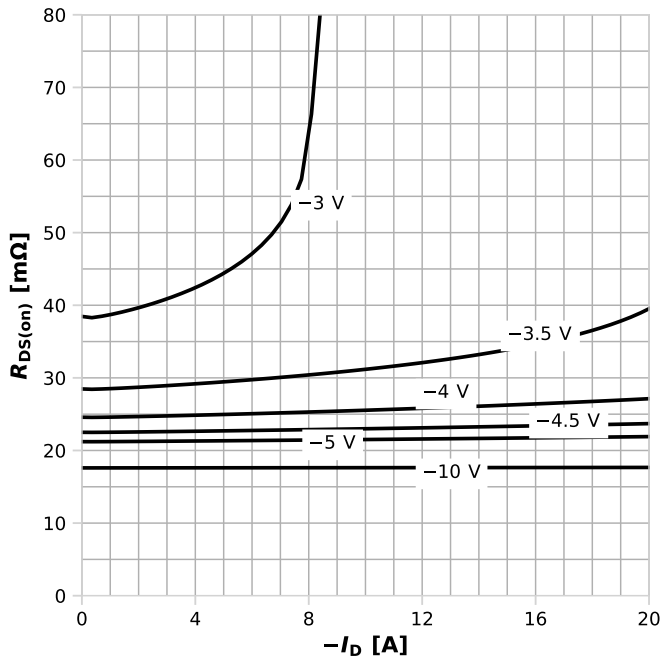
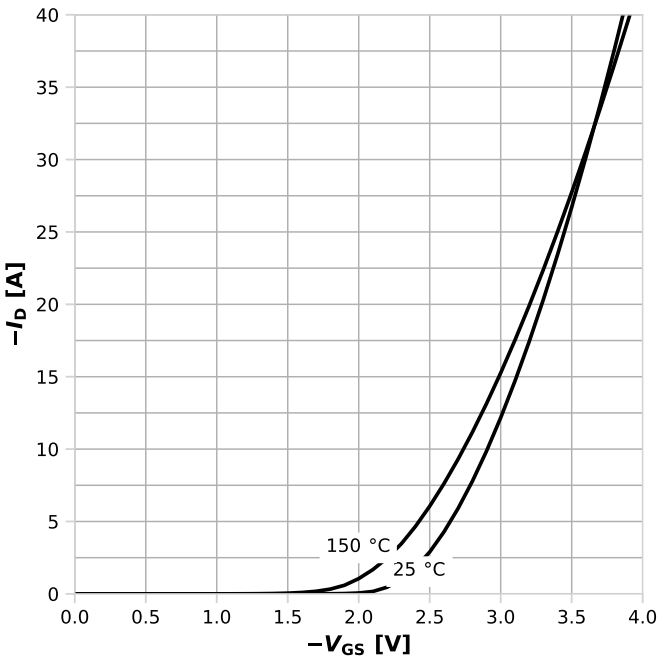
Diagram 21: Typ. drain-source on resistance (p-channel)	Diagram 22: Typ. transfer characteristics (p-channel)
	
$R_{DS(on)}$=f(I_D), T_j=175 °C; parameter: V_{GS}	I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

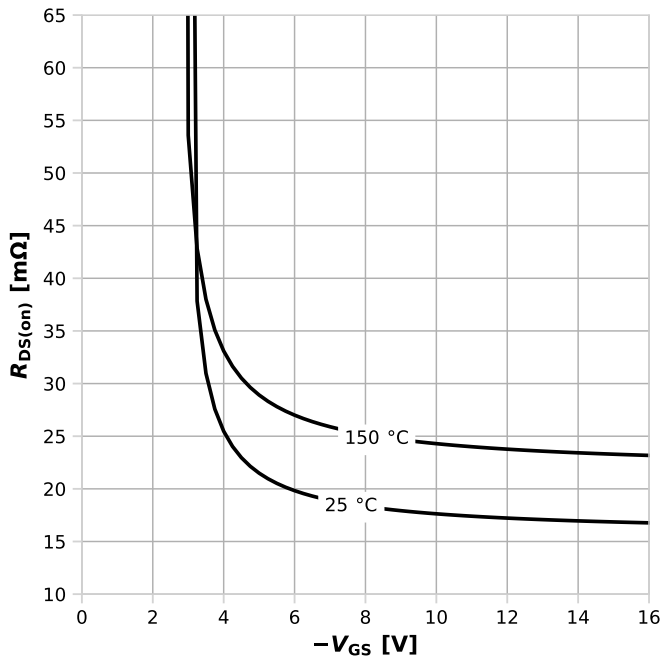
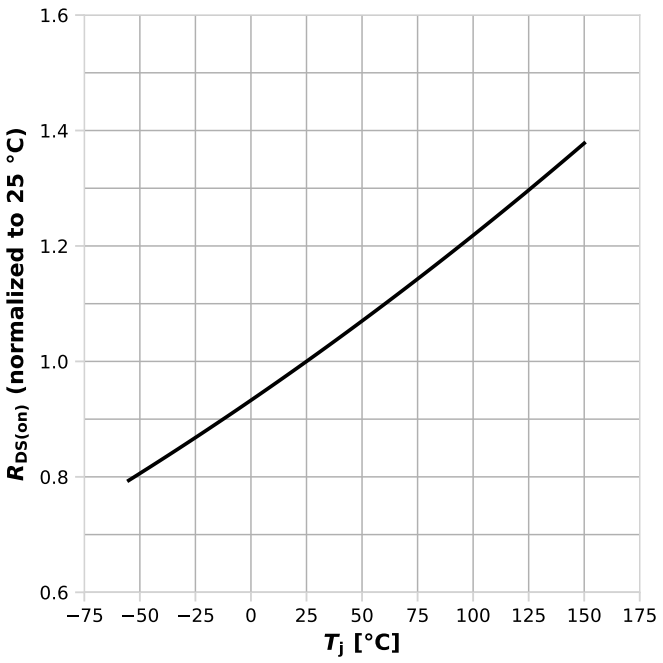
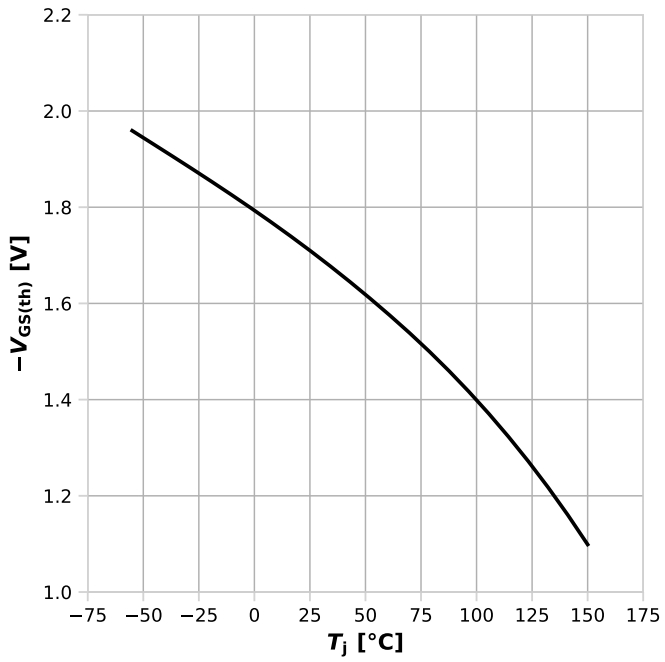
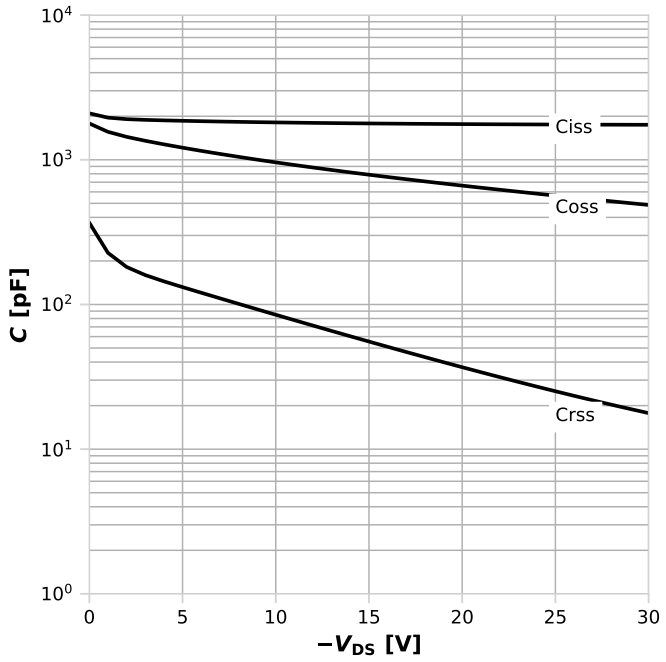
Diagram 23: Typ. drain-source on resistance (p-channel)	Diagram 24: Normalized drain-source on resistance (p-ch.)
	
$R_{DS(on)}$=f(V_{GS}), I_D=-8.8 A; parameter: T_j	$R_{DS(on)}$=f(T_j), I_D=-8.8 A, V_{GS}=-10 V

Diagram 25: Typ. gate threshold voltage (p-channel)



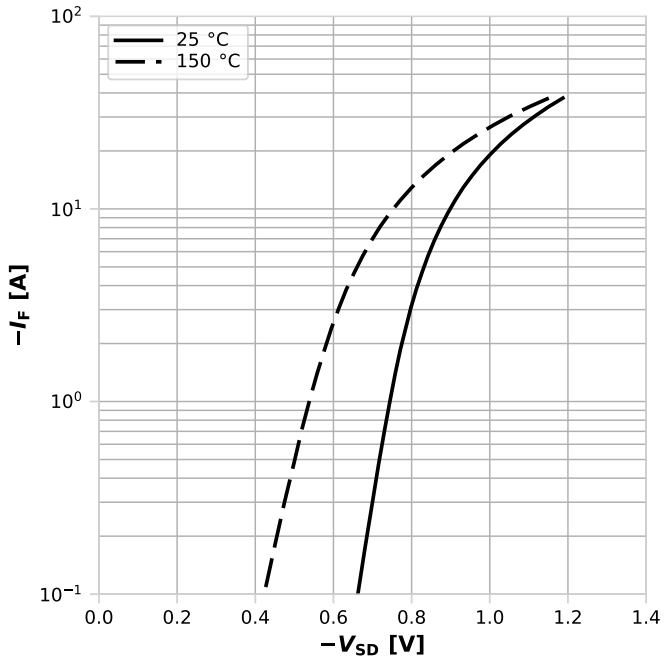
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; I_D=1000µA

Diagram 26: Typ. capacitances (p-channel)



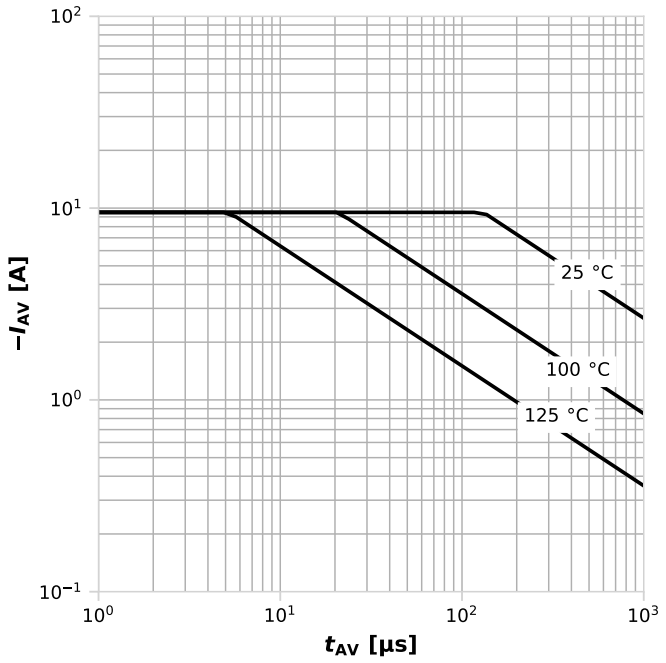
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 27: Forward characteristics of reverse diode (p-ch.)

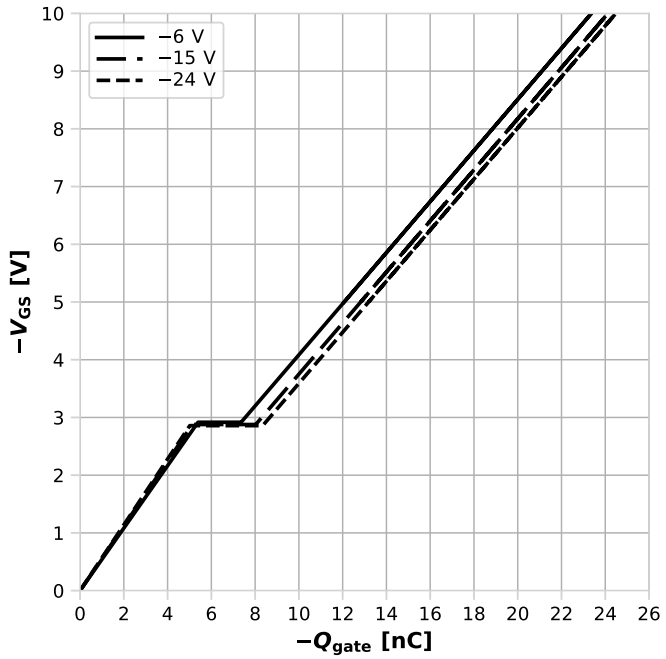
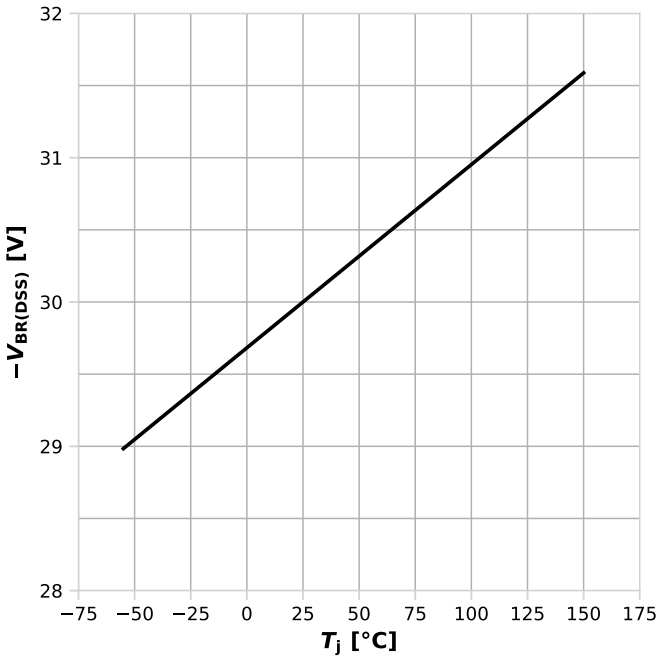


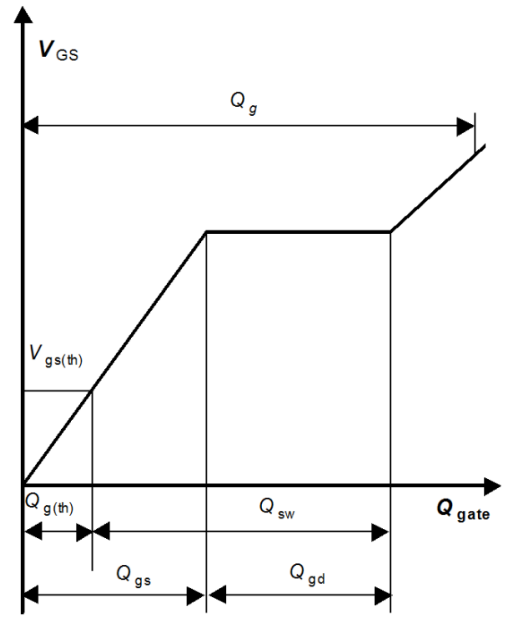
I_F=f(V_{SD}); parameter: T_j

Diagram 28: Avalanche characteristics (p-channel)

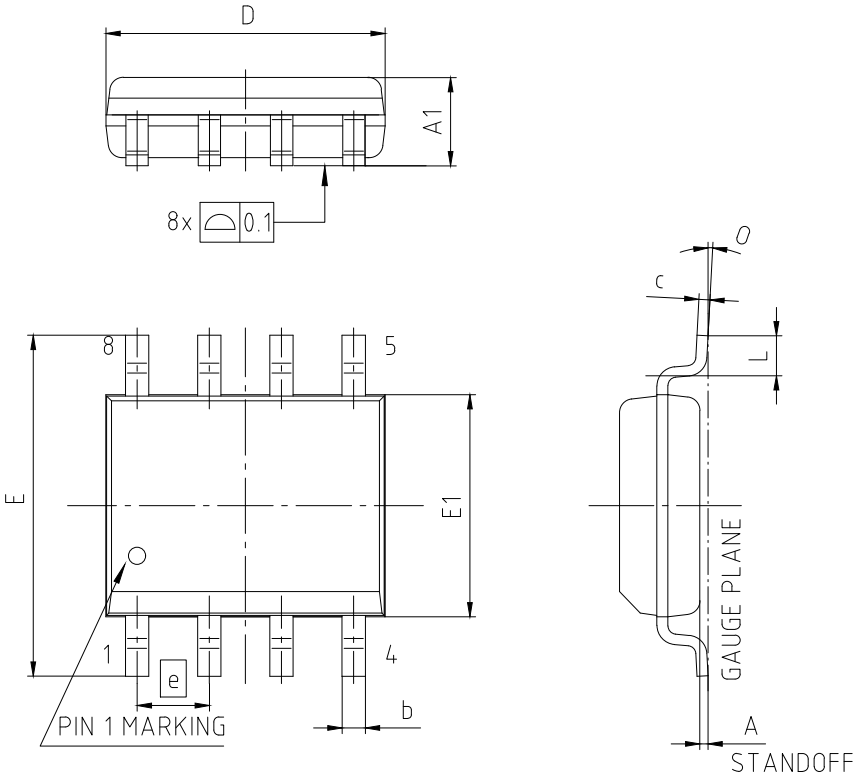


I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 29: Typ. gate charge (p-channel)	Diagram 30: Drain-source breakdown voltage (p-channel)
	
V_{GS}=f(Q_{gate}), I_D=-8.8 A pulsed, T_j=25 °C; parameter: V_{DD}	$V_{BR(DSS)}$=f(T_j); I_D=-1 mA

Gate charge waveforms

-

5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-DSO-8-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.18	0.25
A1	1.35	1.75
b	0.38	0.51
c	0.254	
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27	
L	0.48	0.91
O	4°	
N	8	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-DSO-8, dimensions in mm

Revision History

ISA150233C03LMDS

Revision 2024-10-04, Rev. 1.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-10-04	Release of final

We Listen to Your Comments Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: **erratum@infineon.com**

Published by
Infineon Technologies AG
81726 München, Germany