



# PSMNR70-40YSN

N-channel 40 V, 0.81 mOhm, ASFET for Battery System in LFPAK56E

12 September 2024

Product data sheet

## 1. General description

ASFET for Battery System applications, characterized by low  $R_{DSon}$  and strong SOA capability for reduced I<sup>2</sup>R conduction losses. ASFETs deliver high efficiency, reduced heat generation and superior handling of inrush current during transient and fault conditions.

## 2. Features and benefits

- 360 A continuous  $I_{D(max)}$
- Strong SOA capability
- Avalanche rated, 100% tested at  $I_{AS} = 190$  A
- High reliability LFPAK (Power-SO8) package, qualified to 175 °C
- LFPAK copper clip
- LFPAK gull wing lead

## 3. Applications

- Battery management systems (BMS)
- eFuse
- Load-switch
- BLDC motor control
- High-performance power supply
- High-performance synchronous rectification

## 4. Quick reference data

Table 1. Quick reference data

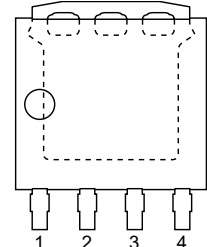
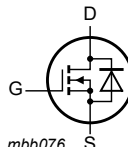
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	-	360	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	-	333	W
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>		0.5	0.72	0.81	mΩ
<b>Dynamic characteristics</b>							
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		14	46	79	nC
<b>Source-drain diode</b>							
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 18</a>	[2]	-	34	-	nC

[1] 360A Continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] includes capacitive recovery

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR70-40YSN	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56E); 4 leads; 1.27 mm pitch	SOT1023

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR70-40YSN	N70S40J

## 8. Limiting values

Table 5. Limiting values

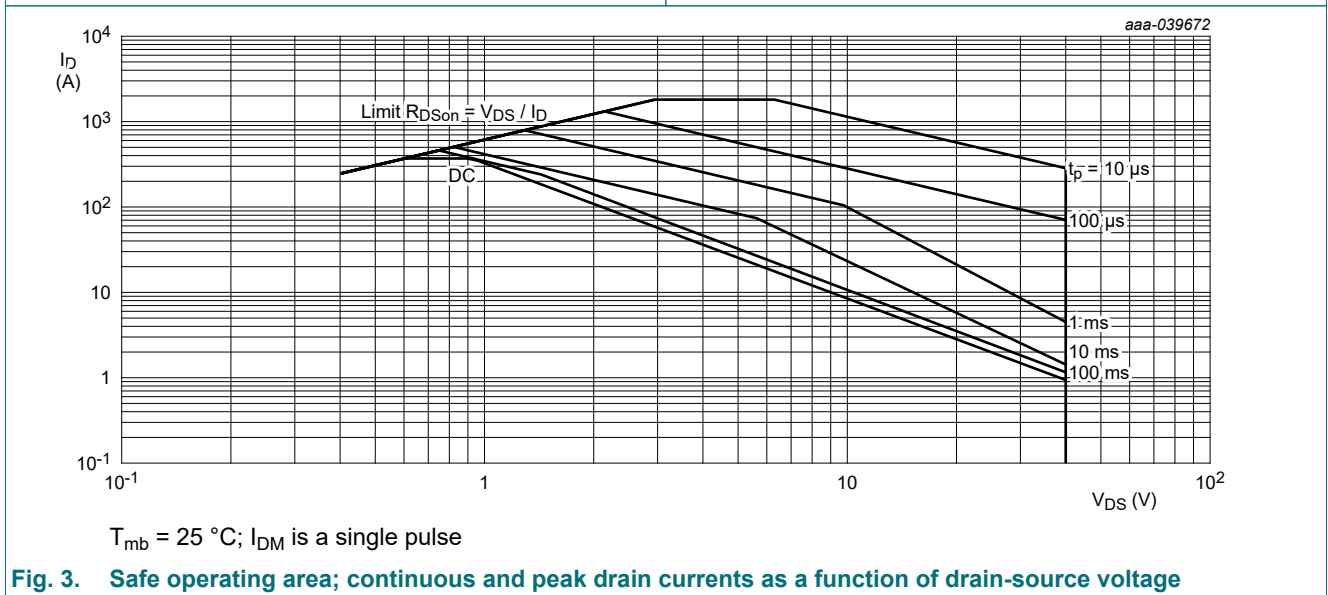
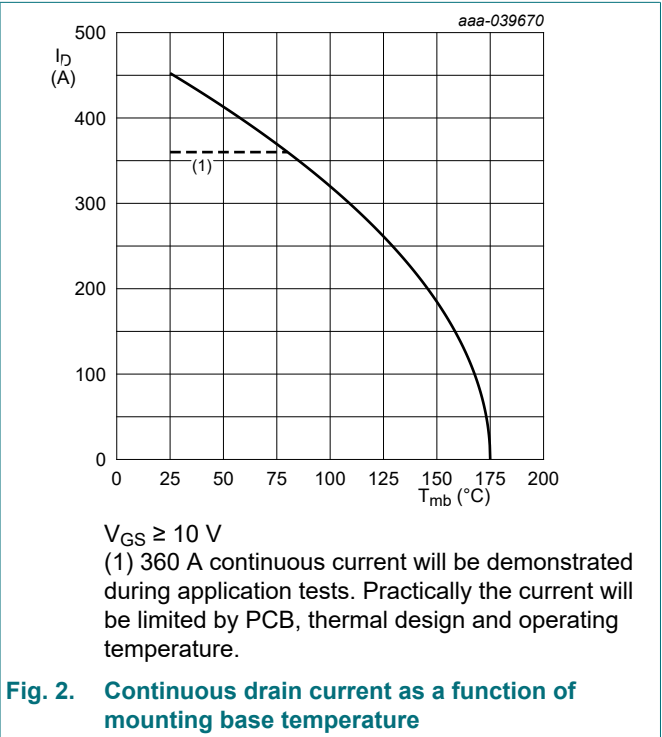
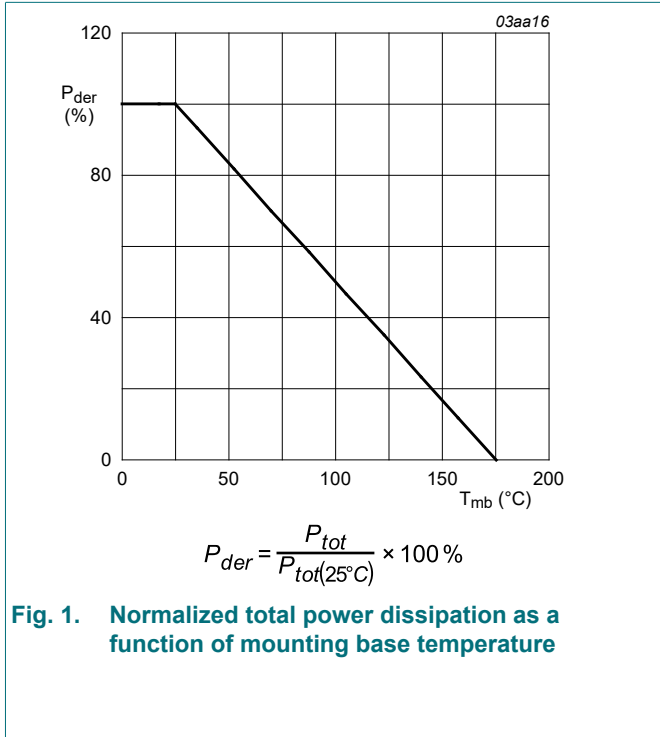
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ °C}$  unless otherwise stated.

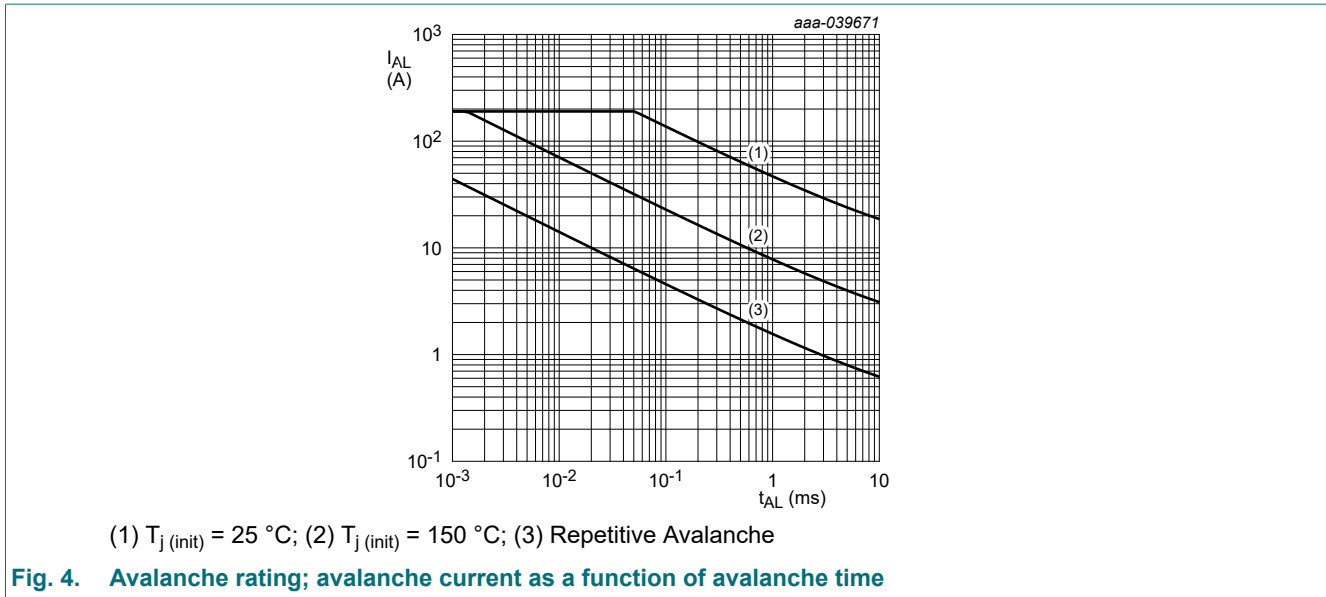
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V
$V_{DSM}$	peak drain-source voltage	$t_p \leq 20\text{ ns}$ ; $f \leq 500\text{ kHz}$ ; $E_{DS(AL)} \leq 200\text{ nJ}$ ; single pulse	-	45	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	333	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	360	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>		320	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>	-	1810	A
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	333	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	1810	A

N-channel 40 V, 0.81 mOhm, ASFET for Battery System in LPAK56E

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 80.8 \text{ A}$ ; $V_{sup} \leq 40 \text{ V}$ ; $R_{GS} = 50 \Omega$ ; $V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$ ; unclamped; $t_p = 304 \mu\text{s}$ ; Fig. 4	[2]	-	638	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 40 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$ ; $R_{GS} = 50 \Omega$ ; Fig. 4	[2]	-	190	A

- [1] 360A Continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

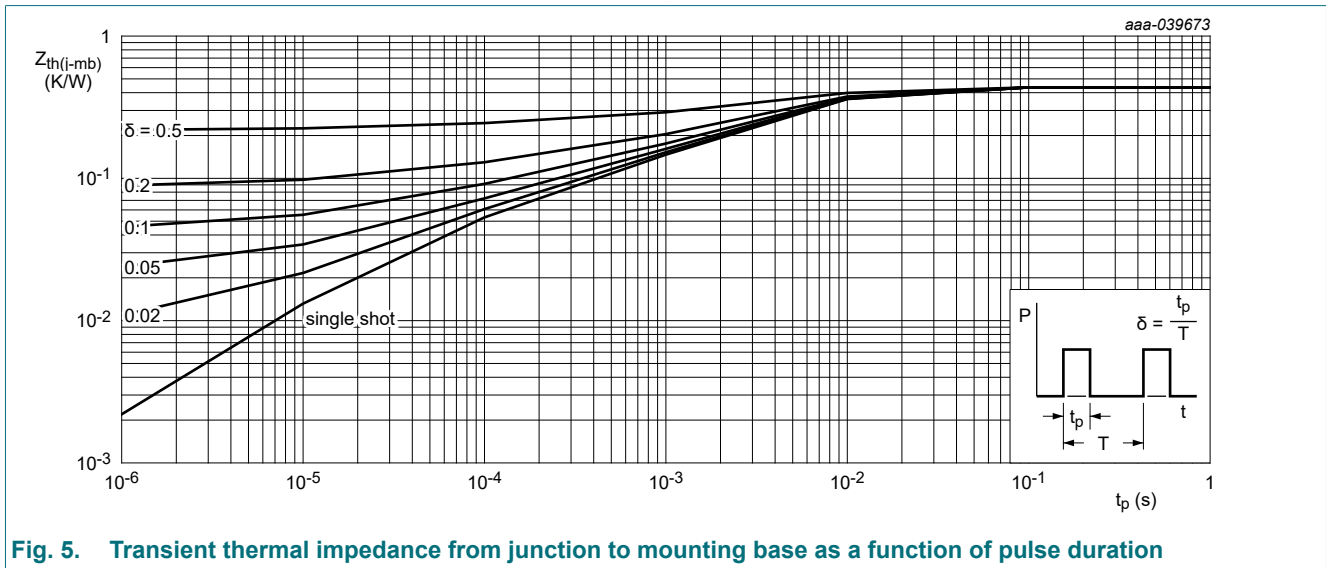


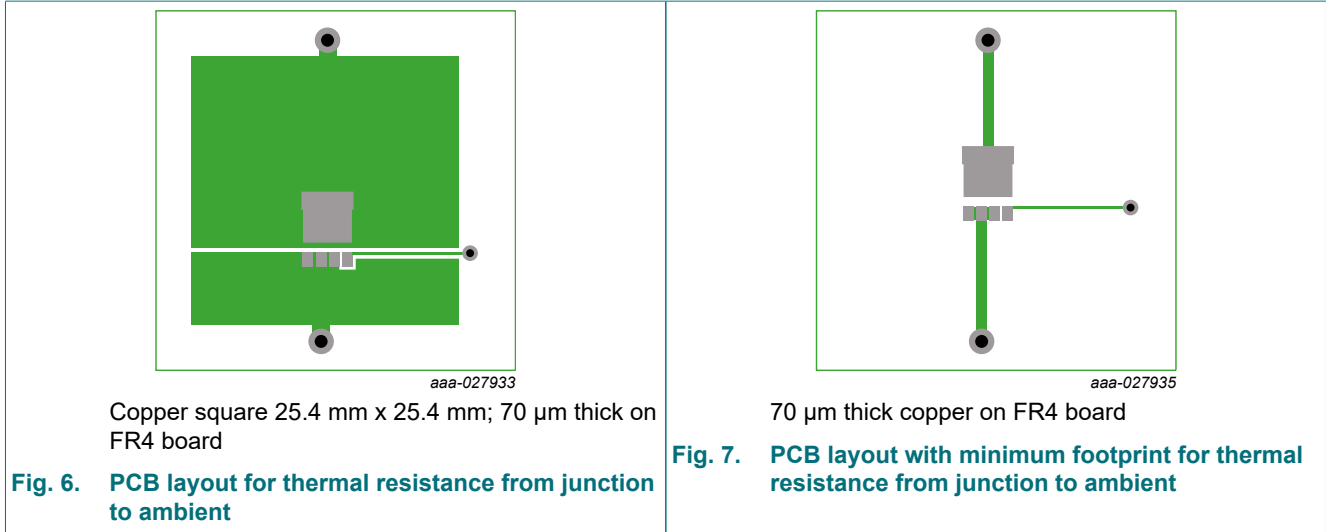


### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.4	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6 Fig. 7	-	42 85	-	K/W K/W





## 10. Characteristics

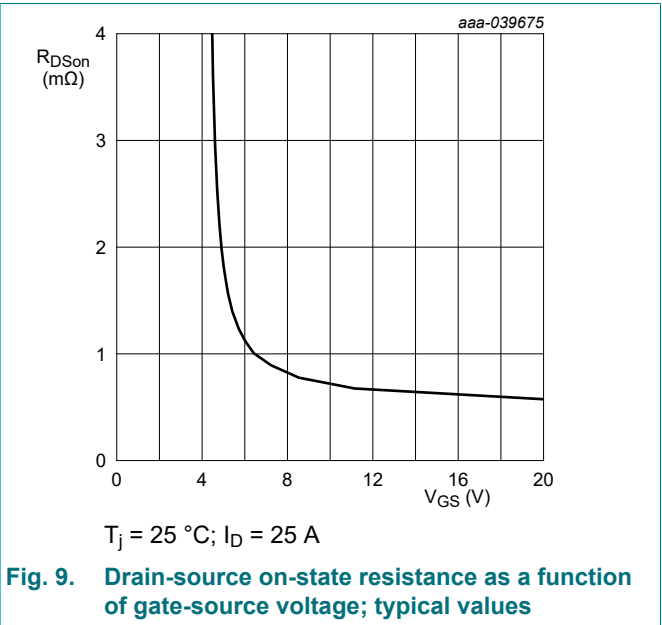
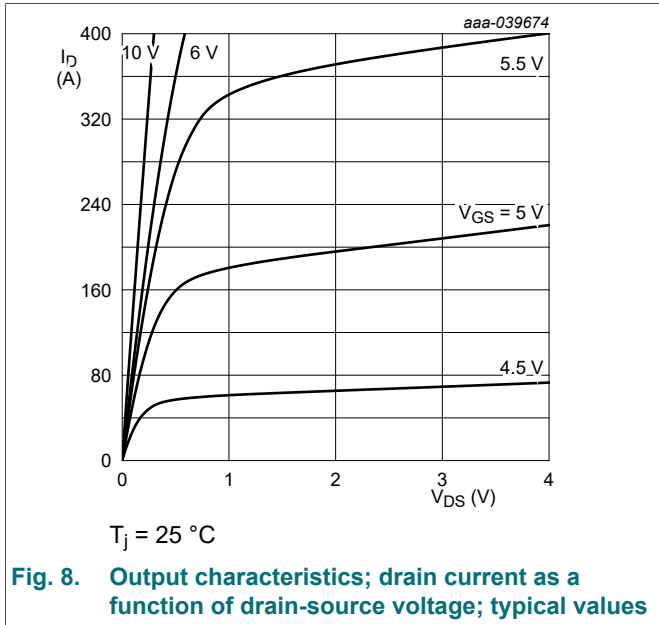
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	43	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	41	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}$	2.4	2.9	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.4	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.9	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 175 \text{ }^\circ C$	-	-7.4	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.1	1	μA
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	1.2	10	μA
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 12}$	0.5	0.72	0.81	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 105 \text{ }^\circ C; \text{ Fig. 13}$	0.69	1.02	1.22	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 125 \text{ }^\circ C; \text{ Fig. 13}$	0.74	1.12	1.33	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C; \text{ Fig. 13}$	0.88	1.36	1.67	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.3	0.78	2	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 14}; \text{ Fig. 15}$	101	168	235	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$	-	136	-	nC

N-channel 40 V, 0.81 mOhm, ASFET for Battery System in LPAK56E

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 20\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14; Fig. 15	20	37	54	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		14	25	36	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		6.6	12	17	nC
$Q_{GD}$	gate-drain charge		14	46	79	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 14; Fig. 15	-	4.3	-	V
$C_{iss}$	input capacitance	$V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 16	6152	10253	14355	pF
$C_{oss}$	output capacitance		1540	2200	2861	pF
$C_{rss}$	reverse transfer capacitance		351	877	1404	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	30	-	ns
$t_r$	rise time		-	51	-	ns
$t_{d(off)}$	turn-off delay time		-	96	-	ns
$t_f$	fall time		-	66	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	67	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.78	1	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 18	-	39	-	ns
$Q_r$	recovered charge		[1]	34	-	nC

[1] includes capacitive recovery



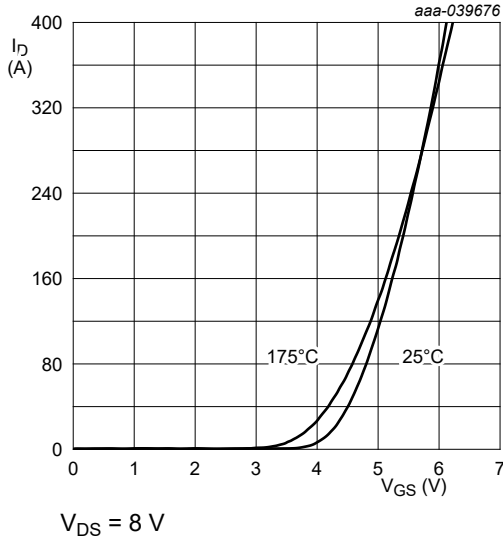


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

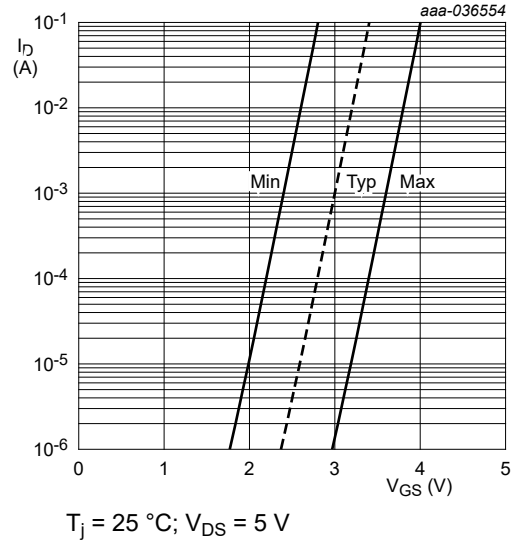


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

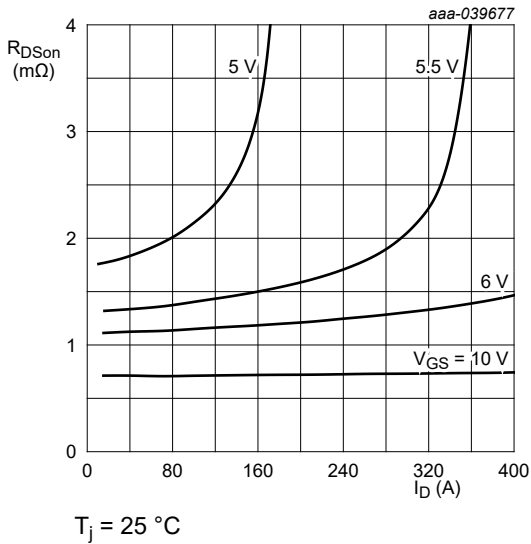


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

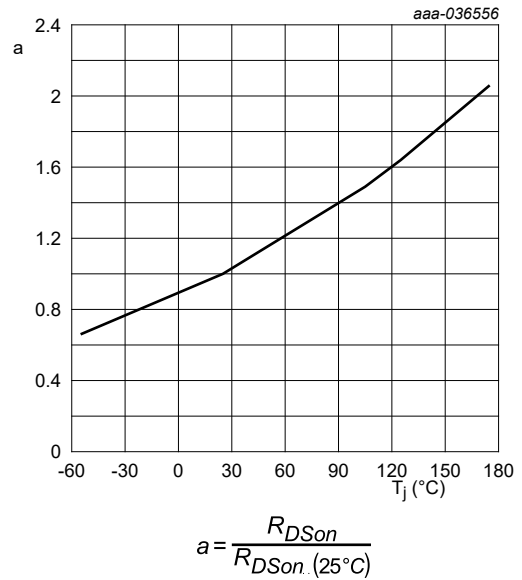


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

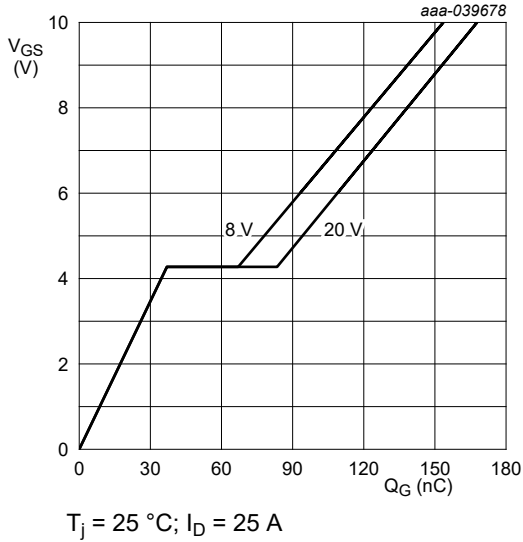


Fig. 14. Gate-source voltage as a function of gate charge; typical values

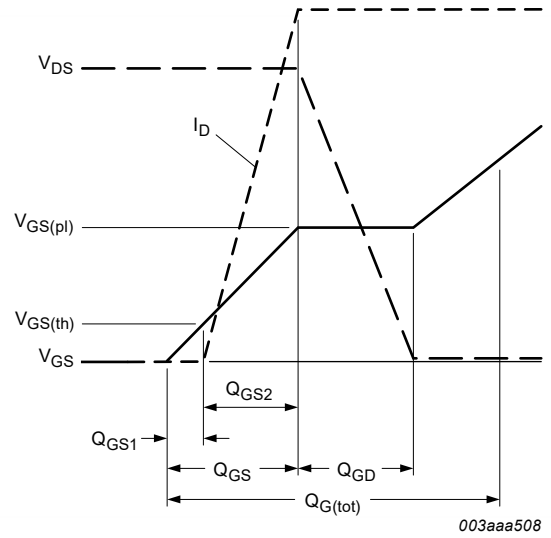


Fig. 15. Gate charge waveform definitions

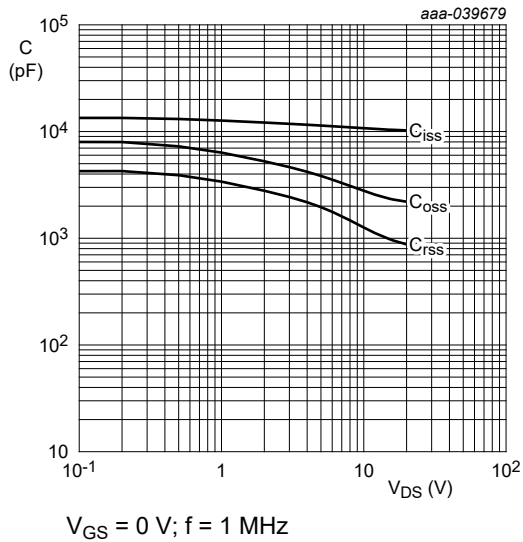


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

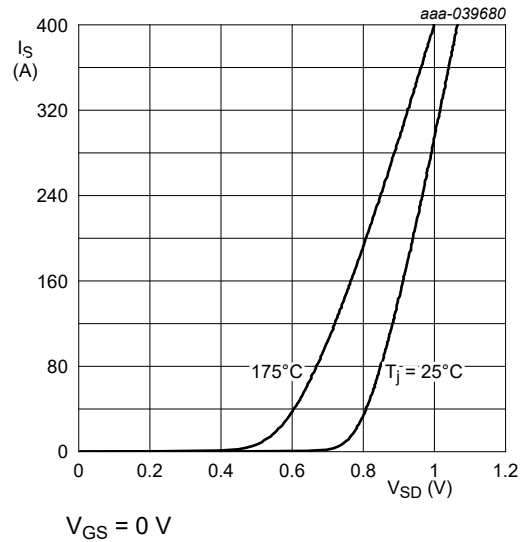


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

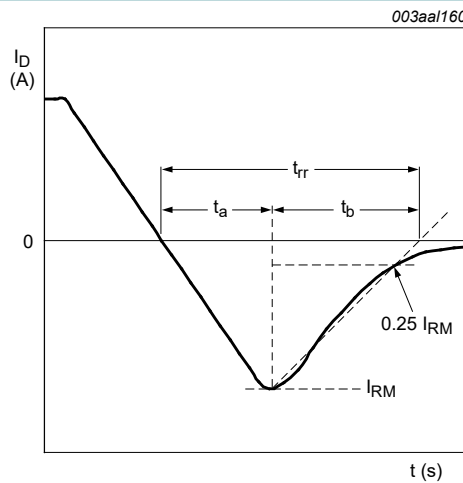


Fig. 18. Reverse recovery timing definition



### 11. Package outline

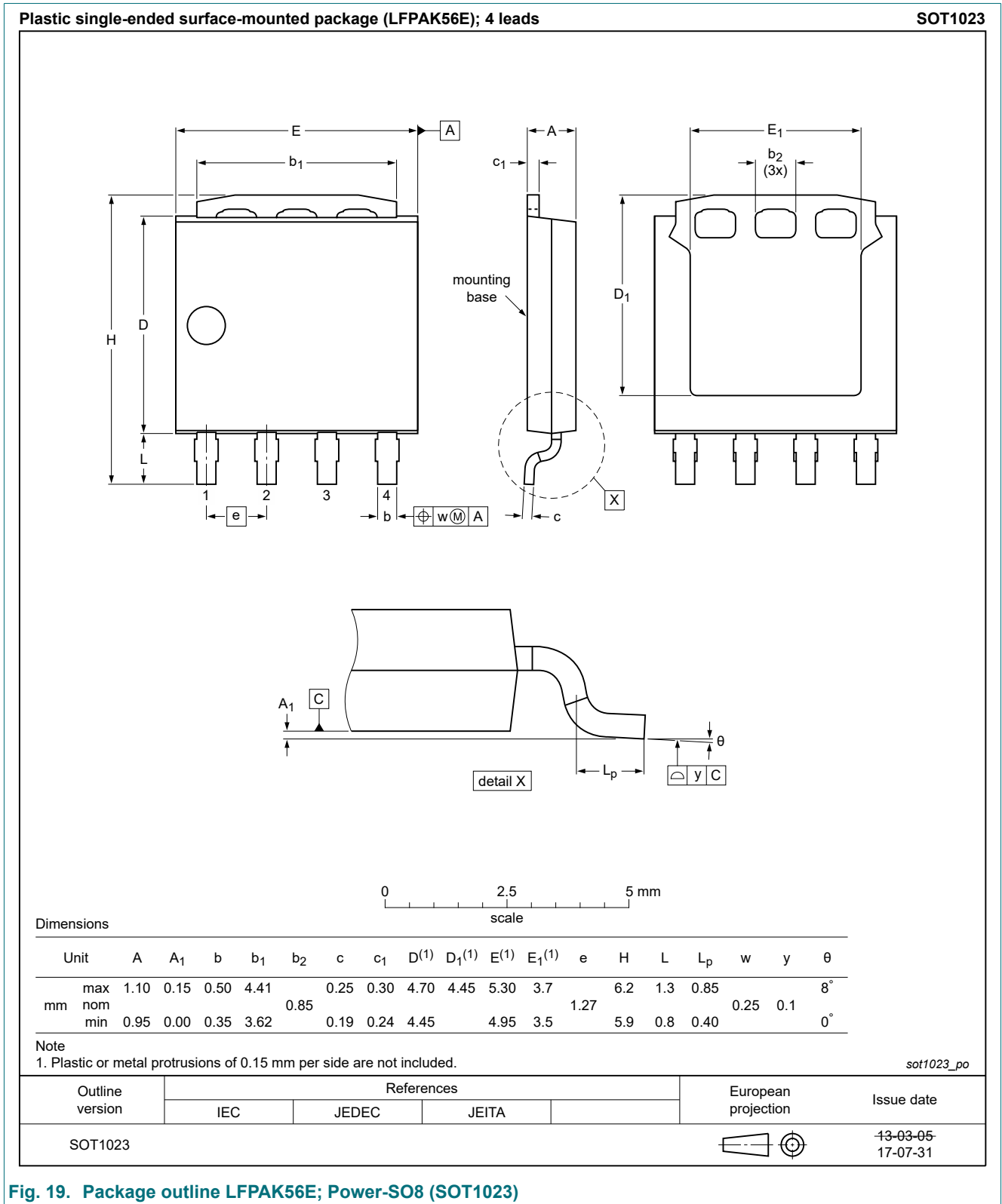
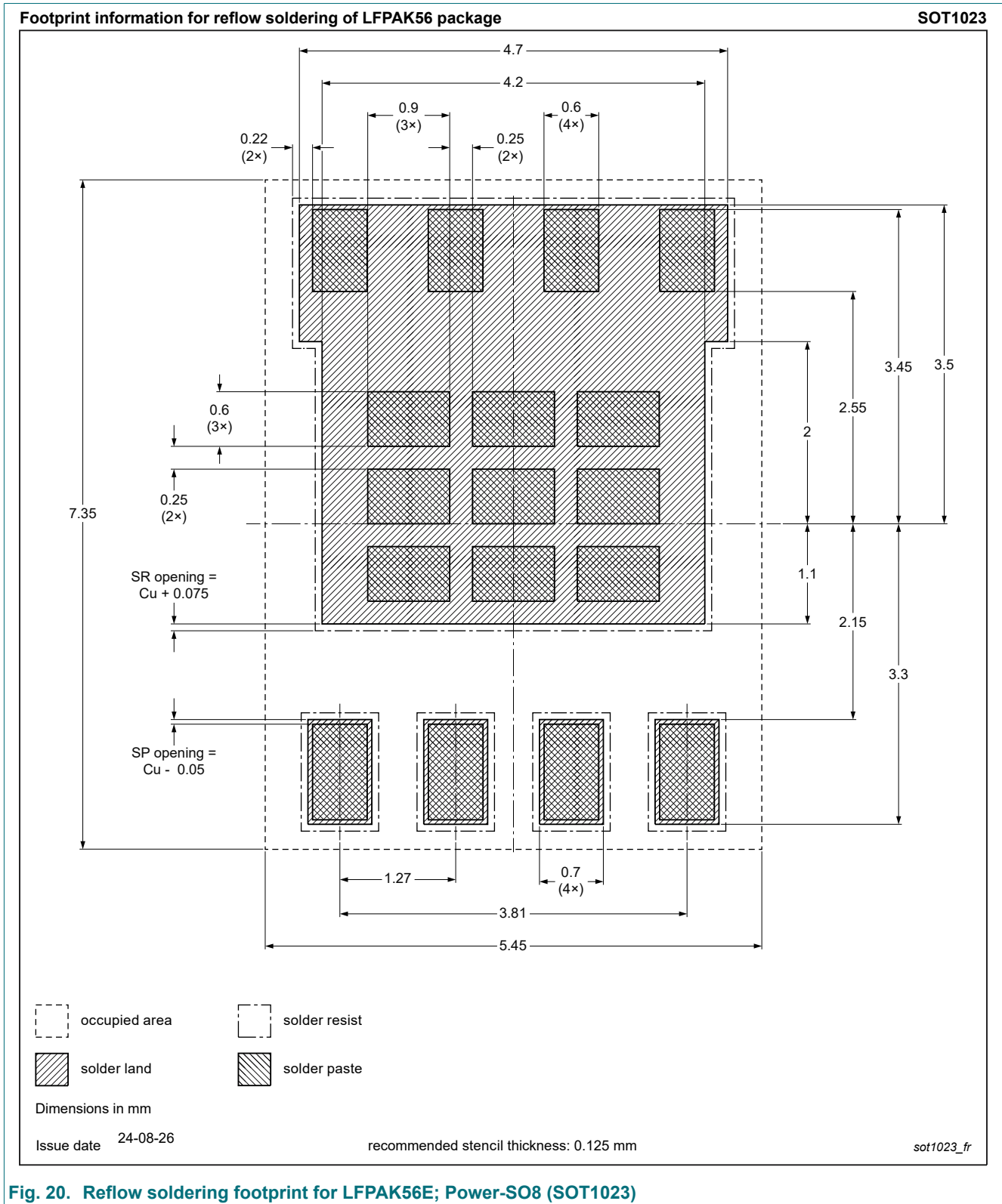


Fig. 19. Package outline LPAK56E; Power-SO8 (SOT1023)

## 12. Soldering



## 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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## Contents

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1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	2
9. Thermal characteristics.....	4
10. Characteristics.....	5
11. Package outline.....	9
12. Soldering.....	10
13. Legal information.....	11

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