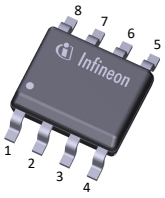
MOSFET

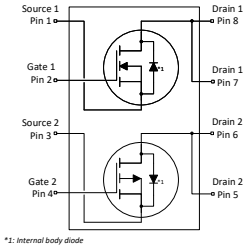
PG-DSO-8

OptiMOS™ 3 Power-Transistors, 40 V



Features

- Complementary N- and P-channel
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS\ (n\text{-}channel)}$	40	V
$R_{DS(on),max\ (n\text{-}channel)}$	25	mΩ
$I_{D\ (n\text{-}channel)}$	7.9	A
$V_{DS\ (p\text{-}channel)}$	-40	V
$R_{DS(on),max\ (p\text{-}channel)}$	30	mΩ
$I_{D\ (p\text{-}channel)}$	-7.8	A

Hal Pb RoHS

Type/Ordering Code	Package	Marking	Related Links
ISA250300C04LMDS	PG-DSO-8	2530C04L	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	7.9 5.0 4.4 5.9	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=90 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	32	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	17.2	mJ	I_D=7.9 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	2.5 1.4	W	T_C=25 °C T_A=25 °C, R_{thJA}=90 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2 for n-channel and the Diagram 17 for the p-channel. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

[3] See Diagrams 3 and 18 for more detailed information

[4] See Diagrams 13 and 28 for more detailed information

Table 3 Maximum ratings (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [5]	I_D	-	-	-7.8 -4.9 -4.1 -5.8	A	V_{GS}=-10 V, T_C=25 °C V_{GS}=-10 V, T_C=100 °C V_{GS}=-4.5 V, T_C=100 °C V_{GS}=-10 V, T_A=25 °C, R_{thJA}=90 °C/W [6]
Pulsed drain current [7]	$I_{D,pulse}$	-	-	-31	A	T_A=25 °C
Avalanche energy, single pulse [8]	E_{AS}	-	-	17.2	mJ	I_D=-7.8 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	2.5 1.4	W	T_C=25 °C T_A=25 °C, R_{thJA}=90 °C/W [6]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

[5] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2 for n-channel and the Diagram 17 for the p-channel. De-rating will be required based on the actual environmental conditions.

[6] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

7) See Diagrams 3 and 18 for more detailed information

8) See Diagrams 13 and 28 for more detailed information

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	R_{thJC}	-	-	50	°C/W	-
Thermal resistance, junction - ambient, minimal footprint, steady state	R_{thJA}	-	-	150	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area, steady state [9)]	R_{thJA}	-	-	90	°C/W	-

9) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 5 Static characteristics (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	-	2.7	V	V_{DS}=V_{GS}, I_D=1000 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	18 26	25 32	mΩ	V_{GS}=10 V, I_D=7.9 A V_{GS}=4.5 V, I_D=7.1 A
Gate resistance	R_G	-	1.5	-	Ω	-
Transconductance [10)]	g_{fs}	9.0	18	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=7.9 A

10) Defined by design. Not subject to production test.

Table 6 Static characteristics (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-40	-	-	V	V_{GS}=0 V, I_D=-1 mA
Gate threshold voltage	$V_{GS(th)}$	-1.1	-	-2.7	V	V_{DS}=V_{GS}, I_D=-1000 µA
Zero gate voltage drain current	I_{DSS}	-	-0.1 -10	-1 -100	µA	V_{DS}=-40 V, V_{GS}=0 V, T_j=25 °C V_{DS}=-40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	V_{GS}=-20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	25 35	30 44	mΩ	V_{GS}=-10 V, I_D=-7.8 A V_{GS}=-4.5 V, I_D=-7 A
Gate resistance	R_G	-	8.5	-	Ω	-
Transconductance [11)]	g_{fs}	9	18	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=-7.8 A

11) Defined by design. Not subject to production test.

Table 7 Dynamic characteristics (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [12)]	C_{iss}	-	550	720	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance [12)]	C_{oss}	-	150	200	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Reverse transfer capacitance [12)]	C_{rss}	-	10	18	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5.8	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=7.9 A, $R_{G,ext}$=1.6 Ω

Table 7 Dynamic characteristics (n-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Rise time	t_r	-	5.3	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=7.9 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	2.9	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=7.9 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	4.0	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=7.9 A, $R_{G,ext}$=1.6 Ω
Gate to source charge	Q_{gs}	-	1.8	-	nC	V_{DD}=20 V, I_D=7.9 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	0.9	-	nC	V_{DD}=20 V, I_D=7.9 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	1.0	-	nC	V_{DD}=20 V, I_D=7.9 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	1.9	-	nC	V_{DD}=20 V, I_D=7.9 A, V_{GS}=0 to 4.5 V
Gate charge total [12)]	Q_g	-	3.8	5.7	nC	V_{DD}=20 V, I_D=7.9 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	3.2	-	V	V_{DD}=20 V, I_D=7.9 A, V_{GS}=0 to 4.5 V
Gate charge total [12)]	Q_g	-	7.9	11.9	nC	V_{DD}=20 V, I_D=7.9 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	5.3	-	nC	V_{DS}=20 V, V_{GS}=0 V

12) Defined by design. Not subject to production test.

Table 8 Dynamic characteristics (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [13)]	C_{iss}	-	1200	1600	pF	V_{GS}=0 V, V_{DS}=-20 V, f=1 MHz
Output capacitance [13)]	C_{oss}	-	460	600	pF	V_{GS}=0 V, V_{DS}=-20 V, f=1 MHz
Reverse transfer capacitance [13)]	C_{rss}	-	26	46	pF	V_{GS}=0 V, V_{DS}=-20 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	V_{DD}=-20 V, V_{GS}=-4.5 V, I_D=-7.8 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	11	-	ns	V_{DD}=-20 V, V_{GS}=-4.5 V, I_D=-7.8 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	16	-	ns	V_{DD}=-20 V, V_{GS}=-4.5 V, I_D=-7.8 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	9.8	-	ns	V_{DD}=-20 V, V_{GS}=-4.5 V, I_D=-7.8 A, $R_{G,ext}$=1.6 Ω
Gate to source charge	Q_{gs}	-	-3.8	-	nC	V_{DD}=-20 V, I_D=-7.8 A, V_{GS}=0 to -4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	-2.0	-	nC	V_{DD}=-20 V, I_D=-7.8 A, V_{GS}=0 to -4.5 V
Gate to drain charge	Q_{gd}	-	-2.4	-	nC	V_{DD}=-20 V, I_D=-7.8 A, V_{GS}=0 to -4.5 V
Switching charge	Q_{sw}	-	-4.2	-	nC	V_{DD}=-20 V, I_D=-7.8 A, V_{GS}=0 to -4.5 V
Gate charge total [13)]	Q_g	-	-8.1	-12	nC	V_{DD}=-20 V, I_D=-7.8 A, V_{GS}=0 to -4.5 V

Table 8 Dynamic characteristics (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate plateau voltage	$V_{plateau}$	-	-3.2	-	V	V_{DD}=-20 V, I_D=-7.8 A, V_{GS}=0 to -4.5 V
Gate charge total	Q_g	-	-16.1	-24	nC	V_{DD}=-20 V, I_D=-7.8 A, V_{GS}=0 to -10 V
Output charge	Q_{oss}	-	-14	-	nC	V_{DS}=-20 V, V_{GS}=0 V

13) Defined by design. Not subject to production test.

Table 9 Reverse diode (n-channel)

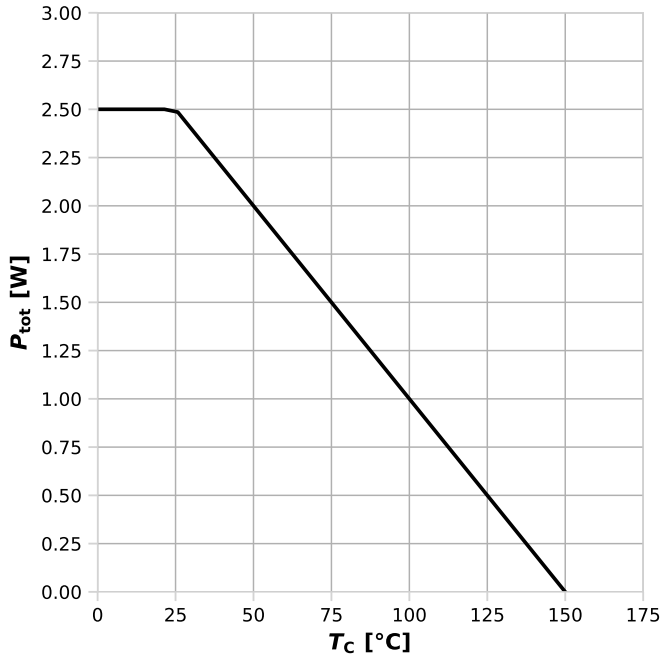
Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	3.1	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	32	A	T_A=25 °C
Diode forward voltage	V_{SD}	-	0.87	1.0	V	V_{GS}=0 V, I_F=7.9 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	12	-	ns	V_R=20 V, I_F=7.9 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	3.6	-	nC	V_R=20 V, I_F=7.9 A, di_F/dt=100 A/µs

Table 10 Reverse diode (p-channel)

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-3.5	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	-31	A	T_A=25 °C
Diode forward voltage	V_{SD}	-	-0.88	-1.0	V	V_{GS}=0 V, I_F=-7.8 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	18	-	ns	V_R=-20 V, I_F=-7.8 A, di_F/dt=-100 A/µs
Reverse recovery charge	Q_{rr}	-	6.9	-	nC	V_R=-20 V, I_F=-7.8 A, di_F/dt=-100 A/µs

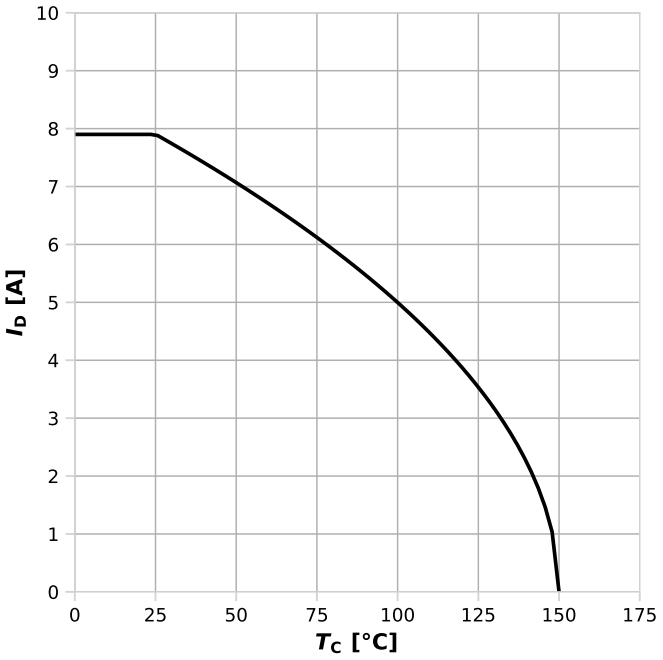
4 Electrical characteristics diagrams

Diagram 1: Power dissipation (n-channel)



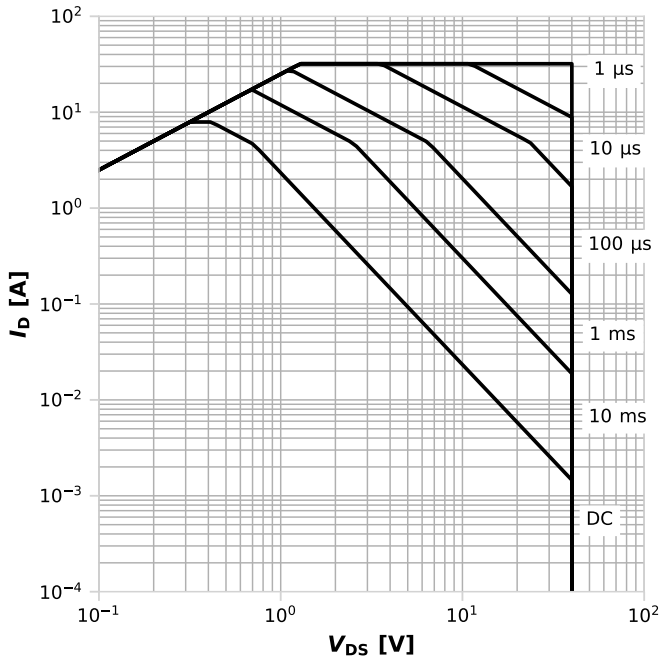
P_{tot}=f(T_C)

Diagram 2: Drain current (n-channel)



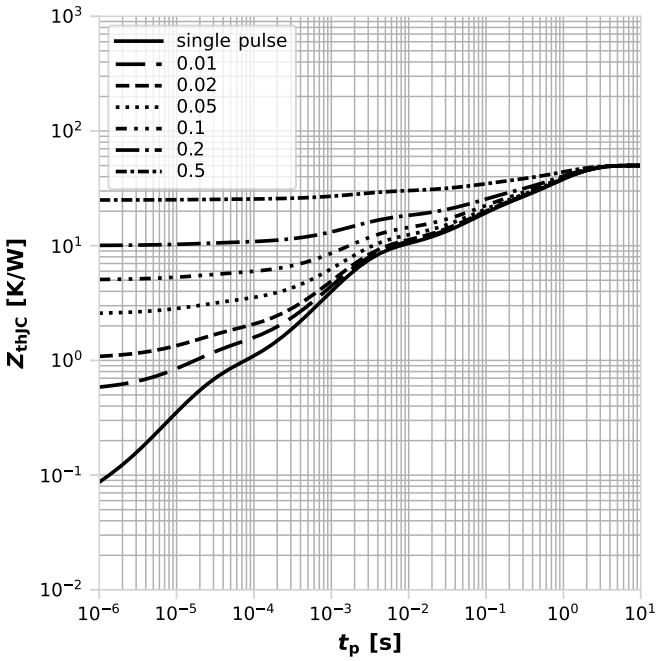
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area (n-channel)



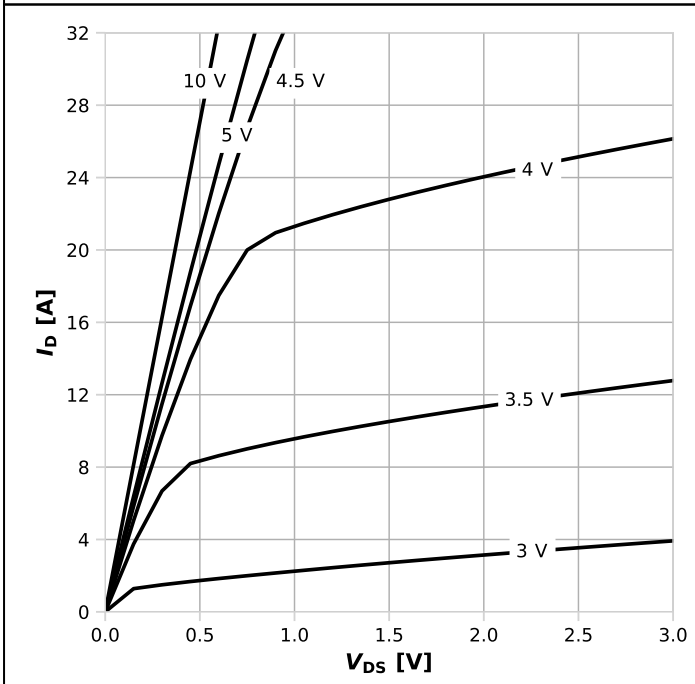
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance (n-channel)



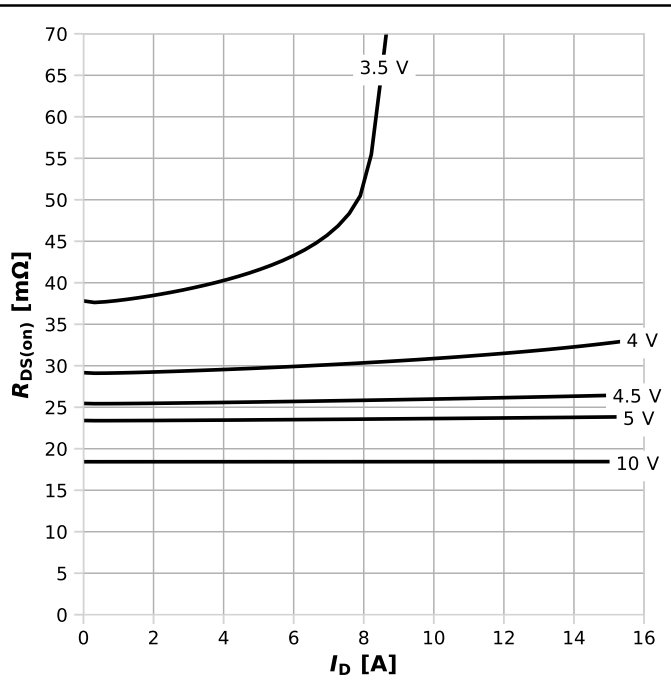
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics (n-channel)



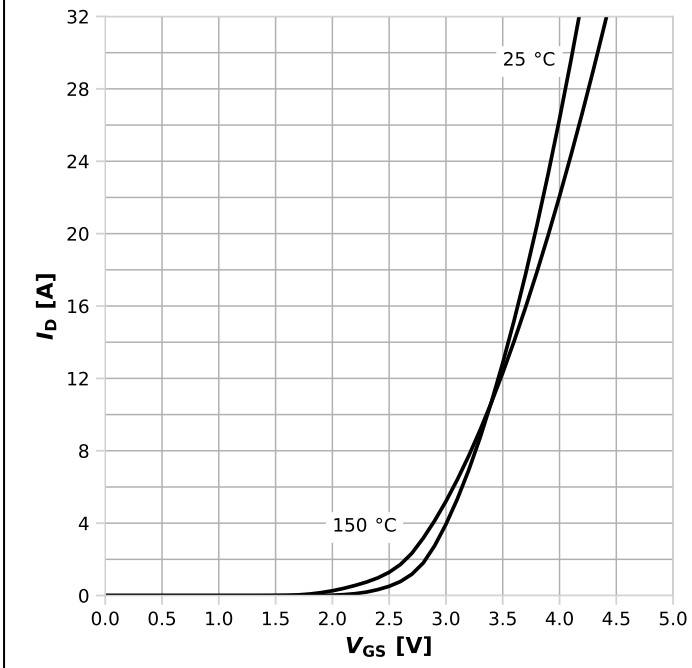
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance (n-channel)



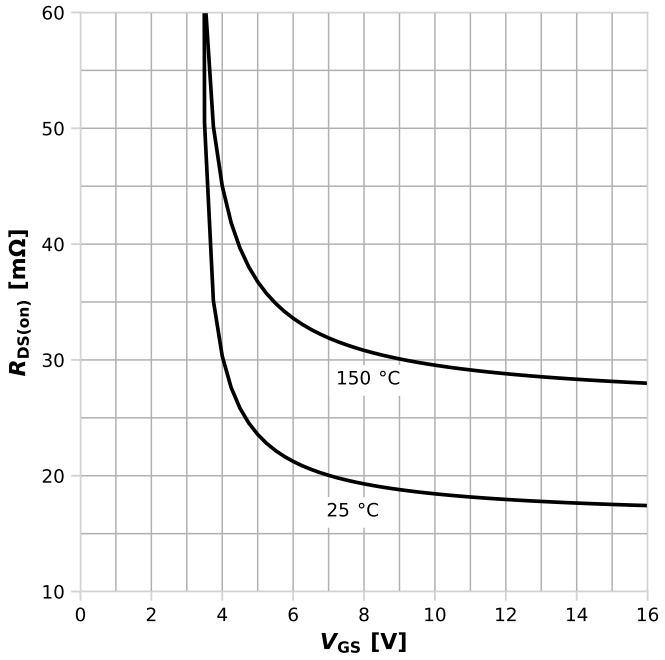
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics (n-channel)



I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance (n-channel)



$R_{DS(on)}$=f(V_{GS}), I_D=7.9 A; parameter: T_j

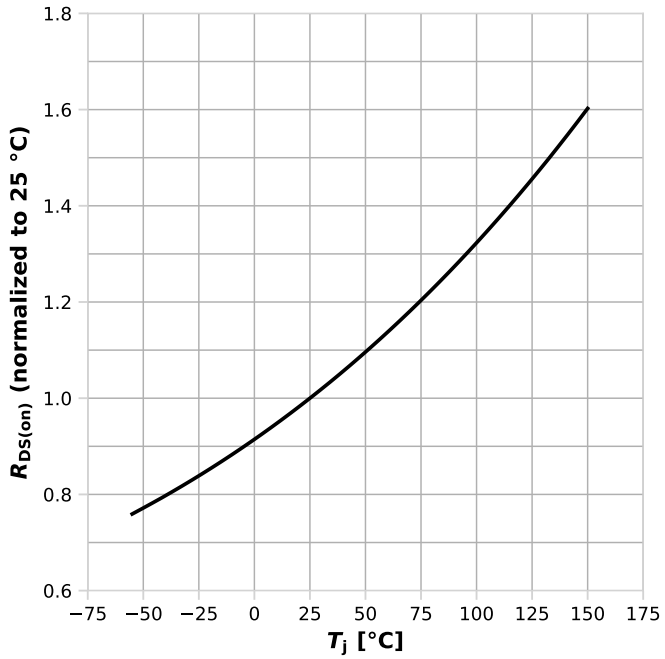
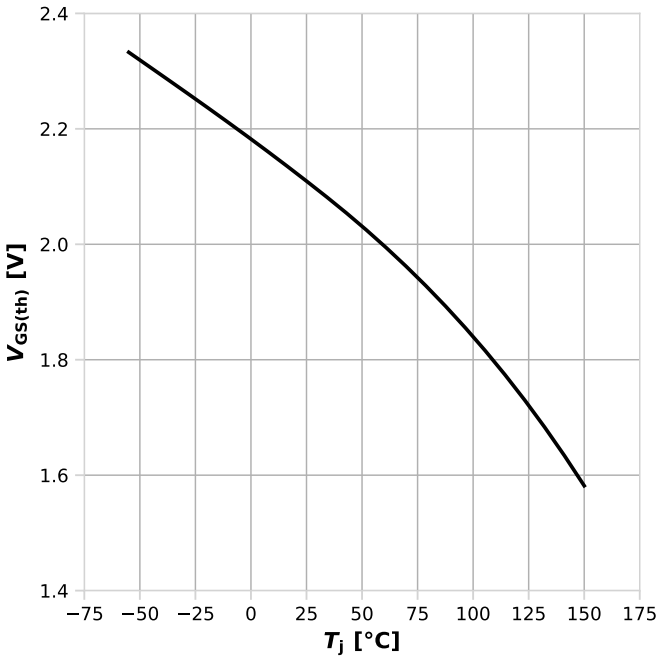
Diagram 9: Normalized drain-source on resistance (n-channel)	Diagram 10: Typ. gate threshold voltage (n-channel)
	
$R_{DS(on)}$=f(T_j), I_D=7.9 A, V_{GS}=10 V	$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D=1000µA

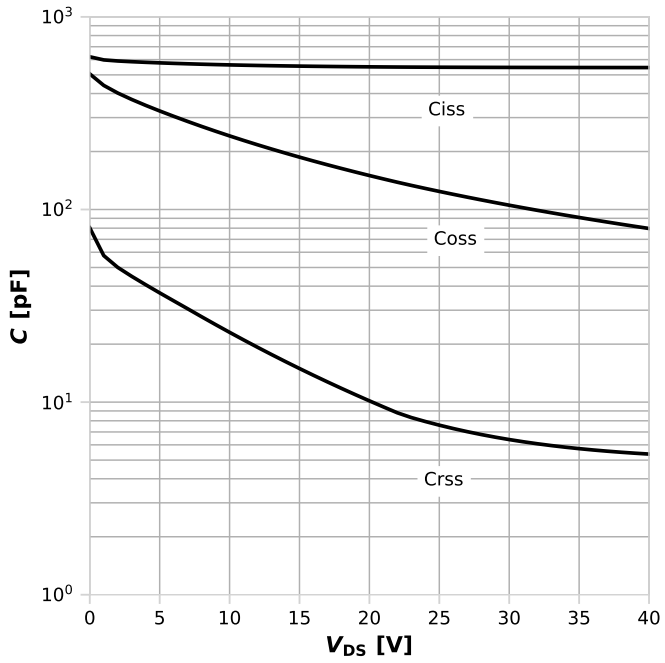
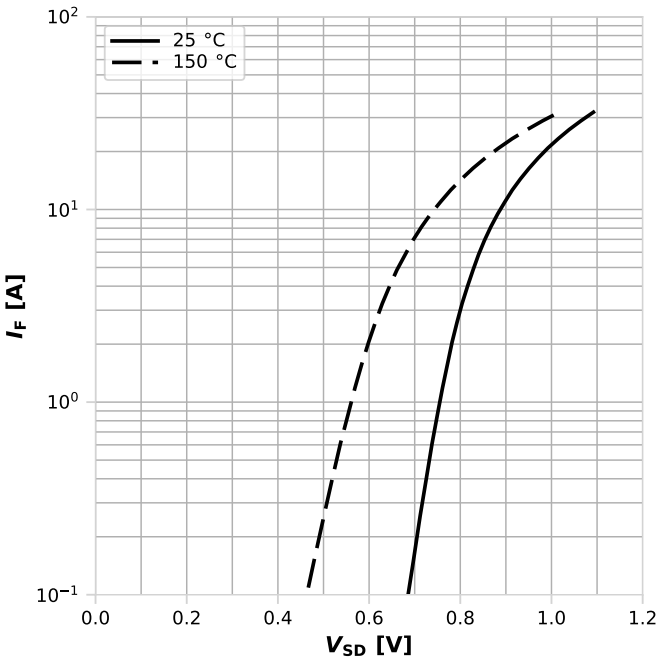
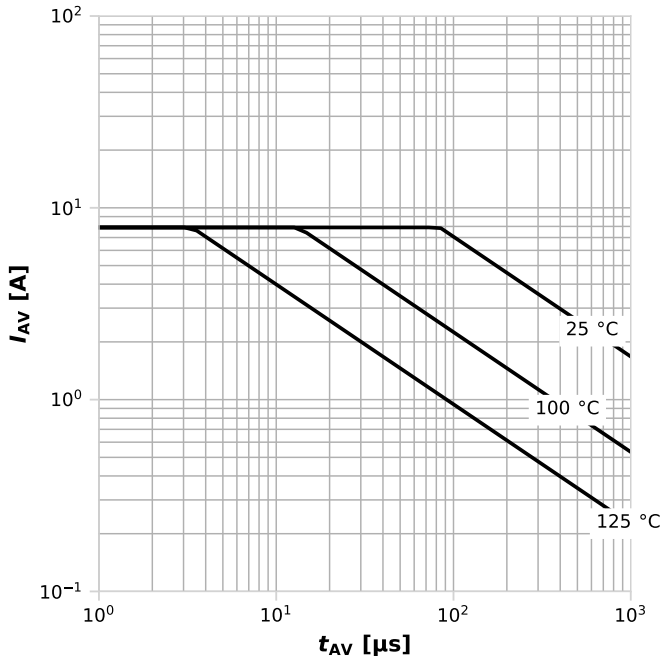
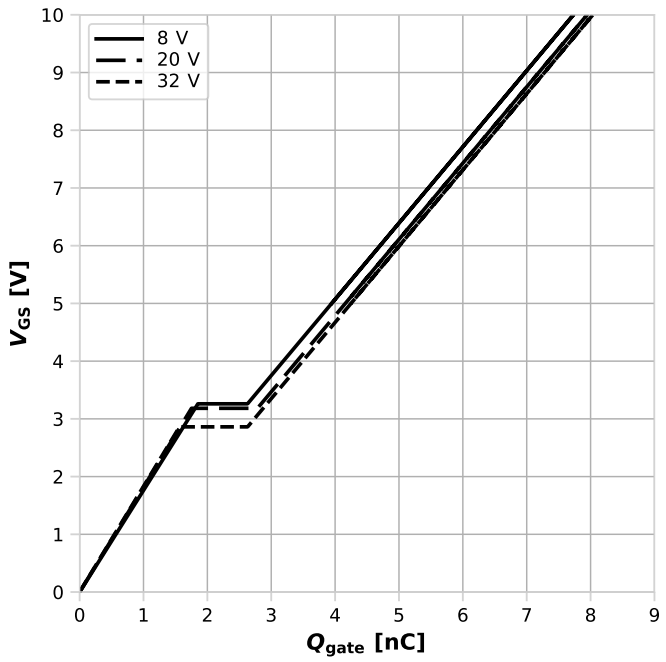
Diagram 11: Typ. capacitances (n-channel)	Diagram 12: Forward characteristics of reverse diode (n-ch.)
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics (n-channel)



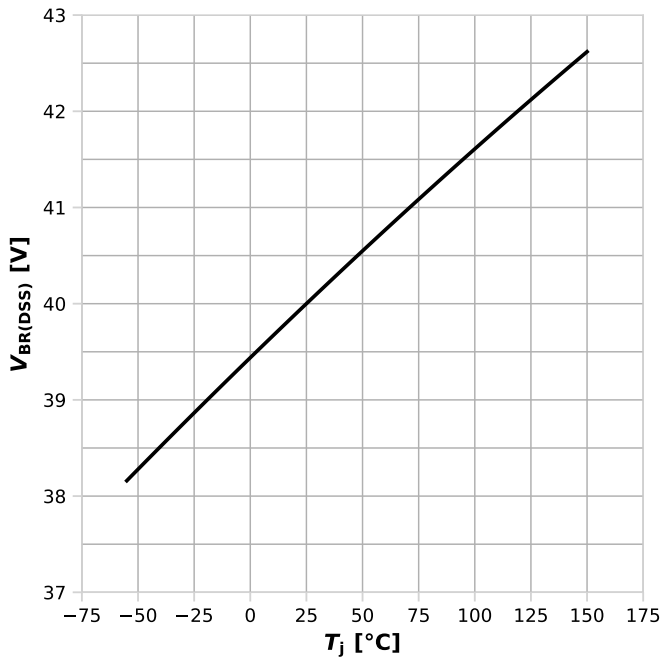
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge (n-channel)



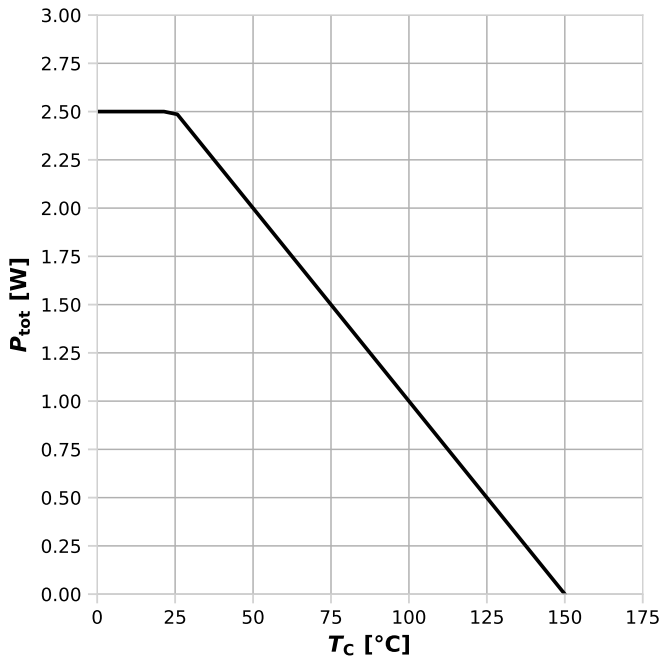
V_{GS}=f(Q_{gate}), I_D=7.9 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage (n-channel)



$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 16: Power dissipation (p-channel)



P_{tot}=f(T_C)

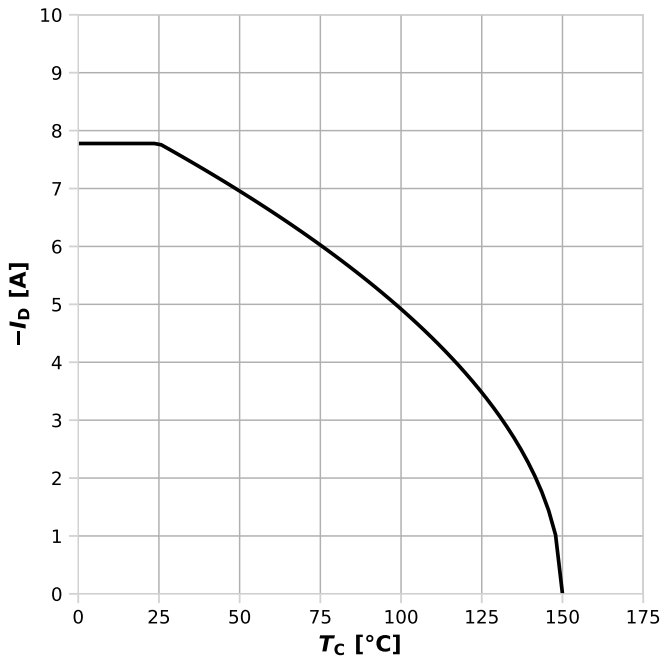
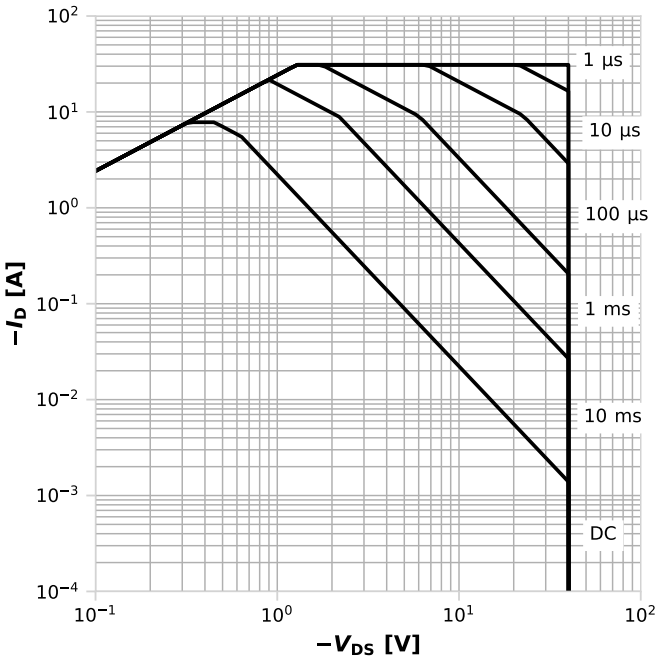
Diagram 17: Drain current (p-channel)	Diagram 18: Safe operating area (p-channel)
	
I_D=f(T_C); |V_{GS}|≥10 V	I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

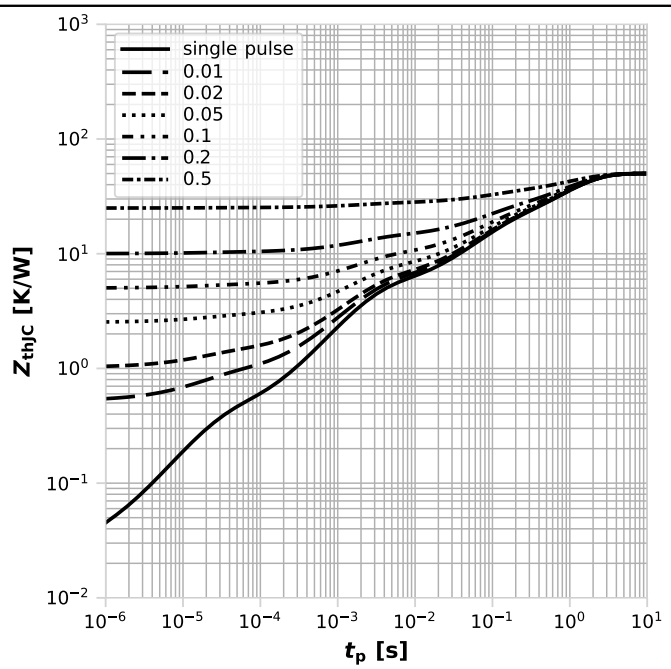
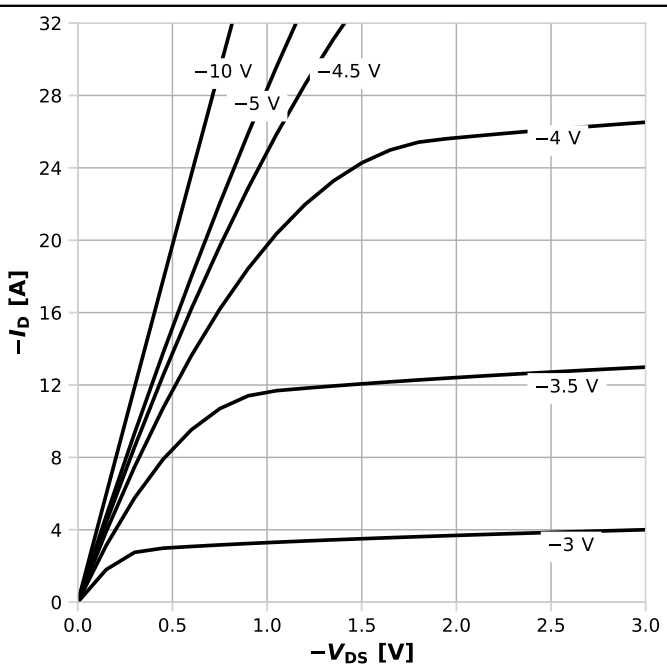
Diagram 19: Max. transient thermal impedance (p-channel)	Diagram 20: Typ. output characteristics (p-channel)
	
Z_{thJC}=f(t_p); parameter: D=t_p/T	I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

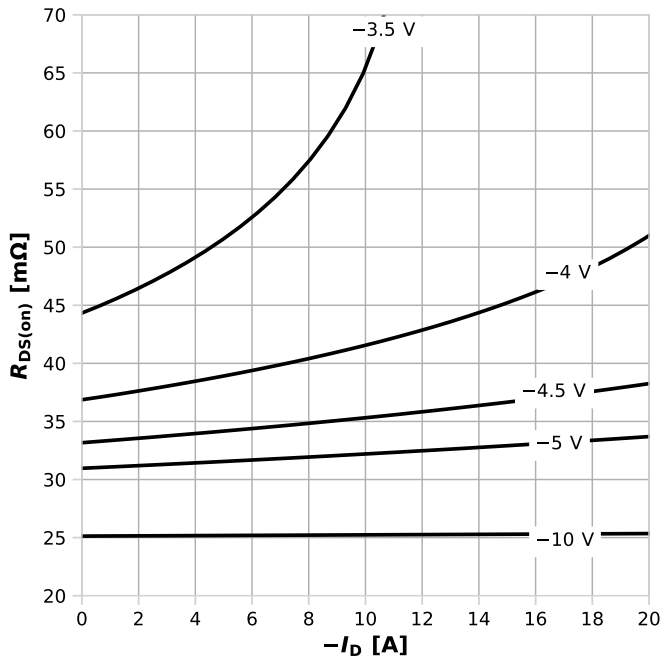
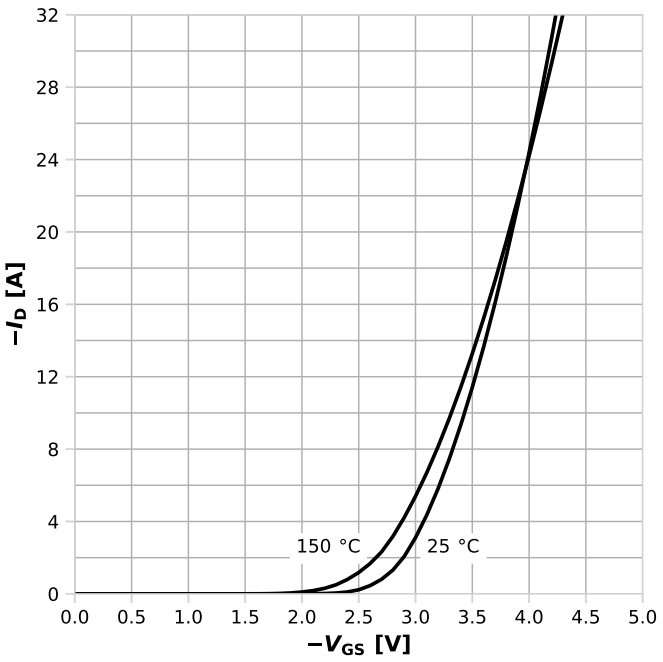
Diagram 21: Typ. drain-source on resistance (p-channel)	Diagram 22: Typ. transfer characteristics (p-channel)
	
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}	I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

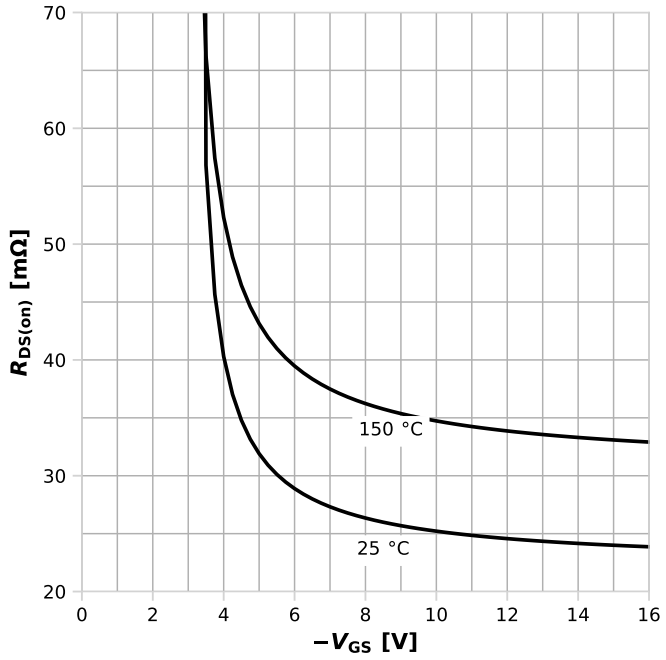
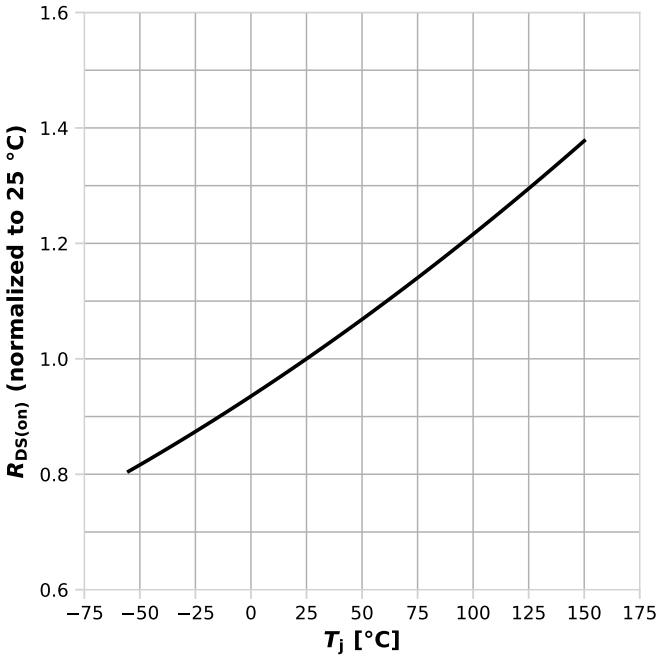
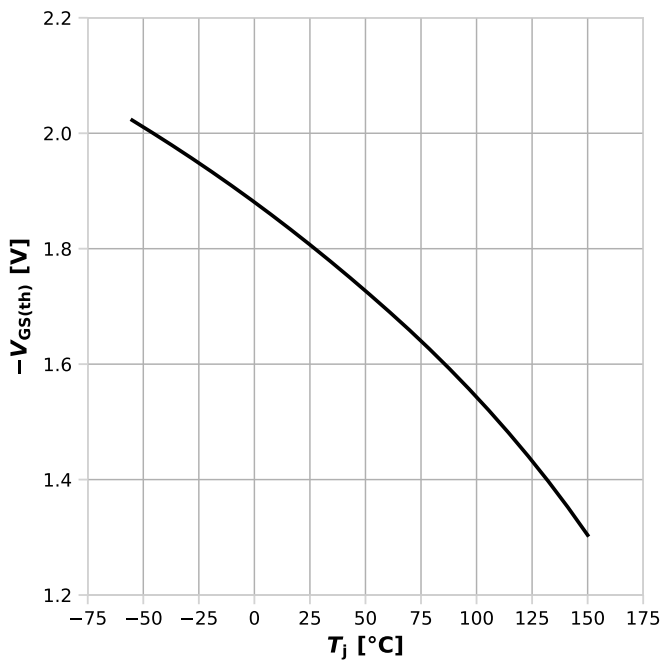
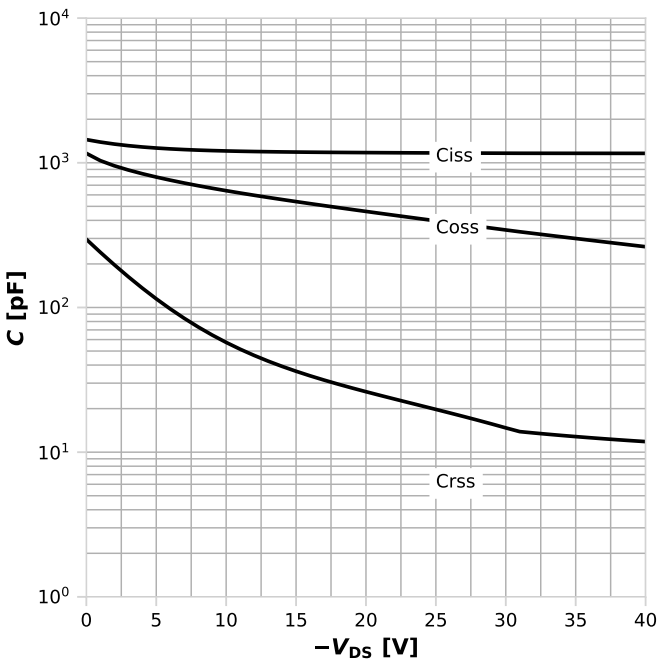
Diagram 23: Typ. drain-source on resistance (p-channel)	Diagram 24: Normalized drain-source on resistance
	
$R_{DS(on)}$=f(V_{GS}), I_D=-7.8 A; parameter: T_j	$R_{DS(on)}$=f(T_j), I_D=-7.8 A, V_{GS}=-10 V

Diagram 25: Typ. gate threshold voltage (p-channel)



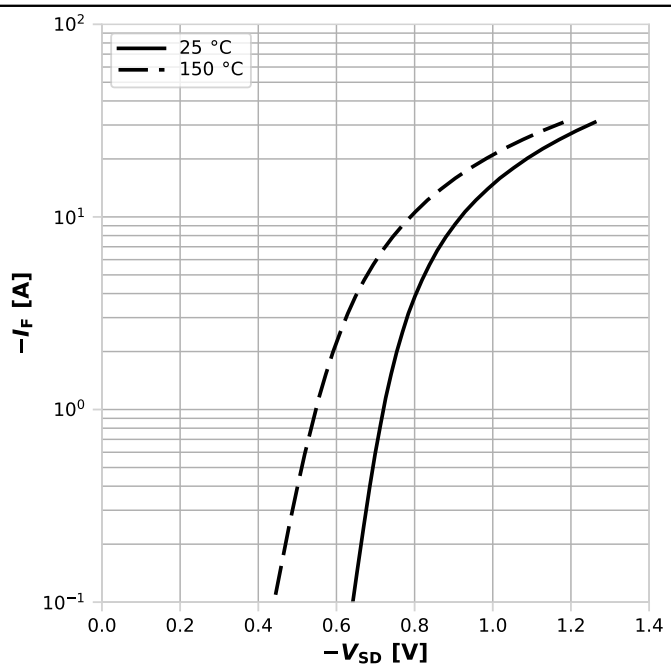
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D=1000µA

Diagram 26: Typ. capacitances (p-channel)



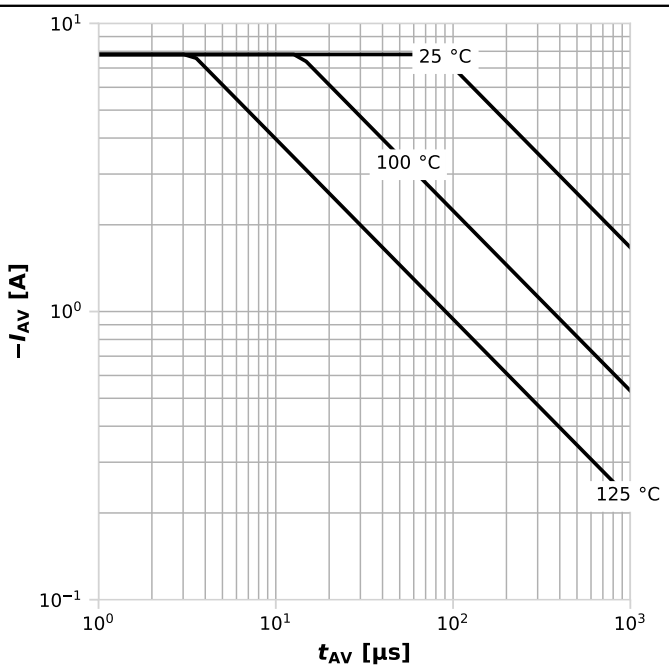
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 27: Forward characteristics of reverse diode (p-ch.)

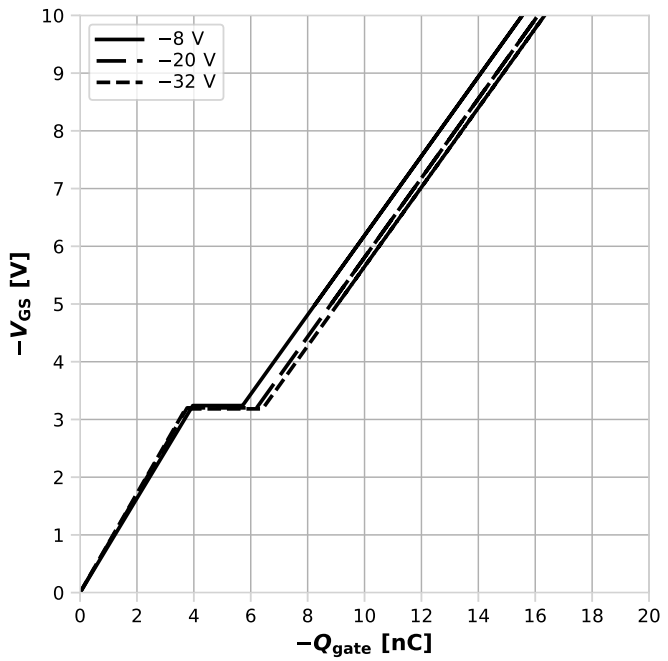
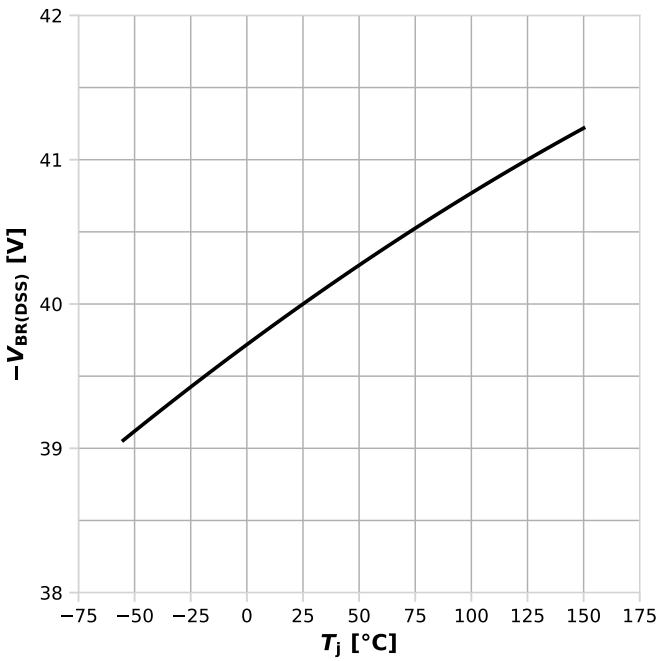


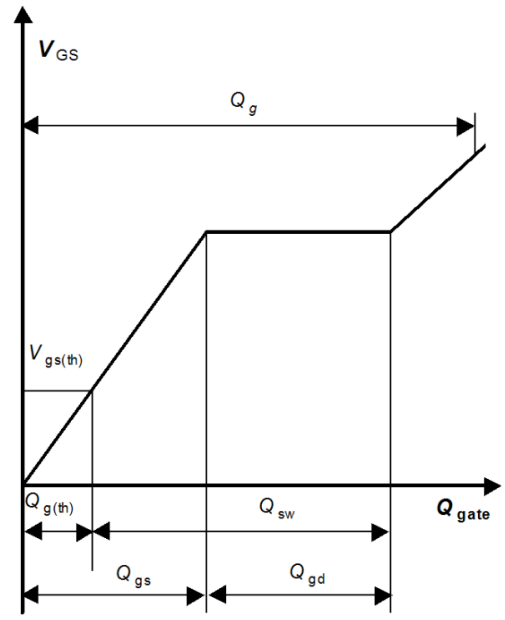
I_F=f(V_{SD}); parameter: T_j

Diagram 28: Avalanche characteristics (p-channel)



I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 29: Typ. gate charge (p-channel)	Diagram 30: Drain-source breakdown voltage (p-channel)
	
V_{GS}=f(Q_{gate}), I_D=-7.8 A pulsed, T_j=25 °C; parameter: V_{DD}	$V_{BR(DSS)}$=f(T_j); I_D=-1 mA

Gate charge waveforms

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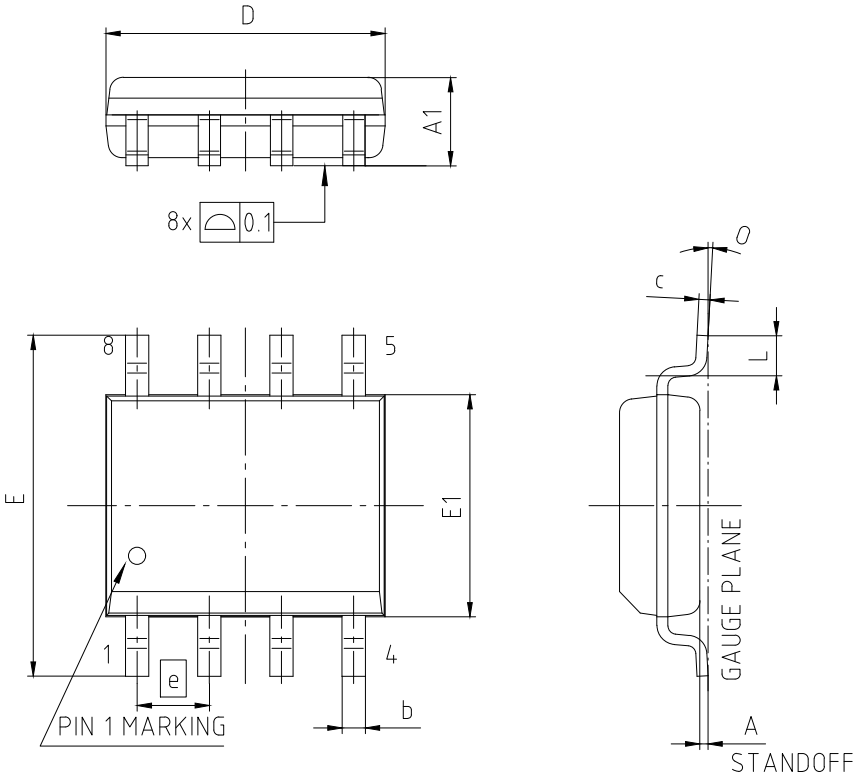
5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-DSO-8-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.18	0.25
A1	1.35	1.75
b	0.38	0.51
c	0.254	
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27	
L	0.48	0.91
O	4°	
N	8	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-DSO-8, dimensions in mm

Revision History

ISA250300C04LMDS

Revision 2024-10-02, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-10-02	Release of final datasheet

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