Low-I_Q Boost/SEPIC/ Inverting Converter with 1A, 60V Switch

FEATURES

- **3.2V to 36V Input Voltage Range**
- **Low Quiescent Current and Low Ripple Burst Mode® Operation: I_Q = 6µA**
- **1A, 60V Power Switch**
- **Positive or Negative Output Voltage Programming with a Single Feedback Pin**
- **Fixed 2MHz Switching Frequency**
- **Accurate 1.6V EN/UVLO Pin Threshold**
- Internal Compensation and Soft-Start
- Low Profile (1mm) ThinSOT™ Package
- Low Profile (0.75mm) 8-Lead (3mm x 2mm) DFN Package

APPLICATIONS

- Industrial
- Telecom
- Medical Diagnostic Equipment
- Portable Electronics

GENERAL DESCRIPTION

The ADPL26001 is a current-mode DC/DC converter capable of generating either positive or negative output voltages using a single feedback pin. It can be configured as a boost, single-ended primary inductance converter (SEPIC), or inverting converter consuming as low as 6µA of quiescent current. Low ripple Burst Mode operation maintains high efficiency down to very low output currents while keeping the output ripple below 15mV in a typical application. The internally compensated current-mode architecture results in stable operation over a wide range of input and output voltages. Integrated soft-start and frequency foldback functions are included to control inductor current during start-up. The ADPL26001 comes in small package options that combined with a high switching frequency of 2MHz, helps to maintain a small footprint for an overall efficient, space-saving and cost-effective solution.

SIMPLIFIED APPLICATION DIAGRAM

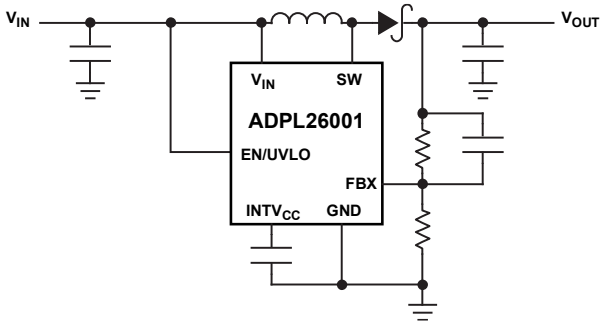

Figure 1. Simplified Boost Converter

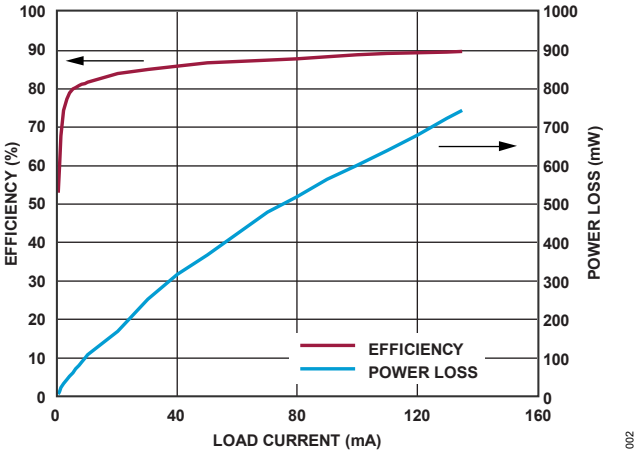

Figure 2. Efficiency and Power Loss vs. Load Current (Figure 30 Circuit)

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SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = T_J = –40°C to 125°C, V_{IN} = 12V, EN/UVLO = 12V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage Range	V_{IN}		3.2		36	V
V_{IN} Quiescent Current at Shutdown	I_{Q-SD}	$V_{EN/UVLO}$ = 0.2V, T_A = 25°C		0.9	2	µA
		$V_{EN/UVLO}$ = 0.2V		2	5	
		$V_{EN/UVLO}$ = 1.5V, T_A = 25°C		2	5	
		$V_{EN/UVLO}$ = 1.5V		3.6	9.5	
V_{IN} Quiescent Current	I_Q	Sleep Mode, Not Switching, T_A = 25°C		5.5	10	µA
		Sleep Mode, Not Switching		8.5	15	
		Active Mode, Not Switching, T_A = 25°C		780	1100	
		Active Mode, Not Switching		840	1200	
FBX Regulation						
FBX Regulation Voltage	V_{FBX_REG}	FBX > 0V	1.568	1.6	1.632	V
		FBX < 0V	–0.820	–0.80	–0.780	
FBX Line Regulation		FBX > 0V, 3.2V < V_{IN} < 36V, T_A = 25°C		0.005	0.015	%/V
		FBX < 0V, 3.2V < V_{IN} < 36V, T_A = 25°C		0.005	0.015	
FBX Pin Current	I_{FBX}	FBX = 1.6V, –0.8V	–10		10	nA
Oscillator						
Switching Frequency (f_{OSC})	f_{SW}	V_{IN} = 24V	1.8	2.0	2.2	MHz
Minimum On-Time	t_{ON_MIN}	V_{IN} = 24V, T_A = 25°C		70	110	ns
Minimum Off-Time	t_{OFF_MIN}	V_{IN} = 24V, T_A = 25°C		50	70	ns
Switch						
Maximum Switch Current-Limit Threshold	I_{SW_LIM}		1.0	1.2	1.5	A
Switch $R_{DS(ON)}$	$R_{DS(ON)}$	I_{SW} = 0.5A, T_A = 25°C		400		mΩ
Switch Leakage Current	I_{SW_LKG}	V_{SW} = 60V, T_A = 25°C		0.1	1	µA
EN/UVLO Logic						
EN/UVLO Pin Threshold (Rising)	V_{EN_R}	Start Switching	1.620	1.68	1.755	V
EN/UVLO Pin Threshold (Falling)	V_{EN_F}	Stop Switching	1.556	1.60	1.644	V
EN/UVLO Pin Current	I_{EN}	$V_{EN/UVLO}$ = 1.6V	–40		40	nA
Soft-Start						
Soft-Start Time	t_{SS}	V_{IN} = 24V, T_A = 25°C		1		ms

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
SW	60V
V_{IN}, EN/UVLO	36V
EN/UVLO Pin Above V_{IN} Pin	6V
$INTV_{CC}$[1]	4V
FBX	±4V
Temperature Range	
Operating Junction[2, 3]	−40°C to 125°C
Storage	−65°C to 150°C

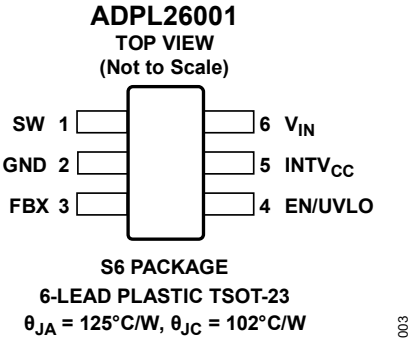
1 $INTV_{CC}$ cannot be externally driven. No additional components or loading is allowed on this pin.

2 Junction temperature greater than +125°C degrades operating lifetimes.

3 The IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature exceeds 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature reduces the lifetime.

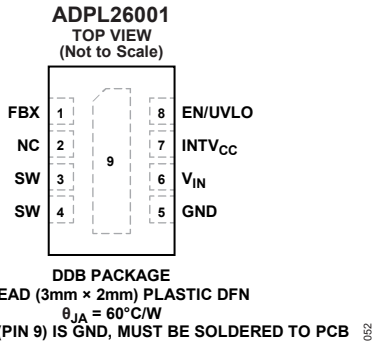
Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
θ_{JA} = 125°C/W, θ_{JC} = 102°C/W

Figure 3. Pin Configuration TSOT



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
θ_{JA} = 60°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

Figure 4. Pin Configuration DFN

Figure 5.

Pin Descriptions

Table 3. Pin Descriptions

PIN		NAME	DESCRIPTION
TSOT	DFN		
1	3, 4	SW	The Output of Internal Power Switch. Minimize the metal trace area connected to this pin to reduce EMI.
2	5	GND	Ground Connection for the ADPL26001. The DFN package has the best thermal performance due to an exposed pad (Pin 9) on the bottom of the package. This exposed pad must be soldered to the ground plane. The pin 5 of the DFN package (and Pin 2 of the TSOT package) should also be connected to the ground plane. Connect the ground pin to large copper layers to spread heat dissipated by the ADPL26001.
3	1	FBX	Voltage Regulation Feedback Pin for Positive or Negative Outputs. Connect this pin to a resistor-divider between the output and GND. FBX reduces the switching frequency during start-up and fault conditions when FBX is close to GND.
4	8	EN/UVLO	Shutdown and Undervoltage Detect Pin. The ADPL26001 shuts down when this pin is low and active when this pin is high. Below an accurate 1.6V threshold the part enters undervoltage lockout and stops switching. This allows an undervoltage lockout (UVLO) threshold to be programmed for system input voltage by resistively dividing down system input voltage to the EN/UVLO pin. An 80mV pin hysteresis ensures part switching resumes when the pin exceeds 1.68V. EN/UVLO pin voltage below 0.2V reduces V_{IN} current below 1µA. If shutdown and UVLO features are not required, the pin can be connected directly to system input.
5	7	$INTV_{CC}$	Regulated 3V Supply for Internal Loads. The $INTV_{CC}$ pin must be bypassed with a minimum 1µF low equivalent series resistance (ESR) ceramic capacitor to ground. No additional components or loading is allowed on this pin.
6	6	V_{IN}	Input Supply. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN} pin, and the negative terminal as close as possible to the GND pin.
—	2	NC	No Internal Connection. Tie directly to local ground.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

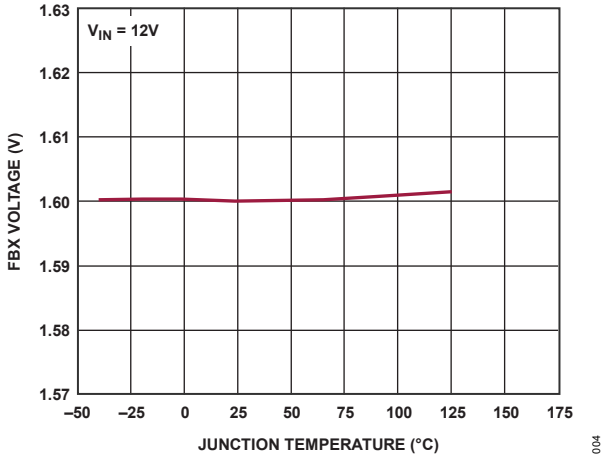


Figure 6. FBX Positive Regulation Voltage vs. Temperature

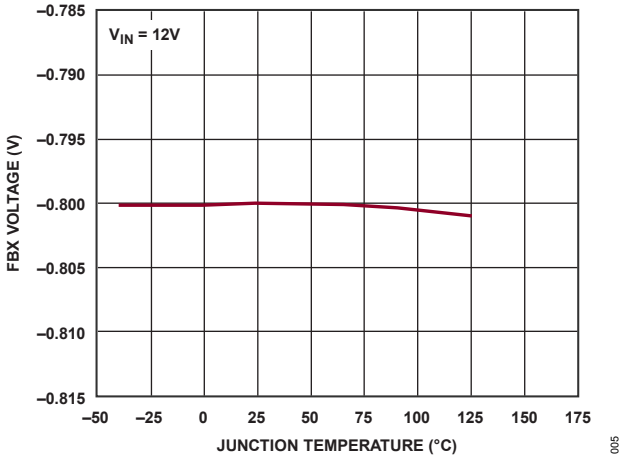


Figure 7. FBX Negative Regulation Voltage vs. Temperature

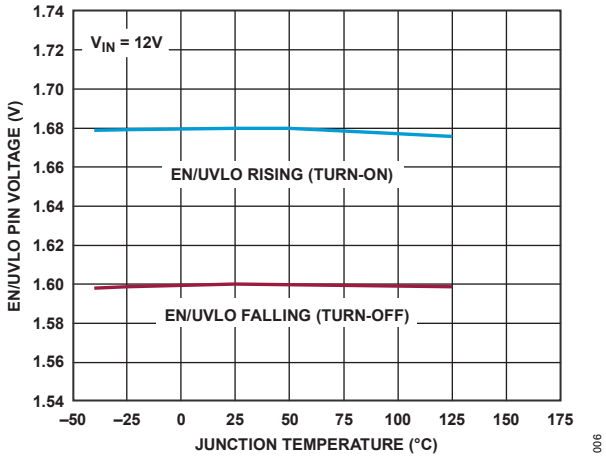


Figure 8. EN/UVLO Pin Thresholds vs. Temperature

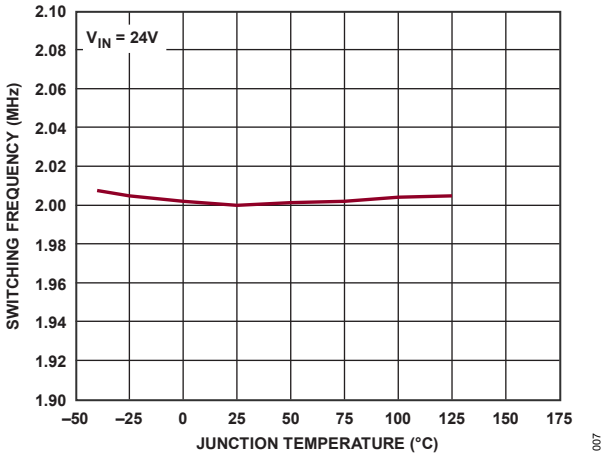


Figure 9. Switching Frequency vs. Temperature

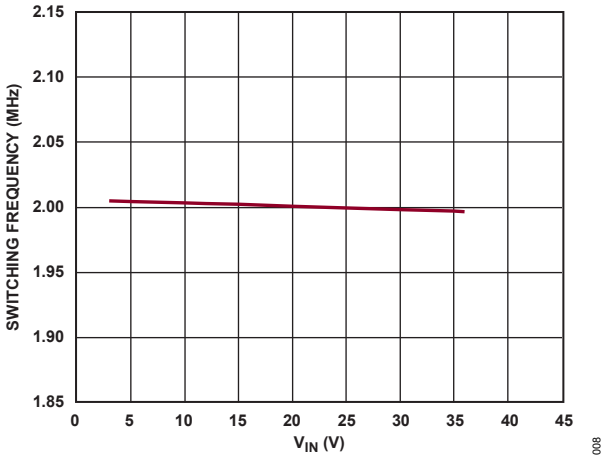


Figure 10.Switching Frequency vs. V_{IN}

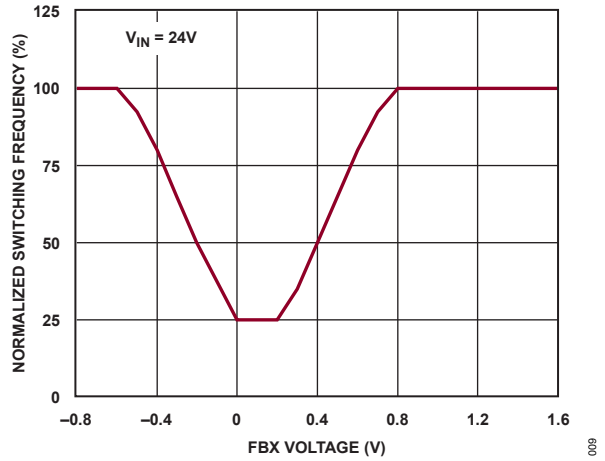


Figure 11. Normalized Switching Frequency vs. FBX Voltage

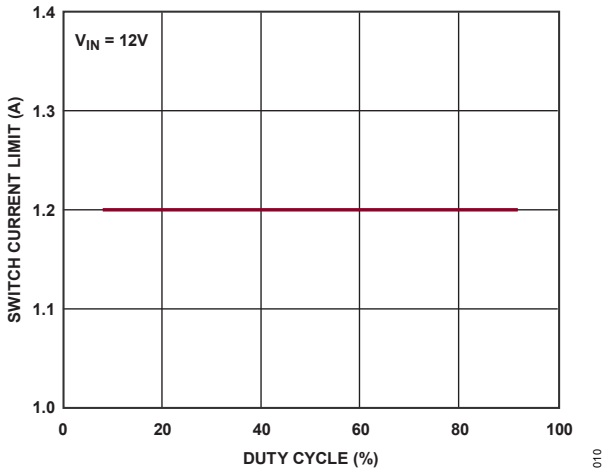


Figure 12. Switch Current-Limit vs. Duty Cycle

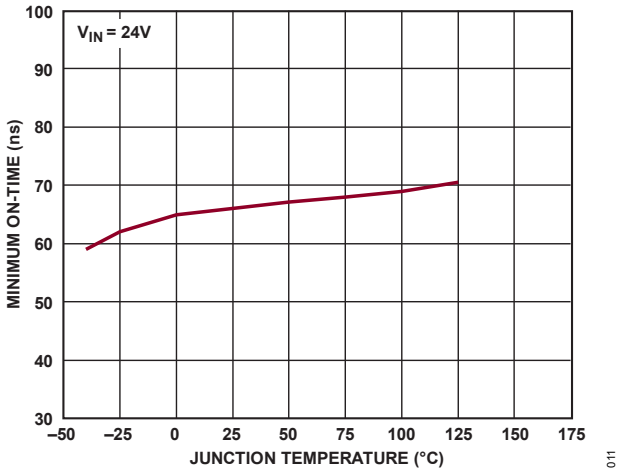


Figure 13. Switch Minimum On-Time vs. Temperature

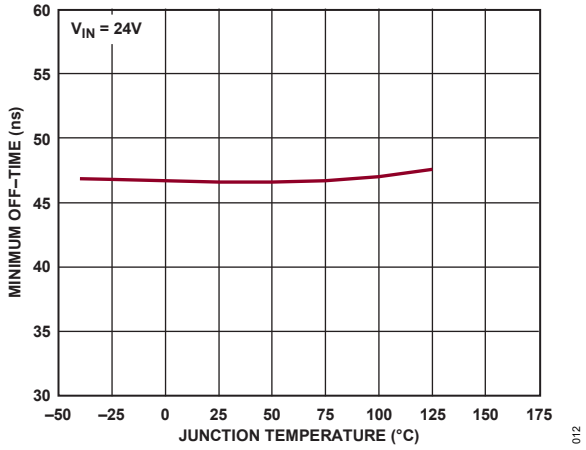


Figure 14. Switch Minimum Off-Time vs. Temperature

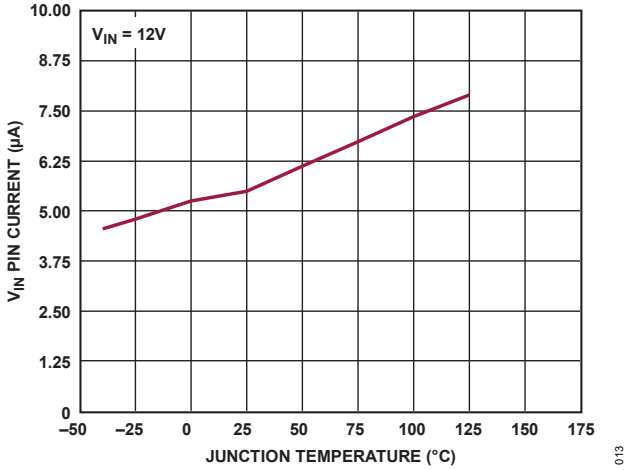


Figure 15. V_{IN} Pin Current (Sleep Mode, Not Switching) vs. Temperature

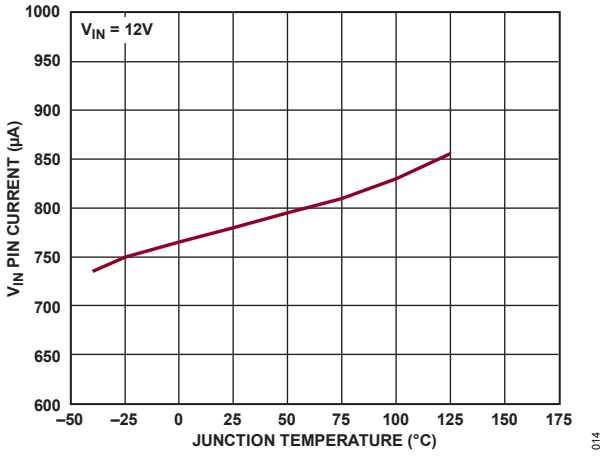


Figure 16. V_{IN} Pin Current (Active Mode, Not Switching) vs. Temperature

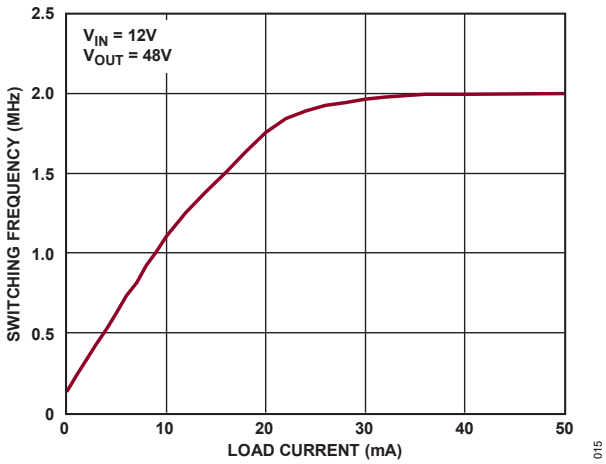


Figure 17. Burst Frequency vs. Load Current (Figure 30 Circuit)

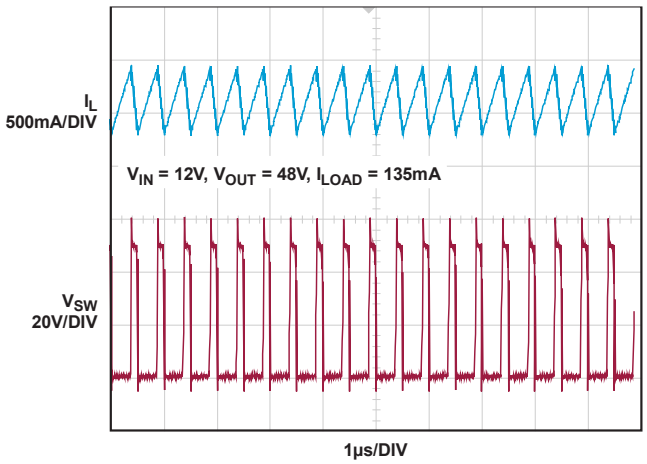


Figure 18. Switching Waveforms (Figure 30 Circuit in CCM)

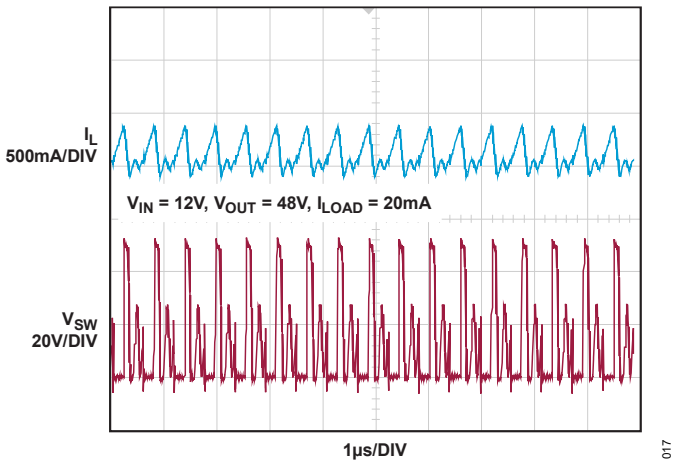


Figure 19. Switching Waveforms (Figure 30 Circuit in DCM/Light Burst Mode)

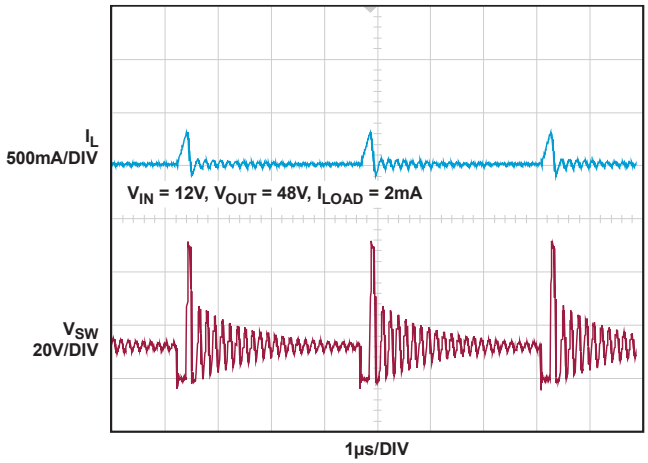


Figure 20. Switching Waveforms (Figure 30 Circuit in Deep Burst Mode)

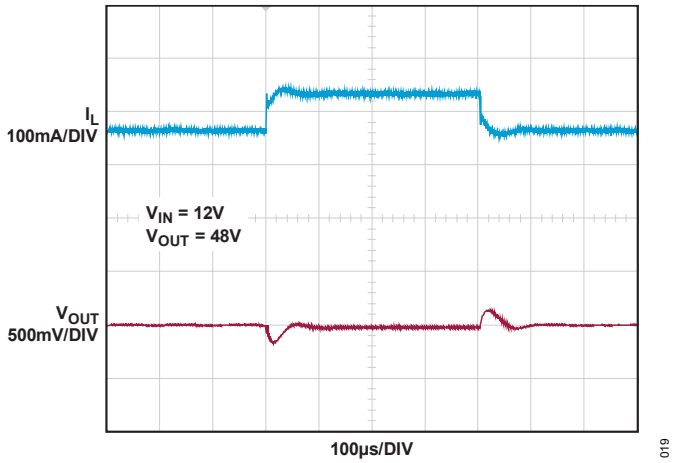


Figure 21. V_{OUT} Transient-Response: Load Current Transients from 67.5mA to 135mA to 67.5mA (Figure 30 Circuit)

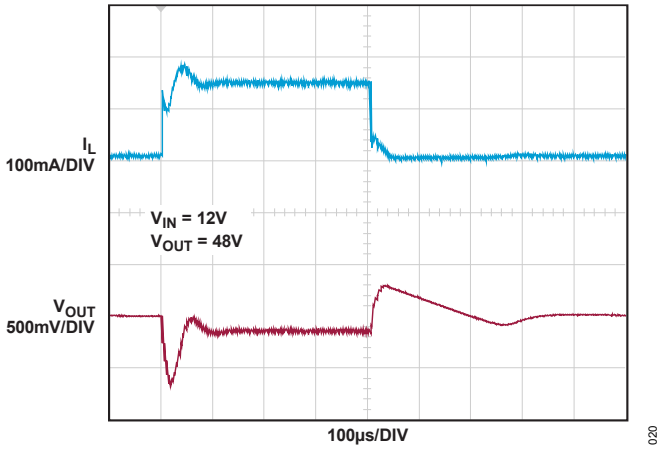
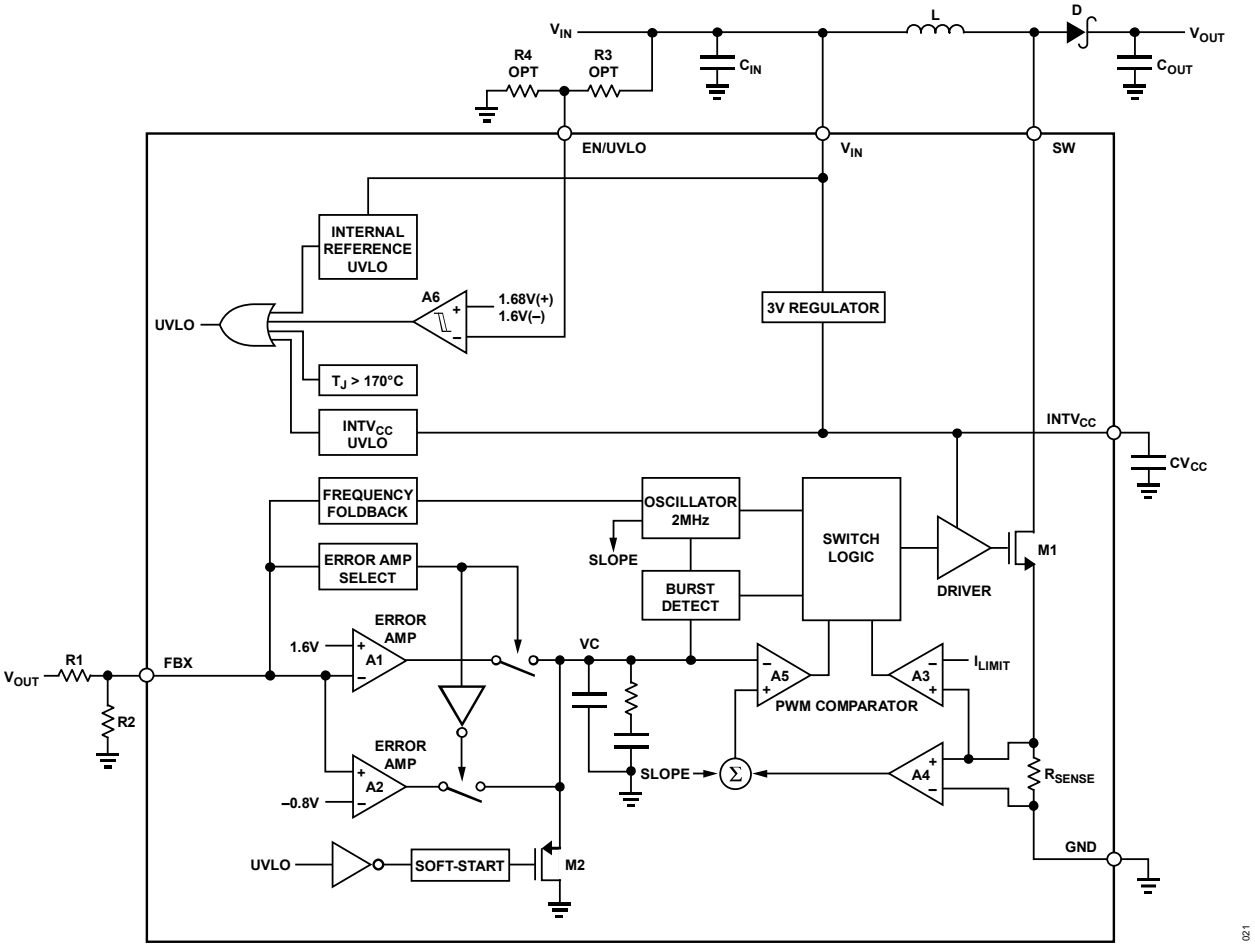


Figure 22. V_{OUT} Transient-Response: Load Current Transients from 5mA to 135mA to 5mA (Figure 30 Circuit)

BLOCK DIAGRAM



THEORY OF OPERATION

The ADPL26001 uses a fixed frequency, current-mode control scheme to provide excellent line and load regulation. For better understanding of the operation, see *Block Diagram*. An internal 2MHz oscillator turns on the internal power switch at the beginning of each clock cycle. Current in the inductor then increases until the current comparator trips and turns off the power switch. The peak inductor current at which the switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the FBX pin with an internal reference voltage (1.60V or –0.80V, which depends on the chosen topology). When the load current increases it causes a reduction in the FBX pin voltage relative to the internal reference. This causes the error amplifier to increase the VC voltage until the new load current is satisfied. In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation.

The ADPL26001 is capable of generating either a positive or negative output voltage with a single FBX pin. It can be configured as a boost or SEPIC converter to generate a positive output voltage, or as an inverting converter to generate a negative output voltage. When configured as a boost converter as shown in the *Block Diagram*, the FBX pin is pulled up to the internal bias voltage of 1.60V by a voltage-divider (R1 and R2) connected from V_{OUT} to GND. Amplifier A2 becomes inactive and amplifier A1 performs (inverting) amplification from FBX to VC. When the ADPL26001 is in an inverting configuration, the FBX pin is pulled down to –0.80V by a voltage-divider from V_{OUT} to GND. Amplifier A1 becomes inactive and amplifier A2 performs (noninverting) amplification from FBX to VC.

If the EN/UVLO pin voltage is below 1.6V, the ADPL26001 enters UVLO, and stops switching. When the EN/UVLO pin voltage is above 1.68V (typical), the ADPL26001 resumes switching. If the EN/UVLO pin voltage is below 0.2V, the ADPL26001 only draws 1µA from V_{IN}.

To optimize efficiency at light loads, the ADPL26001 operates in Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch shuts down, which reduces the input supply current to 6µA.

APPLICATIONS INFORMATION

Achieving Ultra-Low Quiescent Current

To enhance efficiency at light loads the ADPL26001 uses a low-ripple Burst Mode architecture. This keeps the output capacitor charged to the required output voltage while minimizing the input quiescent current and output ripple. In Burst Mode operation, the ADPL26001 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the ADPL26001 consumes only 6µA.

As the output load decreases, the frequency of single current pulses decreases (see *Figure 23*) and the percentage of time the ADPL26001 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. To optimize the quiescent current performance at light loads, the current in the feedback resistor-divider must be minimized as it appears to the output as load current. In addition, all possible leakage currents from the output should also be minimized as they all add to the equivalent output load. The largest contributor to leakage current can be due to the reverse biased leakage of the Schottky diode (for more information, see the *Diode Selection* section).

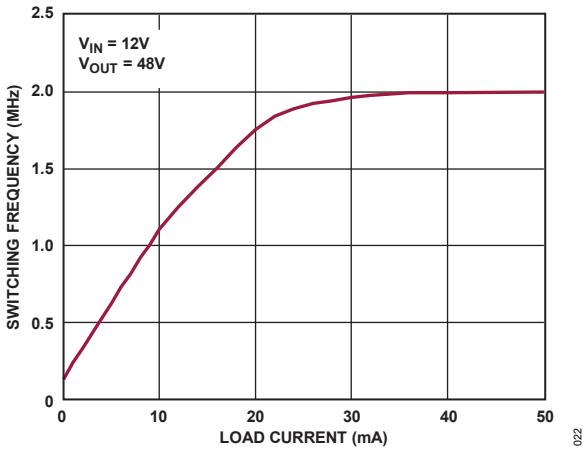


Figure 23. Burst Frequency vs. Load Current (Figure 30 Circuit)

While in Burst Mode operation, the current-limit of the switch is approximately 240mA, resulting in the output voltage ripple shown in *Figure 24*. Increasing the output capacitance decreases the output ripple proportionally. As the output load ramps upward from zero the switching frequency increases but only up to the fixed 2MHz defined by the internal oscillator as shown in *Figure 23*. The output load at which the ADPL26001 reaches the fixed 2MHz frequency varies based on input voltage, output voltage, and inductor choice.

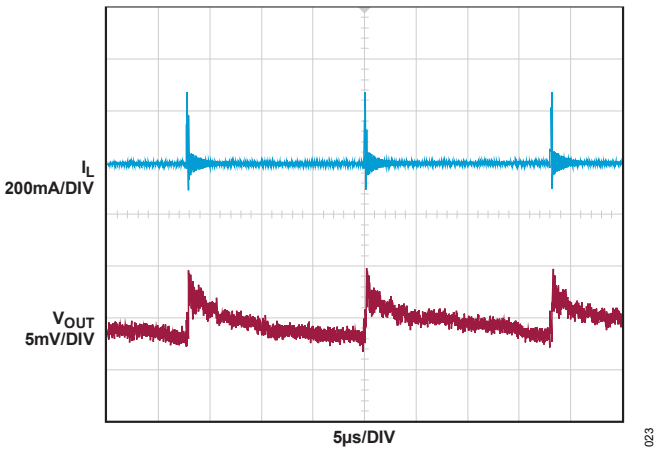


Figure 24. Burst Mode Operation

Programming Input Turn-On and Turn-Off Thresholds With EN/UVLO Pin

The EN/UVLO pin voltage controls whether the ADPL26001 is enabled or is in a shutdown state. A 1.6V reference and a comparator A6 with built-in hysteresis (typical 80mV) allow the user to accurately program the system input voltage at which the IC turns on and off (see *Block Diagram*). The typical input falling and rising threshold voltages can be calculated by the following equations:

$$V_{IN(FALLING,UVLO(-))} = 1.60 \times (R3 + R4)/R4$$

$$V_{IN(RISING,UVLO(+))} = 1.68 \times (R3 + R4)/R4$$

V_{IN} current is reduced below 1µA when the EN/UVLO pin voltage is less than 0.2V. The EN/UVLO pin can be connected directly to the input supply V_{IN} for always-enabled operation. A logic input can also control the EN/UVLO pin.

When operating in Burst Mode operation for light load currents, the current through the R3 and R4 network can easily be greater than the supply current consumed by the ADPL26001. Therefore, R3 and R4 should be large enough to minimize their effect on efficiency at light loads.

$INTV_{CC}$ Regulator

A low dropout (LDO) linear regulator, supplied from V_{IN}, produces a 3V supply at the $INTV_{CC}$ pin. A minimum 1µF low ESR ceramic capacitor must be used to bypass the $INTV_{CC}$ pin to ground to supply the high transient currents required by the internal power MOSFET gate driver.

No additional components or loading is allowed on this pin. The $INTV_{CC}$ rising threshold (to allow soft-start and switching) is typically 2.6V. The $INTV_{CC}$ falling threshold (to stop switching and reset soft-start) is typically 2.5V.

Duty-Cycle Consideration

The ADPL26001 minimum on-time, minimum off-time, and switching frequency (f_{OSC}) define the allowable minimum and maximum duty cycles of the converter (see Minimum On-Time, Minimum Off-Time, and Switching Frequency in *Table 1*) and the following equation:

$$Minimum\ Allowable\ Duty\ Cycle = Minimum\ On\text{-}Time_{(MAX)} \times f_{OSC(MAX)}$$

$$Maximum\ Allowable\ Duty\ Cycle = 1 - Minimum\ Off\text{-}Time_{(MAX)} \times f_{OSC(MAX)}$$

The required switch duty-cycle range for a Boost converter operating in continuous conduction mode (CCM) can be calculated as:

$$D_{MIN} = 1 - V_{IN(MAX)}/(V_{OUT} + V_D)$$

$$D_{MAX} = 1 - V_{IN(MIN)}/(V_{OUT} + V_D)$$

Where V_D is the diode forward voltage drop. If the above duty-cycle calculations for a given application violate the minimum and/or maximum allowed duty cycles for the ADPL26001, operation in discontinuous conduction mode (DCM) might provide a solution. For the same V_{IN} and V_{OUT} levels, operation in DCM does not demand as low a duty cycle as in CCM. DCM also allows higher duty-cycle operation than CCM. The additional advantage of DCM is the removal of the limitations to inductor value and duty cycle required to avoid subharmonic oscillations and the right half plane zero (RHPZ). While DCM provides these benefits, the trade-off is higher inductor peak current, lower available output power and reduced efficiency.

Setting the Output Voltage

The output voltage is programmed with a resistor-divider from the output to the FBX pin. Choose the resistor values for a positive output voltage according to:

$$R1 = R2 \times (V_{OUT}/1.60V - 1)$$

Choose the resistor values for a negative output voltage according to:

$$R1 = R2 \times (|V_{OUT}|/0.80V - 1)$$

The locations of R1 and R2 are shown in the *Block Diagram*. 1% resistors are recommended to maintain output voltage accuracy.

Higher-value FBX divider resistors result in the lowest input quiescent current and highest light-load efficiency. FBX divider resistors R1 and R2 are usually in the range from 25k to 1M. Most applications use a phase-lead capacitor from V_{OUT} to FBX in combination with high-value FBX divider resistors (for more information, see the *Compensation* section).

Soft-Start

The ADPL26001 contains several features to limit peak-switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load.

High peak-switch currents during start-up may occur in switching regulators. Since V_{OUT} is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

The ADPL26001 addresses this mechanism with an internal soft-start function. As shown in the *Block Diagram*, the soft-start function controls the ramp of the power-switch current by controlling the ramp of VC through M2. This allows the output capacitor to be charged gradually toward its final value while limiting the start-up peak currents. *Figure 25* shows the output voltage and supply current for the *Figure 30* circuit. It can be seen that both the output voltage and supply current come up gradually.

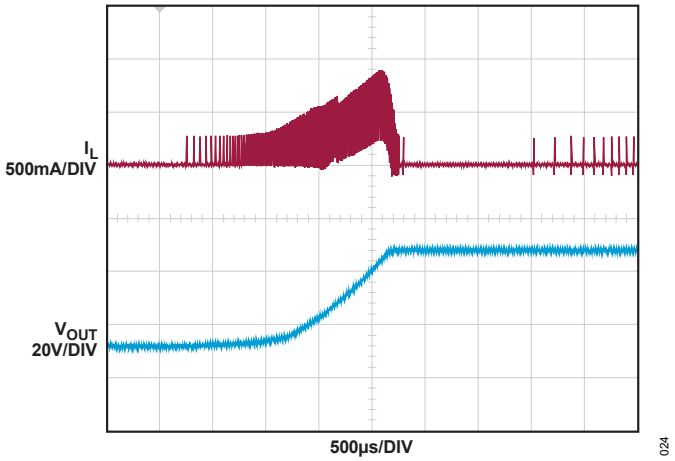


Figure 25. Soft-Start Waveforms

$INTV_{CC}$ undervoltage ($INTV_{CC}$ < 2.5V) and/or thermal lockout (T_J > 170°C) immediately prevent switching, reset the internal soft-start function and pull-down VC. Once all faults are removed, the ADPL26001 soft-starts the VC and hence inductor peak current.

Frequency Foldback

During start-up or fault conditions in which V_{OUT} is very low, extremely small duty cycles may be required to maintain control of inductor peak current. The minimum on-time limitation of the power switch might prevent these low duty cycles from being achievable. In this scenario, inductor current rise exceeds inductor current fall during each cycle, causing inductor current to walk up beyond the switch current-limit. The ADPL26001 provides protection from this by folding back switching frequency whenever FBX pin is close to GND (low V_{OUT} levels). This frequency foldback provides a larger switch-off time, which allows inductor current to fall enough each cycle (for more information, see *Figure 11*).

Thermal Lockout

If the ADPL26001 die temperature reaches 170°C (typical), the part stops switching and go into thermal lockout. When the die temperature drops by 5°C (nominal), the part resumes switching with a soft-started inductor peak current.

Switching Frequency and Inductor Selection

The ADPL26001 switches at 2MHz, which allows small value inductors to be used. A 0.68µH to 10µH usually suffice. Choose an inductor that can handle at least 1.4A without saturating and ensure that the inductor has a low DCR (copper-wire resistance) to minimize I^2R power losses. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one-half of the total switch current. For better efficiency, use similar valued inductors with a larger volume. Many different sizes and shapes are available from various manufacturers. Choose a core material that has low losses at 2MHz, such as a ferrite core. The final value chosen for the inductor should not allow peak inductor currents to exceed 1A in steady state at maximum load. Due to tolerances, be sure to account for minimum possible inductance value, switching frequency, and converter efficiency.

Table 4. Inductor Manufacturers

SUPPLIER	WEBSITE
Sumida	*www.sumida.com*
TDK	*www.tdk.com*
Murata	*www.murata.com*
Coilcraft	*www.coilcraft.com*
Würth	*www.we-online.com*

Input Capacitor

Bypass the input of the ADPL26001 circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and GND pins. Y5V types have poor performance over temperature and applied voltage and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the ADPL26001 and easily handles the ripple current. If the input power source has high impedance or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the ADPL26001. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the ADPL26001 circuit is plugged into a live supply input voltage can ring to twice its nominal value, possibly exceeding the ADPL26001's voltage rating. This situation is easily avoided (for more information, see the Application Note 88*: Ceramic Input Capacitors Can Cause Overvoltage Transients*).

Output Capacitor and Output Ripple

Low ESR capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they are small and have extremely low ESR. Use X5R or X7R types. This choice provides low output ripple and good transient response. A 4.7µF to 15µF output capacitor is sufficient for most applications, but systems with very low output currents may need only a 1µF or 2.2µF output capacitor. Solid tantalum or OS-CON capacitor can be used, but it occupies more board area than a ceramic and have a higher ESR. Always use a capacitor with a sufficient voltage rating.

Compensation

The ADPL26001 is internally compensated. The decision to use either low ESR (ceramic) capacitors or the higher ESR (tantalum or OS-CON) capacitors, for the output capacitor, can affect the stability of the overall system. The ESR of any capacitor, along with the capacitance itself, contributes a zero to the system. For the tantalum and OS-CON capacitors, this zero is located at a lower frequency due to the higher value of the ESR, while the zero of a ceramic capacitor is at a much higher frequency and can generally be ignored.

A phase lead zero can be intentionally introduced by placing a capacitor in parallel with the resistor between V_{OUT} and FBX. By choosing the appropriate values for the resistor and capacitor, the zero frequency can be designed to improve the phase margin of the overall converter. The typical target value for the zero frequency is between 30kHz to 60kHz.

A practical approach to compensation is to start with one of the circuits in this data sheet that is similar to user's application. Optimize performance by adjusting the output capacitor and/or the feed forward capacitor (connected across the feedback resistor from output to FBX pin).

Ceramic Capacitors

Ceramic capacitors are small, robust, and have very low ESR. However, ceramic capacitors can cause problems when used with the ADPL26001 due to their piezoelectric nature. When in Burst Mode operation, the ADPL26001's switching frequency depends on the load current, and at very light loads the ADPL26001 can excite the ceramic capacitor at audio frequencies, which generates audible noise. Since the ADPL26001 operates at a lower current-limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Table 5. Ceramic Capacitor Manufacturers

SUPPLIER	WEBSITE
Taiyo Yuden	*www.ty-top.com*
AVX	*www.kyocera-avx.com*
Murata	*www.murata.com*

Diode Selection

A Schottky diode is recommended for use with the ADPL26001. Low leakage Schottky diodes are necessary when low quiescent current is desired at low loads. The diode leakage appears as an equivalent load at the output and should be minimized. Choose Schottky diodes with sufficient reverse voltage ratings for the target applications.

Table 6. Recommended Schottky Diodes

PART NUMBER	AVERAGE FORWARD CURRENT (mA)	REVERSE VOLTAGE (V)	REVERSE CURRENT (µA)	MANUFACTURER
PMEG6010CEJ	≤1000	≤60	50	NXP
PMEG6030EP	≤3000	≤60	200	NXP

Layout Hints

The high-speed operation of the ADPL26001 demands careful attention to board layout. Careless layout results in performance degradation. *Figure 26* shows the recommended component placement for the ThinSOT and DFN packages. Note the vias under the exposed pad. These should connect to a local ground plane for better thermal performance.

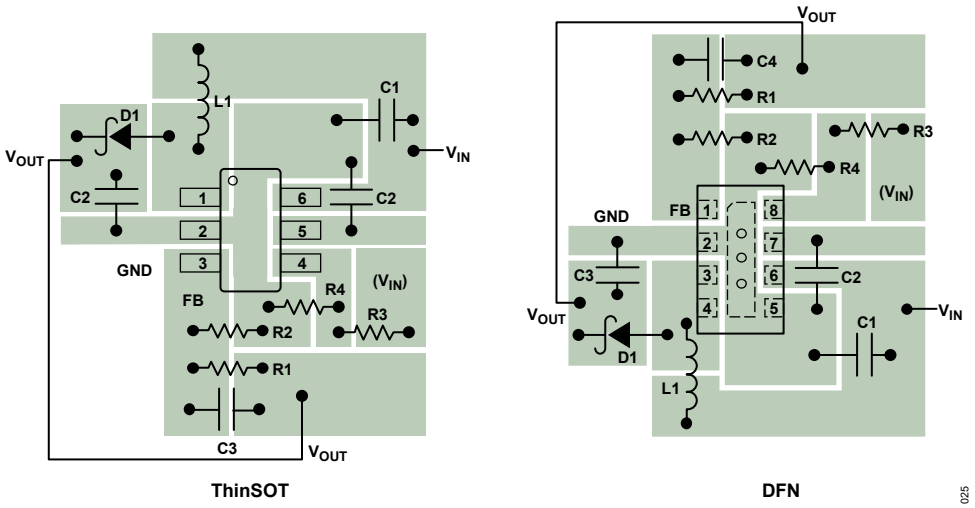


Figure 26. Suggested Layout

Thermal Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the ADPL26001. The DFN package has the best thermal performance due to an exposed pad (Pin 9) on the bottom of the package. This exposed pad must be soldered to a ground plane. Pin 5 of the DFN package (and Pin 2 of the TSOT package) should also be connected to a ground plane. The ground plane should be connected to large copper layers to spread heat dissipated by the ADPL26001 and to further reduce the thermal resistance (θ_{JA}) values listed in the *Pin Configurations and Function Descriptions* section. Power dissipation within the ADPL26001 ($P_{DISS\_ADPL26001}$) can be estimated by subtracting the inductor and Schottky diode power losses from the total power losses calculated in an efficiency measurement. The junction temperature of ADPL26001 can then be estimated by:

$$T_J(ADPL26001) = T_A + \theta_{JA} \times P_{DISS\_ADPL26001}$$

Additional Topologies: SEPIC and Inverting

In addition to the Boost topology, the ADPL26001 can be configured in a SEPIC or Inverting topology. SEPIC and Inverting converters are analyzed below.

SEPIC Converter Applications

The ADPL26001 can be configured as a SEPIC as shown in *Figure 27*. This topology allows for the input to be higher, equal, or lower than the required output voltage. The conversion ratio as a function of duty cycle is (in CCM):

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{D}{1 - D}$$

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}), the input voltage (V_{IN}), and the diode forward voltage (V_D).

The maximum duty cycle (D_{MAX}) occurs when the converter operates at the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_{OUT} + V_D}$$

Conversely, the minimum duty cycle (D_{MIN}) occurs when the converter operates at the maximum input voltage:

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{IN(MAX)} + V_{OUT} + V_D}$$

Be sure to check that D_{MAX} and D_{MIN} obey:

$$D_{MAX} < 1 - Minimum\ Off\text{-}Time_{(MAX)} \times f_{OSC(MAX)}$$

and

$$D_{MIN} > Minimum\ On\text{-}Time_{(MAX)} \times f_{OSC(MAX)}$$

Where Minimum Off-Time, Minimum On-Time, and f_{OSC} are specified in *Table 1*.

SEPIC Converter: The Maximum Output Current Capability and Inductor Selection

As shown in *Figure 27*, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 can be independent, but can also be wound on the same core, since identical voltages are applied to L1 and L2 throughout the switching cycle.

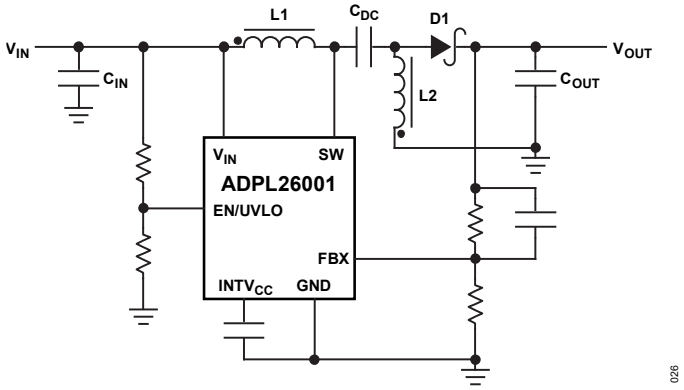


Figure 27. ADPL26001 Configured in a SEPIC Topology

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact that, ideally, the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are:

$$I_{L1(MAX)(AVE)} = I_{IN(MAX)(AVE)} = I_{O(MAX)} \times \frac{D_{MAX}}{1 - D_{MAX}}$$

$$I_{L2(MAX)(AVE)} = I_{O(MAX)}$$

In a SEPIC converter, the switch current is equal to $I_{L1} + I_{L2}$ when the power switch is on, therefore, the maximum average switch current is defined as:

$$I_{SW(MAX)(AVE)} = I_{L1(MAX)(AVE)} + I_{L2(MAX)(AVE)} = I_{O(MAX)} \times \frac{1}{1 - D_{MAX}}$$

and the peak switch current is:

$$I_{SW(PEAK)} = \left(1 + \frac{\chi}{2}\right) \times I_{O(MAX)} \times \frac{1}{1 - D_{MAX}}$$

The constant χ in the preceding equations represents the percentage peak-to-peak ripple current in the switch, relative to $I_{SW(MAX)(AVE)}$, as shown in *Figure 28*. Then, the switch ripple current ΔI_{SW} can be calculated by:

$$\Delta I_{SW} = \chi \times I_{SW(MAX)(AVE)}$$

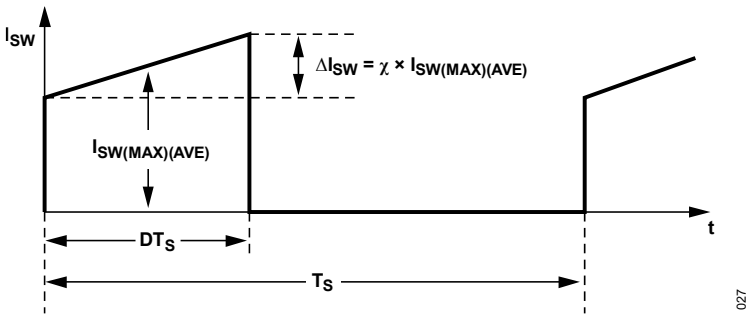


Figure 28. The Switch Current Waveform of the SEPIC Converter

The inductor ripple currents ΔI_{L1} and ΔI_{L2} are identical:

$$\Delta I_{L1} = \Delta I_{L2} = 0.5 \times \Delta I_{SW}$$

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter approaches the voltage mode). Accepting larger values of ΔI_L allows the use of low inductances but results in higher input current ripple and greater core losses. It is recommended that χ falls in the range of 0.2 to 0.6.

Due to the current limit of its internal power switch, the ADPL26001 should be used in a SEPIC converter whose maximum output current ($I_{O(MAX)}$) is less than the output current capability by a sufficient margin (10% or higher is recommended):

$$I_{O(MAX)} < (1 - D_{MAX}) \times (1 - 0.5 \times \Delta I_{SW}) \times (0.9)$$

Given an operating input voltage range, and having chosen ripple current in the inductor, the inductor value (L1 and L2 are independent) of the SEPIC converter can be determined using the following equation:

$$L1 = L2 = \frac{V_{IN(MIN)}}{0.5 \times \Delta I_{SW} \times f_{OSC}} \times D_{MAX}$$

For most SEPIC applications, the equal inductor values fall in the range of 1µH to 47µH.

By making L1 = L2, and winding them on the same core, the value of inductance in the preceding equation is replaced by 2L, due to mutual inductance:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \times f_{OSC}} \times D_{MAX}$$

This maintains the same ripple current and energy storage in the inductors. The peak inductor currents are:

$$I_{L1(PEAK)} = I_{L1(MAX)} + 0.5 \times \Delta I_{L1}$$

$$I_{L2(PEAK)} = I_{L2(MAX)} + 0.5 \times \Delta I_{L2}$$

The maximum RMS inductor currents are approximately equal to the maximum average inductor currents.

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast-switching diode with a low forward drop and low reverse leakage is required. The average forward current in normal operation is equal to the output current.

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than $V_{OUT} + V_{IN(MAX)}$ by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \times V_D$$

Where V_D is diode's forward voltage drop, and the diode junction temperature is:

$$T_J = T_A + P_D \times R_{\theta JA}$$

The $R_{\theta JA}$ used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

SEPIC Converter: Output and Input Capacitor Selection

The selections of the output and input capacitors of the SEPIC converter are similar to those of the boost converter.

SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in *Figure 27*) should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

CDC has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \times \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

Inverting Converter Applications

The ADPL26001 can be configured as a dual-inductor inverting topology as shown in *Figure 29*. The V_{OUT} to V_{IN} ratio is (in CCM):

$$\frac{V_{OUT} - V_D}{V_{IN}} = \frac{-D}{1 - D}$$

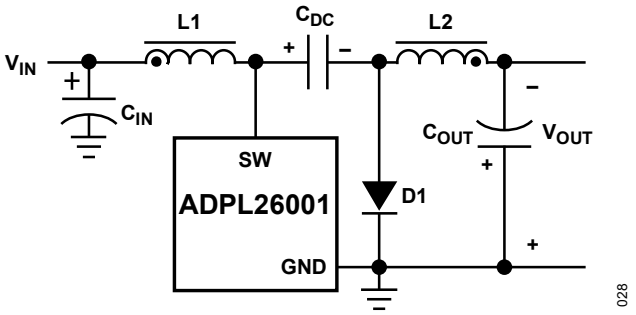


Figure 29. A Simplified Inverting Converter

Inverting Converter: Switch Duty Cycle and Frequency

For an inverting converter operating in CCM, the duty cycle of the main switch can be calculated based on the negative output voltage (V_{OUT}) and the input voltage (V_{IN}).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MIN)}}$$

Conversely, the minimum duty cycle (D_{MIN}) occurs when the converter operates at the maximum input voltage:

$$D_{MIN} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MAX)}}$$

Be sure to check that D_{MAX} and D_{MIN} obey:

$$D_{MAX} < 1 - Minimum\ Off\text{-}Time_{(MAX)} \times f_{OSC(MAX)}$$

and

$$D_{MIN} > Minimum\ On\text{-}Time_{(MAX)} \times f_{OSC(MAX)}$$

Where Minimum Off-Time, Minimum On-Time and f_{OSC} are specified in *Table 1*.

Inverting Converter: Inductor, Output Diode and Input Capacitor Selections

The selections of the inductor, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. See the corresponding SEPIC converter sections.

Inverting Converter: Output Capacitor Selection

The inverting converter requires much smaller output capacitors than those of the boost, flyback, and SEPIC converters for similar output ripples. This is due to the fact that, in the inverting converter, the inductor L2 is in series with the output, and the ripple current flowing through the output capacitors are continuous. The output ripple voltage is produced by the ripple current of L2 flowing through the ESR and bulk capacitance of the output capacitor:

$$\Delta V_{OUT(P-P)} = \Delta I_{L2} \times \left(ESR_{COUT} + \frac{1}{8 \times f \times C_{OUT}} \right)$$

After specifying the maximum output ripple, the user can select the output capacitors according to the preceding equation.

The ESR can be minimized by using high quality X5R or X7R dielectric ceramic capacitors. In many applications, ceramic capacitors are sufficient to limit the output voltage ripple.

The RMS ripple current rating of the output capacitor needs to be greater than:

$$I_{RMS(OUT)} > 0.3 \times \Delta I_{L2}$$

Inverting Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC-coupling capacitor (C_{DC}, as shown in *Figure 29*) should be larger than the maximum input voltage minus the output voltage (negative voltage):

$$V_{CDC} > V_{IN(MAX)} - V_{OUT}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

TYPICAL APPLICATION CIRCUITS

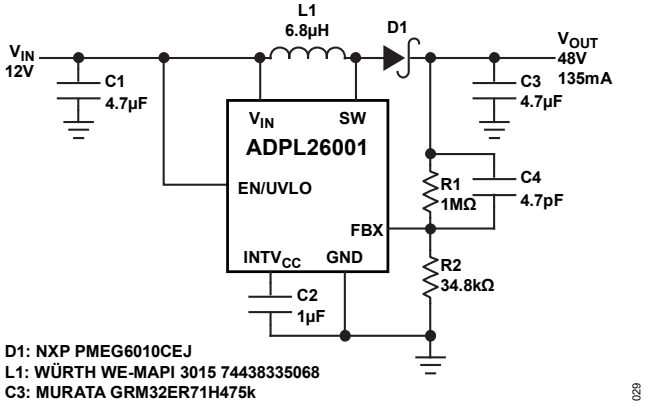


Figure 30. 48V Boost Converter

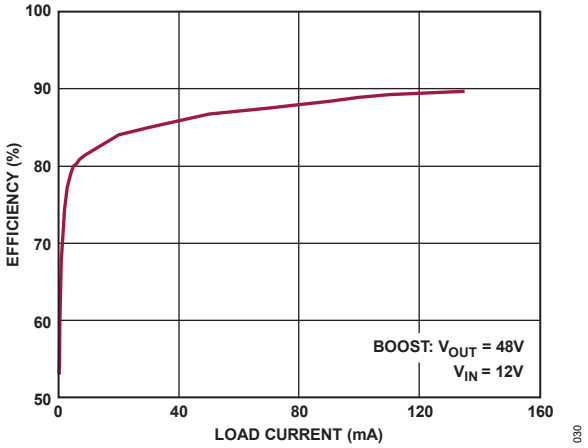


Figure 31. Efficiency vs. Load Current (Figure 30 Circuit)

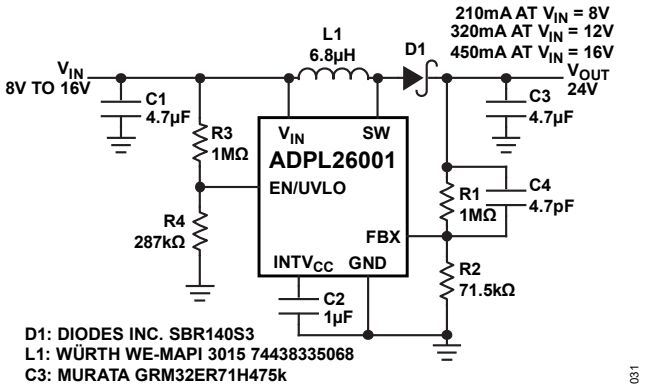


Figure 32. 8V to 16V Input, 24V Boost Converter

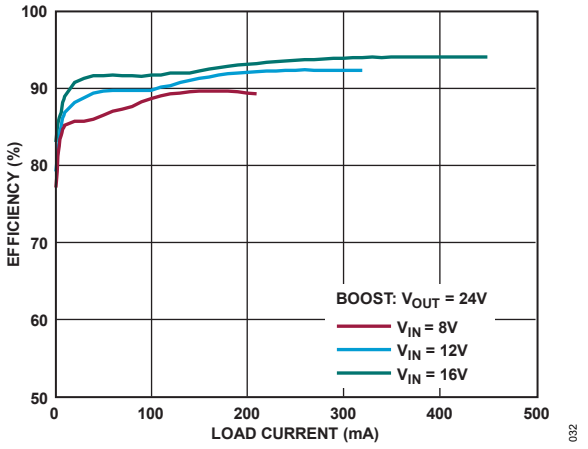


Figure 33. Efficiency vs. Load Current (Figure 32 Circuit)

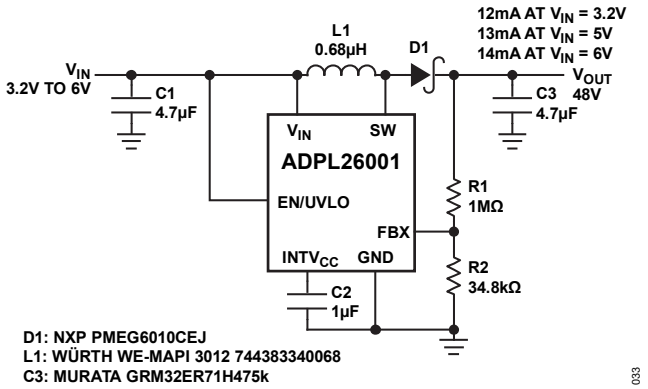


Figure 34. 3.2V to 6V Input, 48V Boost Converter

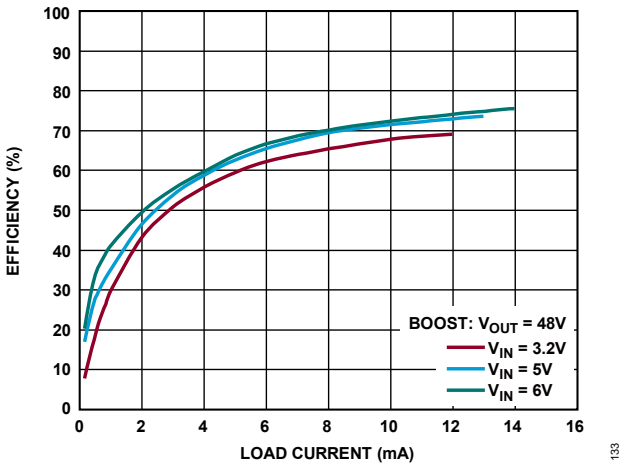


Figure 35. Efficiency vs. Load Current (Figure 34 Circuit)

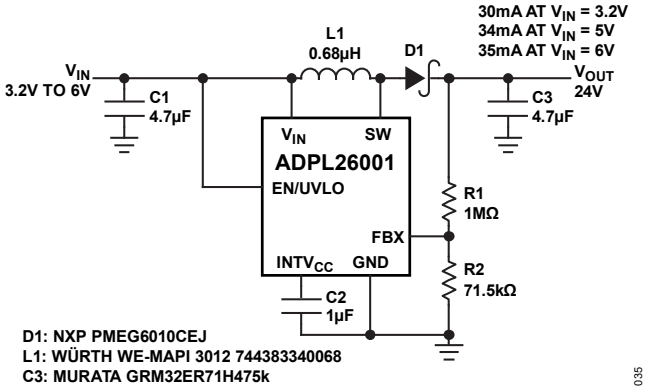


Figure 36. 3.2V to 6V, 24V Boost Converter

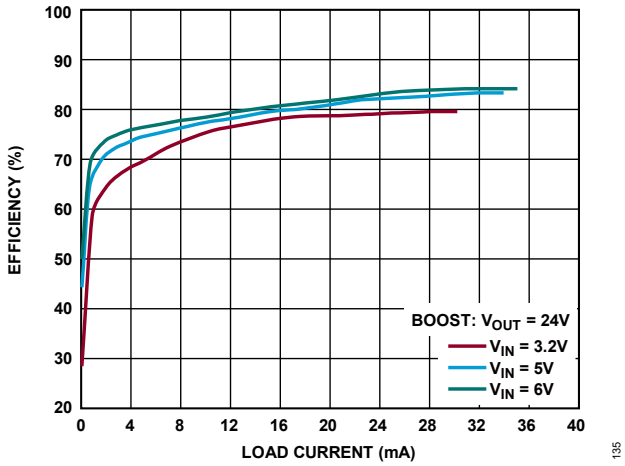


Figure 37. Efficiency vs. Load Current (Figure 36 Circuit)

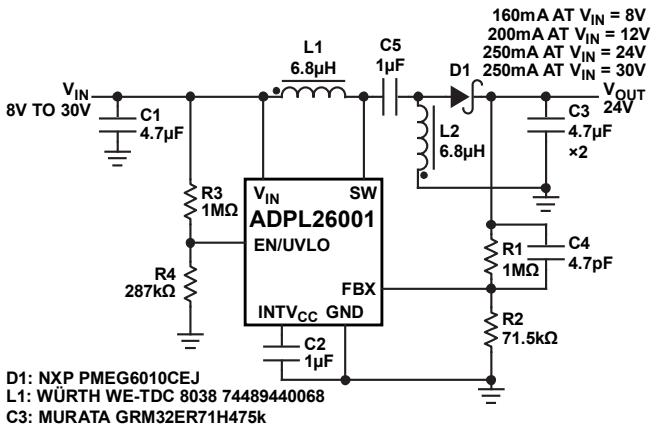


Figure 38. 8V to 30V, 24V SEPIC Converter

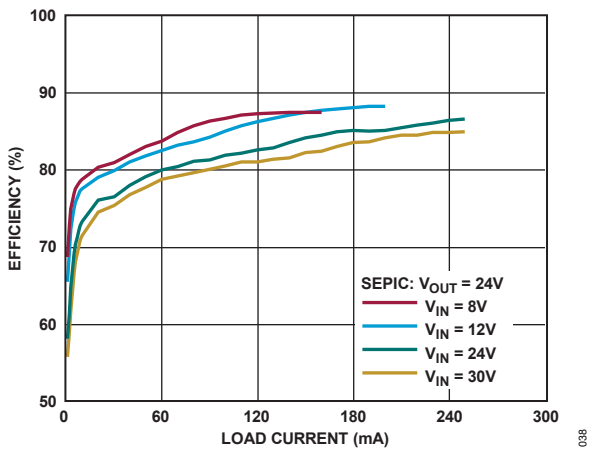


Figure 39. Efficiency vs. Load Current (Figure 38 Circuit)

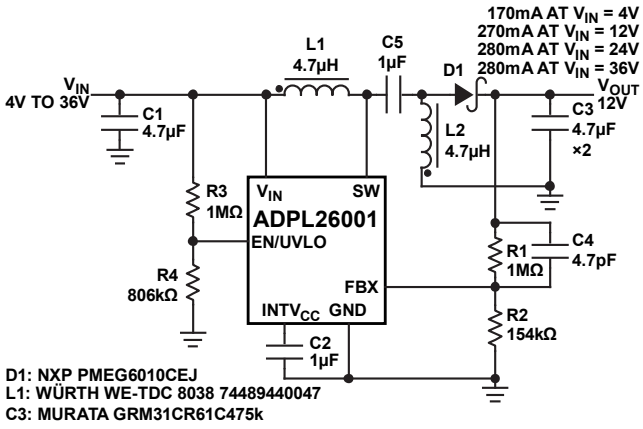


Figure 40. 4V to 36V, 12V SEPIC Converter

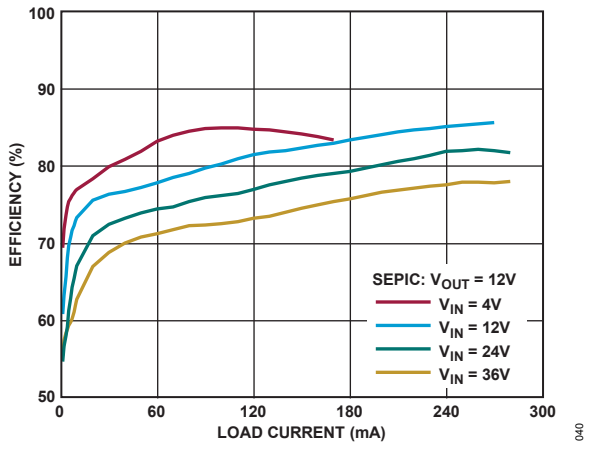


Figure 41. Efficiency vs. Load Current (Figure 40 Circuit)

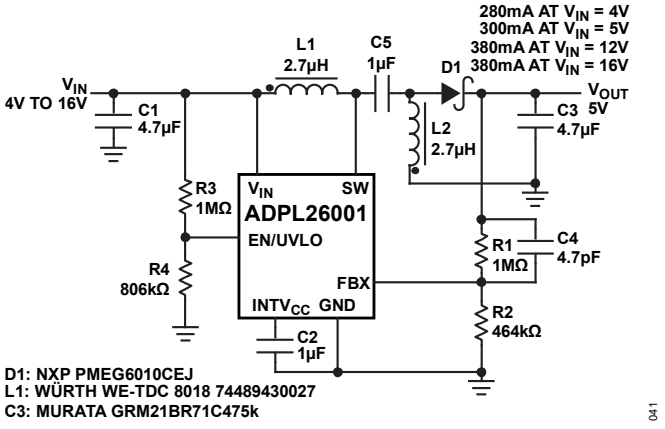


Figure 42. 4V to 16V Input, 5V SEPIC Converter

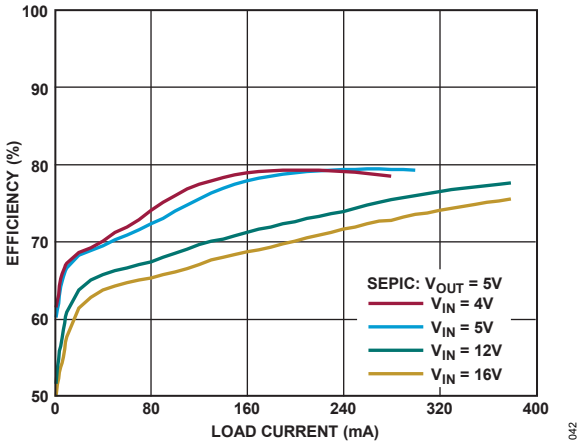


Figure 43. Efficiency vs. Load Current (Figure 42 Circuit)

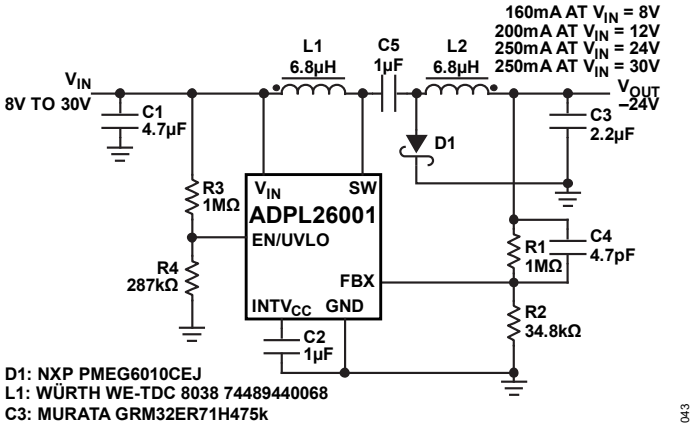


Figure 44. 8V to 30V, –24V Inverting Converter

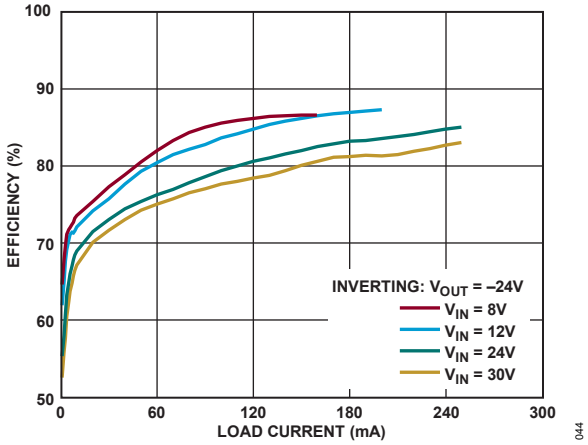


Figure 45. Efficiency vs. Load Current (Figure 44 Circuit)

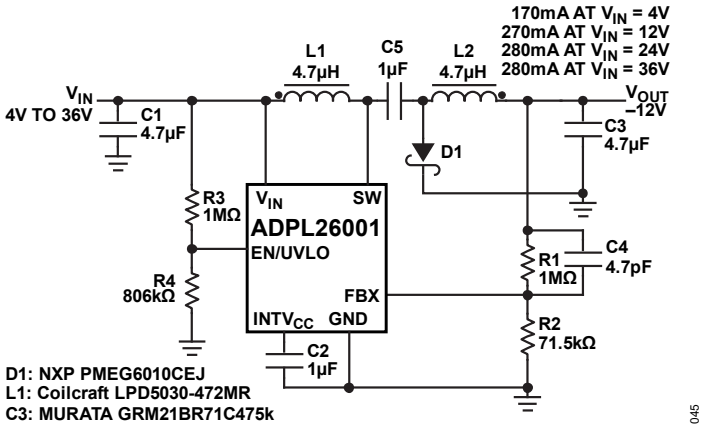


Figure 46. 4V to 36V Input, –12V Inverting Converter

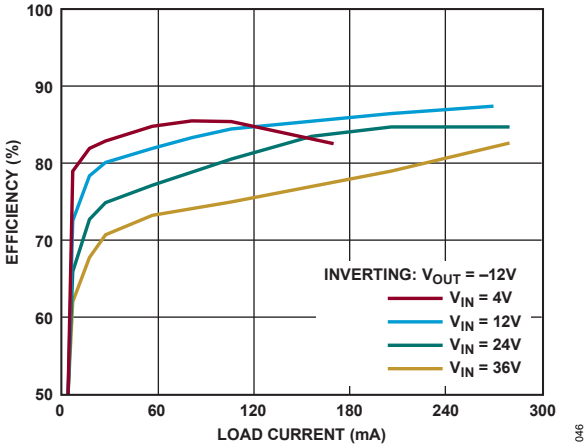


Figure 47. Efficiency vs. Load Current (Figure 46 Circuit)

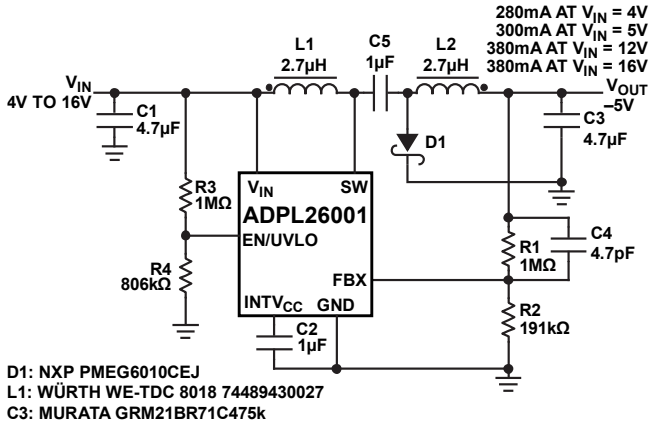


Figure 48. 4V to 16V Input, –5V Inverting Converter

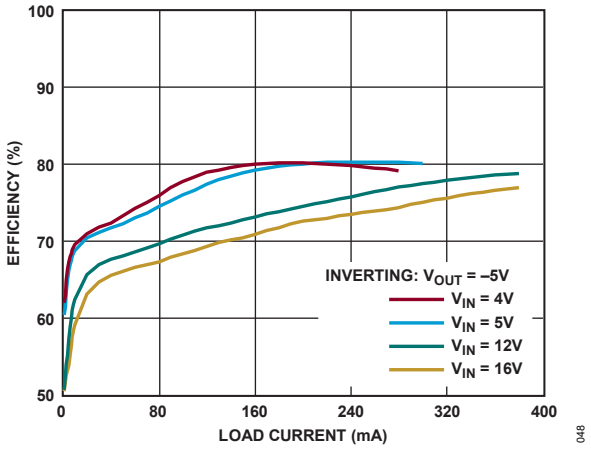


Figure 49. Efficiency vs. Load Current (Figure 48 Circuit)

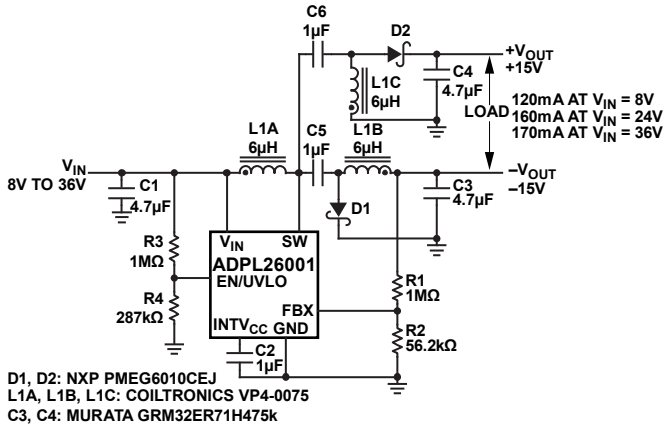


Figure 50. 8V to 40V Input, ±15V Converter

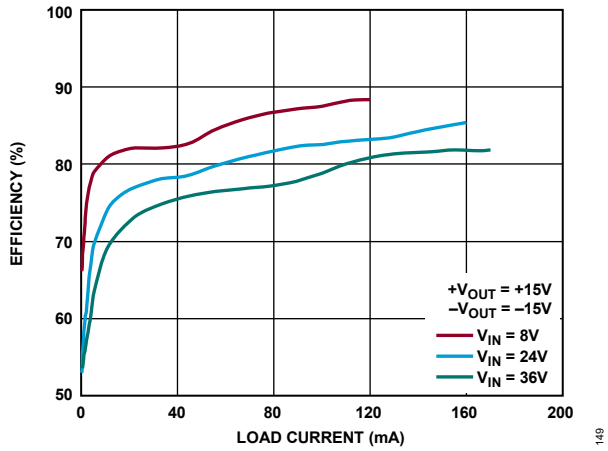
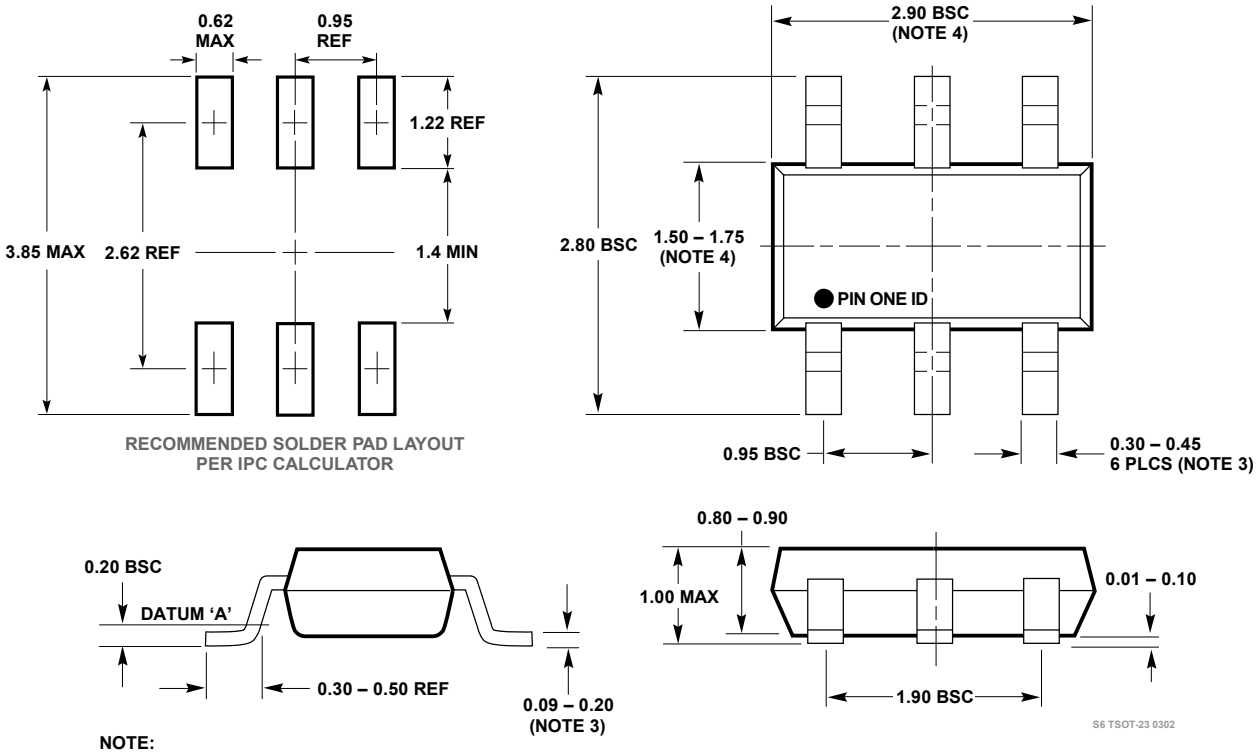


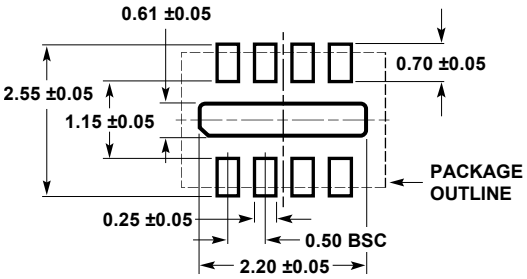
Figure 51. Efficiency vs. Load Current (Figure 50 Circuit)

OUTLINE DIMENSIONS

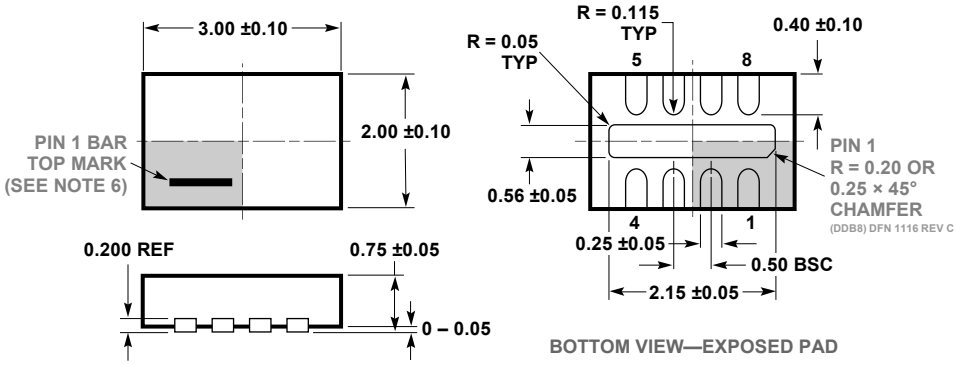


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

Figure 52. 6-Lead Plastic TSOT Package



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 53. 8-Lead Plastic DFN (3mm x 2mm)

ORDERING GUIDE

Table 7. Ordering Guide

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
ADPL26001ES6#TRMPBF	ADPL26001ES6#TRPBF	ADHWM	6-Lead Plastic TSOT-23	–40°C to 125°C
ADPL26001EDDB#TRMPBF	ADPL26001EDDB#TRPBF	LHWX	8-Lead (3mm x 2mm) Plastic DFN	-40°C to 125°C

TRM = 500 pieces.

For more information on tape and reel specifications, refer to the *Tape and reel specifications*.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	12/23	Initial Release	—
1	8/24	Updated Features section	1
		Added DFN Pin Configuration	6
		Updated Pin Descriptions table	6
		Updated Figure 13	8
		Removed phone columns from Table 4 and Table 5	16, 17
		Updated Layout Hints section	17
		Updated Thermal Considerations section	18
		Updated Inverting Converter Applications section	21
		Updated Figure 50	27
		Added Figure 52	29
		Updated Ordering Guide table	30