Data Sheet

ADG2436

0.5 Ω R_{ON}, ±15 V, +12 V, ±5 V, and +5 V/−12 V, Dual SPDT Switch

FEATURES

- Low R_{ON}: 0.5 Ω
- High continuous current of up to 847 mA
- Flat R_{ON} across signal range: 0.003 Ω
- THD of −108 dB at 1 kHz
- Improved balance between on resistance and on capacitance
  - Low R_{ON} (0.5 Ω) and C_{ON} (100 pF)
- 1.8 V, 3.3 V, and 5 V logic compatibility
- 16-lead, 4 mm × 4 mm LFCSP
  - Pin to pin compatible with the ADG1436
- Fully specified at ±15 V, +12 V, ±5 V, and +5 V/−12 V
- Operational with asymmetric power supplies
- V_{SS} to V_{DD} − 2 V analog signal range

APPLICATIONS

- Automatic test equipment
- Data acquisition
- Instrumentation
- Avionics
- Audio and video switching
- Communication systems
- Relay replacement

GENERAL DESCRIPTION

The ADG2436 is an analog multiplexer containing two independently selectable single-pole, double throw (SPDT) switches. An EN input is used to disable all of the switches. For use in multiplexer applications, both switches exhibit break-before-make switching action.

Each channel conducts equally well in both directions when on, and each switch has an input signal range that extends from V_{SS} to V_{DD} − 2 V. When switches are disabled, the signal levels up to the supplies are blocked.

The digital inputs are compatible with 5 V, 3.3 V, and 1.8 V logic inputs without the requirement for a separate digital logic supply pin.

The on-resistance profile is exceptionally flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals.

FUNCTIONAL BLOCK DIAGRAM

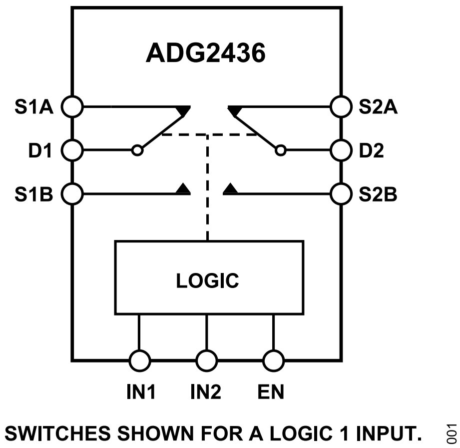

Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

1. Low R_{ON} of 0.5 Ω.
2. High continuous current carrying capability, see Table 5 to Table 6.
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG2436 can be operated from dual supplies up to ±16.5 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG2436 can be operated from a single rail power supply up to 16.5 V.
5. 1.8 V logic-compatible digital inputs: V_{INH} = 1.3 V, V_{INL} = 0.8 V.
6. No V_L logic power supply required.

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

7/2024—Revision 0: Initial Version

SPECIFICATIONS

OPERATING SUPPLY VOLTAGES

Table 1. Operating Supply Voltages

Supply Voltage	Min	Max	Unit
Dual Supply	±4.5	±16.5	V
Single Supply	+5	+16.5	V

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 2. ±15 V Dual-Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +13.5 V, V_{SS} = −13.5 V
Analog Signal Range			V_{DD} − 2 V to V_{SS}	V	
On Resistance (R_{ON})	0.50			Ω typ	Source voltage (V_S) = −13.5 V to +10 V and source current (I_S) = −10 mA (see Figure 31)
	0.65	0.8	0.95	Ω max	
	0.54			Ω typ	V_S = −13.5 V to +11 V and I_S = −100 mA
	0.7	0.85	1.0	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.003			Ω typ	V_S = −13.5 V to +11 V and I_S = −100 mA
	0.085	0.1	0.1	Ω max	
On-Resistance Flatness, ($R_{FLAT\,(ON)}$)	0.003			Ω typ	V_S = −13.5 V to +10 V and I_S = −100 mA
	0.035	0.035	0.035	Ω max	
	0.04			Ω typ	V_S = −13.5 V to +11 V and I_S = −100 mA
	0.08	0.1	0.1	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V and V_{SS} = −16.5 V
Source Off Leakage (I_S (Off))	±1.9			nA typ	V_S = ±10 V and drain voltage (V_D) = ±10 V (see Figure 30)
	±4	+43.4/−5.5	+230/−5.5	nA max	
Drain Off Leakage (I_D (Off))	±4			nA typ	V_S = ±10 V and V_D = ±10 V (see Figure 30)
	±8	+85.2/−11	+454/−11	nA max	
Channel On Leakage (I_D (On)) and (I_S (On))	±1.7			nA typ	V_S = V_D = ±10 V (see Figure 29)
	±5.3	+45.2/−8.5	+257/−8.5	nA max	
DIGITAL INPUTS					
Input High Voltage (V_{INH})			1.3	V min	
Input Low Voltage (V_{INL})			0.8	V max	
Input Current (I_{INL} or I_{INH})	0.01			µA typ	Input voltage (V_{IN}) = GND voltage (V_{GND}) or V_{DD}
			±0.15	µA max	
Digital Input Capacitance (C_{IN})	4.6			pF typ	
DYNAMIC CHARACTERISTICS					
Transition Time ($t_{TRANSITION}$)	313			ns typ	Load resistance (R_L) = 300 Ω and load capacitance (C_L) = 35 pF
	381	419	459	ns max	V_S = 10 V (see Figure 39)
On Time ($t_{ON\,(EN)}$)	306			ns typ	Load resistance (R_L) = 300 Ω and load capacitance (C_L) = 35 pF
	363	401	439	ns max	V_S = 10 V (see Figure 38)
Off Time ($t_{OFF\,(EN)}$)	211			ns typ	R_L = 300 Ω and C_L = 35 pF

SPECIFICATIONS

Table 2. ±15 V Dual-Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
	245	250	253	ns max	V_S = 10 V (see Figure 38)
Break-Before-Make Time Delay (t_D)	182			ns typ	R_L = 300 Ω and C_L = 35 pF
	139	169	201	ns min	V_S = 10 V (see Figure 37)
Charge Injection (Q_{INJ})	−1.68			nC typ	V_S = 0 V, R_S = 0 Ω, and C_L = 1 nF (see Figure 40)
Off Isolation	−76			dB typ	R_L = 50 Ω, C_L = 5 pF, and frequency = 100 kHz (see Figure 33)
Channel-to-Channel Crosstalk	−82			dB typ	R_L = 50 Ω, C_L = 5 pF, and frequency = 100 kHz (see Figure 32)
Total Harmonic Distortion + Noise (THD + N)	0.008			% typ	R_L = 1 kΩ, 20 V p-p, and frequency = 20 Hz to 20 kHz (see Figure 34)
Total Harmonic Distortion (THD)	−108			dB typ	R_L = 1 kΩ, 20 V p-p, and frequency = 1 kHz
	−82			dB typ	R_L = 1 kΩ, 20 V p-p, and frequency = 20 kHz
	−69			dB typ	R_L = 1 kΩ, 20 V p-p, and frequency = 100 kHz
−3 dB Bandwidth	77			MHz typ	R_L = 50 Ω, C_L = 5 pF, and signal = 0 dBm (see Figure 35)
Insertion Loss	−0.07			dB typ	R_L = 50 Ω, C_L = 5 pF, and frequency = 1 MHz (see Figure 35)
Source Off Capacitance (C_S (Off))	74			pF typ	V_S = 0 V and frequency = 1 MHz
Drain Off Capacitance (C_D (Off))	148			pF typ	V_S = 0 V and frequency = 1 MHz
Drain On Capacitance (C_D (On)) and Source On Capacitance (C_S (On))	100			pF typ	V_S = 0 V and frequency = 1 MHz
Match On Capacitance (C_{MATCH}(On))	0.3			pF typ	V_S = 0 V and frequency = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V and V_{SS} = −16.5 V
Power Supply Current (I_{DD})	170			µA typ	Digital inputs = 0 V or 5 V
	260		260	µA max	
	225			µA typ	Digital inputs = 1.3 V
	330		330	µA max	
Negative Supply Current (I_{SS})	85			µA typ	Digital inputs = 0 V or 5 V
	140		140	µA max	

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, and GND = 0 V, unless otherwise noted.

Table 3. 12 V Single-Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8 V and V_{SS} = 0 V
Analog Signal Range			0 V to V_{DD} − 2 V	V	
On Resistance (R_{ON})	0.50			Ω typ	Source voltage (V_S) = 0 V to 7.3 V and source current (I_S) = −100 mA (see Figure 31)
	0.65	0.8	0.95	Ω max	
	0.54			Ω typ	V_S = 0 V to 8.3 V and I_S = −100 mA
	0.7	0.85	1.0	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.003			Ω typ	V_S = 0 V to 8.3 V and I_S = −100 mA
	0.085	0.1	0.1	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.003			Ω typ	V_S = 0 V to 7.3 V and I_S = −100 mA

SPECIFICATIONS

Table 3. 12 V Single-Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
	0.035	0.035	0.035	Ω max	
	0.04			Ω typ	V_S = 0 V to 8.3 V and I_S = −100 mA
	0.08	0.1	0.1	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V and V_{SS} = 0 V
Source Off Leakage (I_S (Off))	±1.9			nA typ	V_S = 1 V/10 V and drain voltage (V_D) = 10 V/1 V (see Figure 30)
	±4	+43.4/−5.5	+230/−5.5	nA max	
Drain Off Leakage (I_D (Off))	±4			nA typ	V_S = 1 V/10 V and V_D = 10 V/1 V (see Figure 30)
	±8	+85.2/−11	+454/−11	nA max	
Channel On Leakage (I_D (On)) and (I_S (On))	±1.7			nA typ	V_S = V_D = 1 V/10 V (see Figure 29)
	±5.3	+45.2/−8.5	+257/−8.5	nA max	
DIGITAL INPUTS					
Input High Voltage (V_{INH})			1.3	V min	
Input Low Voltage, (V_{INL})			0.8	V max	
Input Current (I_{INL}) or (I_{INH})	0.01			µA typ	Input voltage (V_{IN}) = GND voltage (V_{GND}) or V_{DD}
			±0.15	µA max	
Digital Input Capacitance (C_{IN})	4.6			pF typ	
DYNAMIC CHARACTERISTICS					
Transition Time ($t_{TRANSITION}$)	382			ns typ	Load resistance (R_L) = 300 Ω and load capacitance (C_L) = 35 pF
	460	471	475	ns max	V_S = 8 V (see Figure 39)
On Time ($t_{ON\ (EN)}$)	190			ns typ	Load resistance (R_L) = 300 Ω and load capacitance (C_L) = 35 pF
	224	239	253	ns max	V_S = 8 V (see Figure 38)
Off Time ($t_{OFF\ (EN)}$)	367			ns typ	R_L = 300 Ω and C_L = 35 pF
	427	438	449	ns max	V_S = 8 V (see Figure 38)
Break-Before-Make Time Delay (t_D)	59			ns typ	R_L = 300 Ω and C_L = 35 pF
	42	57	68	ns min	V_S = 10 V (see Figure 37)
Charge Injection (Q_{INJ})	−1			nC typ	V_S = 6 V, R_S = 0 Ω, and C_L = 1 nF (see Figure 40)
Off Isolation	−61			dB typ	R_L = 50 Ω, C_L = 5 pF, and frequency = 100 kHz (see Figure 33)
Channel-to-Channel Crosstalk	−65			dB typ	R_L = 50 Ω, C_L = 5 pF, and frequency = 100 kHz (see Figure 32)
Total Harmonic Distortion + Noise (THD + N)	0.008			% typ	R_L = 1 kΩ, 6 V p-p, and frequency = 20 Hz to 20 kHz (see Figure 34)
Total Harmonic Distortion (THD)	−113			dB typ	R_L = 1 kΩ, 6 V p-p, and frequency = 1 kHz
	−89			dB typ	R_L = 1 kΩ, 6 V p-p, and frequency = 20 kHz
	−75			dB typ	R_L = 1 kΩ, 6 V p-p, and frequency = 100 kHz
−3 dB Bandwidth	60			MHz typ	R_L = 50 Ω, C_L = 5 pF, and signal = 0 dBm (see Figure 35)
Insertion Loss	−0.08			dB typ	R_L = 50 Ω, C_L = 5 pF, and frequency = 1 MHz (see Figure 35)
Source Off Capacitance (C_S (Off))	69			pF typ	V_S = 6 V and frequency = 1 MHz

SPECIFICATIONS

Table 3. 12 V Single-Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Drain Off Capacitance (C_D (Off))	190			pF typ	V_S = 6 V and frequency = 1 MHz
Drain On Capacitance (C_D (On)) and Source On Capacitance (C_S (On))	131			pF typ	V_S = 6 V and frequency = 1 MHz
Match On Capacitance (C_{MATCH} (On))	0.4			pF typ	V_S = 6 V and frequency = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
Power Supply Current (I_{DD})	170			µA typ	Digital inputs = 0 V or 5 V
	260		260	µA max	
	225			µA typ	Digital inputs = 1.3 V
	330		330	µA max	
Negative Supply Current (I_{SS})	85			µA typ	Digital inputs = 0 V or 5 V
	140		140	µA max	

DUAL AND ASYMMETRIC SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V to −12 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 4. Dual and Asymmetric Supply Specifications

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +4.5 V and V_{SS} = −13.2 V
Analog Signal Range			V_{DD} – 2 V to V_{SS}	V	
On Resistance (R_{ON})	0.50			Ω typ	Source voltage (V_S) = V_{SS} to +1 V and source current (I_S) = −100 mA (see Figure 31)
	0.65	0.8	0.95	Ω max	
	0.54			Ω typ	V_S = V_{SS} to +2 V and I_S = −100 mA
	0.70	0.85	1.0	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.003			Ω typ	V_S = V_{SS} to +2 V and I_S = −100 mA
	0.085	0.1	0.1	Ω max	
On-Resistance Flatness ($R_{FLAT\ (ON)}$)	0.003			Ω typ	V_S = V_{SS} to +1 V and I_S = −100 mA
	0.035	0.035	0.035	Ω max	
	0.04			Ω typ	V_S = V_{SS} to +2 V and I_S = −100 mA
	0.08	0.1	0.1	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V and V_{SS} = −13.2 V
Source Off Leakage (I_S (Off))	±1.9			nA typ	V_S = +1 V or −10 V and V_D = −10 V or +1 V (see Figure 30)
	±4	+43.4/−5.5	+230/−5.5	nA max	
Drain Off Leakage (I_D (Off))	±4			nA typ	V_S = +1 V or −10 V and V_D = −10 V or +1 V (see Figure 30)
	±8	+85.2/−11	+454/−11	nA max	
Channel On Leakage (I_D (On)) and (I_S (On))	±1.7			nA typ	V_S = V_D = +3 V or −10 V (see Figure 29)
	±5.3	+45.2/−8.5	+257/−8.5	nA max	
DIGITAL INPUTS					
Input High Voltage (V_{INH})			1.3	V min	
Input Low Voltage (V_{INL})			0.8	V max	
Input Current (I_{INL}) or (I_{INH})	0.01			µA typ	Input voltage (V_{IN}) = GND voltage (V_{GND}) or V_{DD}
			±0.15	µA max	
Digital Input Capacitance (C_{IN})	4.6			pF typ	
DYNAMIC CHARACTERISTICS					V_{DD} = +5 V and V_{SS} = −12 V

SPECIFICATIONS

Table 4. Dual and Asymmetric Supply Specifications (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Transition Time ($t_{TRANSITION}$)	282				Load resistance (R_L) = 300 Ω and load capacitance (C_L) = 35 pF
	332	365	393		V_S = 1.5 V (see Figure 39)
On Time ($t_{ON\ (EN)}$)	312			ns typ	Load resistance (R_L) = 300 Ω and load capacitance (C_L) = 35 pF
	368	415	451	ns max	V_S = 1.5 V (see Figure 38)
Off Time ($t_{OFF\ (EN)}$)	264			ns typ	R_L = 300 Ω and C_L = 35 pF
	310	317	323	ns max	V_S = 1.5 V (see Figure 38)
Break-Before-Make Time Delay (t_D)	191			ns typ	R_L = 300 Ω and C_L = 35 pF
	154	186	216	ns min	V_S = 1.5 V (see Figure 37)
Charge Injection (Q_{INJ})	−1.25			nC typ	V_S = −3 V, R_S = 0 Ω, and C_L = 1 nF (see Figure 40)
Off Isolation	−74			dB typ	R_L = 50 Ω, C_L = 5 pF, and frequency = 100 kHz (see Figure 33)
Channel-to-Channel Crosstalk	−76			dB typ	R_L = 50 Ω, C_L = 5 pF, and frequency = 100 kHz (see Figure 32)
Total Harmonic Distortion + Noise (THD + N)	0.004			% typ	R_L = 1 kΩ, 3 V p-p, and frequency = 20 Hz to 20 kHz (see Figure 34)
Total Harmonic Distortion (THD)	−124			dB typ	R_L = 1 kΩ, 3 V p-p, and frequency = 1 kHz
	−102			dB typ	R_L = 1 kΩ, 3 V p-p, and frequency = 20 kHz
	−89			dB typ	R_L = 1 kΩ, 3 V p-p, and frequency = 100 kHz
−3 dB Bandwidth	58			MHz typ	R_L = 50 Ω, C_L = 5 pF, and signal = 0 dBm (see Figure 35)
Insertion Loss	−0.08			dB typ	R_L = 50 Ω, C_L = 5 pF, and frequency = 1 MHz (see Figure 35)
Source Off Capacitance (C_S (Off))	101			pF typ	V_S = 0 V and frequency = 1 MHz
Drain Off Capacitance (C_D (Off))	200			pF typ	V_S = 0 V and frequency = 1 MHz
Drain On Capacitance (C_D (On)) and Source On Capacitance (C_S (On))	117			pF typ	V_S = 0 V and frequency = 1 MHz
Match On Capacitance (C_{MATCH}(On))	0.49			pF typ	V_S = 0 V and frequency = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V and V_{SS} = −13.2 V
Power Supply Current (I_{DD})	170			µA typ	Digital inputs = 0 V or 5 V
	260		260	µA max	
	225			µA typ	Digital inputs = 1.3 V
	330		330	µA max	
Negative Supply Current (I_{SS})	85			µA typ	Digital inputs = 0 V or 5 V
	140		140	µA max	

SPECIFICATIONS

CONTINUOUS CURRENT PER CHANNEL, SX OR DX

Table 5. One Channel On, Per Channel Specifications

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx					
V_{DD} = +15 V and V_{SS} = −15 V					
LFCSP (θ_{JA} = 44°C/W)	847	325	123	mA maximum	V_S = V_{SS} to V_{DD} − 3.5 V
V_{DD} = 12 V and V_{SS} = 0 V					
LFCSP (θ_{JA} = 44°C/W)	847	325	123	mA maximum	V_S = V_{SS} to V_{DD} − 3.5 V
V_{DD} = +5 V and V_{SS} = −5 V					
LFCSP (θ_{JA} = 44°C/W)	847	325	123	mA maximum	V_S = V_{SS} to V_{DD} − 3.5 V
V_{DD} = +5 V and V_{SS} = −12 V					
LFCSP (θ_{JA} = 44°C/W)	847	325	123	mA maximum	V_S = V_{SS} to V_{DD} − 3.5 V

Table 6. Two Channels On, Per Channel Specifications

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx					
V_{DD} = +15 V and V_{SS} = −15 V					
LFCSP (θ_{JA} = 44°C/W)	646	289	120	mA maximum	V_S = V_{SS} to V_{DD} − 3.5 V
V_{DD} = 12 V and V_{SS} = 0 V					
LFCSP (θ_{JA} = 44°C/W)	646	289	120	mA maximum	V_S = V_{SS} to V_{DD} − 3.5 V
V_{DD} = +5 V and V_{SS} = −5 V					
LFCSP (θ_{JA} = 44°C/W)	646	289	120	mA maximum	V_S = V_{SS} to V_{DD} − 3.5 V
V_{DD} = +5 V and V_{SS} = −12 V					
LFCSP (θ_{JA} = 44°C/W)	646	289	120	mA maximum	V_S = V_{SS} to V_{DD} − 3.5 V

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to +6 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx pins[2]	2.6 A (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx pins[2]	Data (see Table 5 and Table 6) + 15%
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb-Free	As per JEDEC J-STD-020

[1] Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

[2] Sx refers to the S1A, S1B, S2A, and S2B pins, and Dx refers to the D1 and D2 pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JCB} is the junction to the bottom of the case value.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JCB}	Unit
CP-16-17[1]	44	17.4	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADG2436

Table 9. ADG2436, 16-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

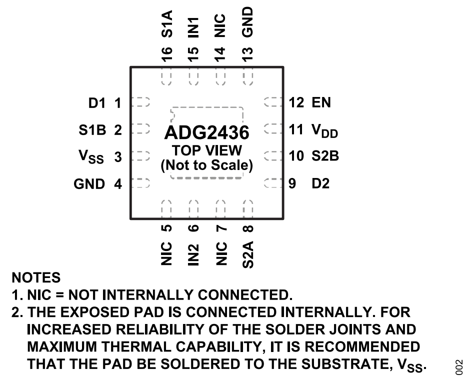

Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	D1	Drain Terminal 1. The D1 pin can be an input or output.
2	S1B	Source Terminal 1B. The S1B pin can be an input or output.
3	V_{SS}	Most Negative Power Supply Voltage.
4, 13	GND	Ground (0 V) Reference.
5, 7, 14	NIC	Not Internally Connected.
6	IN2	Logic Control Input 2.
8	S2A	Source Terminal 2A. The S2A pin can be an input or output.
9	D2	Drain Terminal 2. The D2 pin can be an input or output.
10	S2B	Source Terminal 2B. The S2B pin can be an input or output.
11	V_{DD}	Most Positive Power Supply.
12	EN	Active High Digital Input. When the EN pin is low, the device is disabled, and all switches are off. When the EN pin is high, INx logic inputs determine the on switches.
15	IN1	Logic Control Input 1.
16	S1A	Source Terminal 1A. The S1A pin can be an input or output.
	EP	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 11. ADG2436 Truth Table

EN	INx	SxA	SxB
0	X[1]	Off	Off
1	0	Off	On
1	1	On	Off

[1] X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

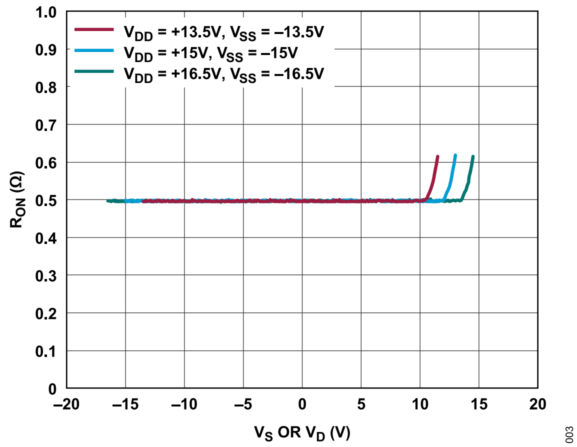

Figure 3. R_{ON} as a Function of V_S, V_D, ±15 V Dual Supply

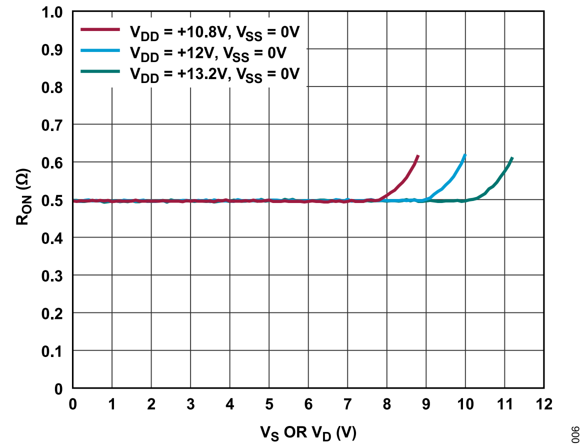

Figure 6. R_{ON} as a Function of V_S, V_D, 12 V Single Supply

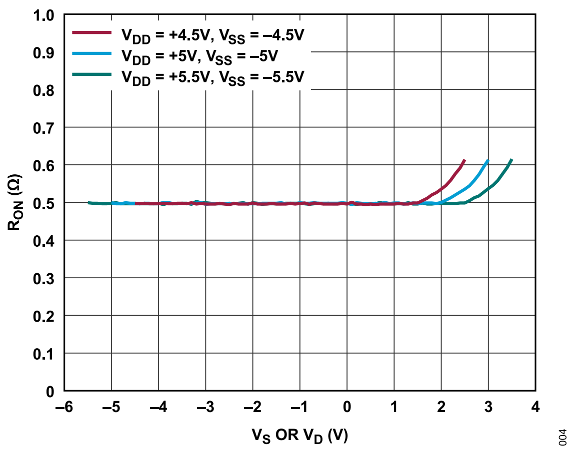

Figure 4. R_{ON} as a Function of V_S, V_D, ±5 V Dual Supply

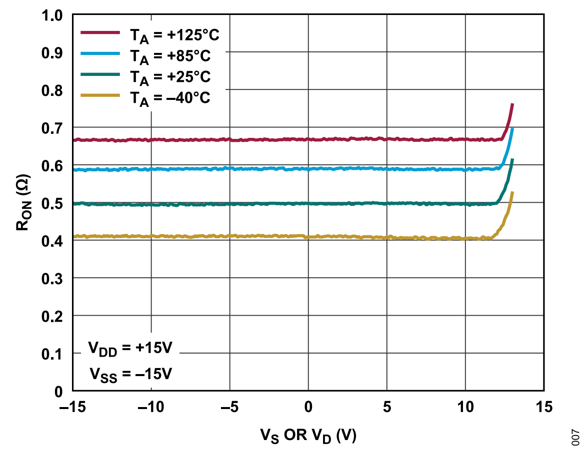

Figure 7. R_{ON} as a Function of V_S (V_D) for Different Temperatures, ±15 V Dual Supply

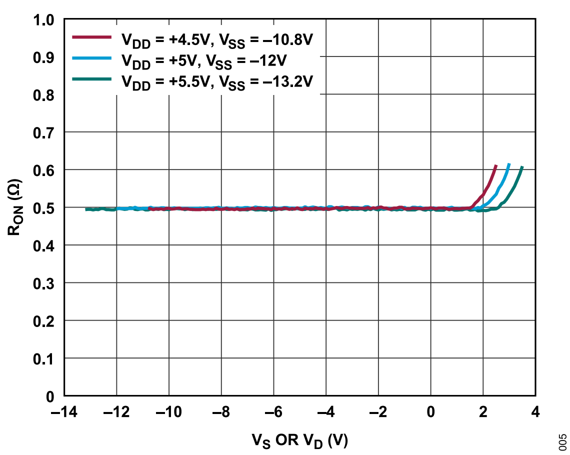

Figure 5. R_{ON} as a Function of V_S, V_D, +5 V, −12 V Dual Supply

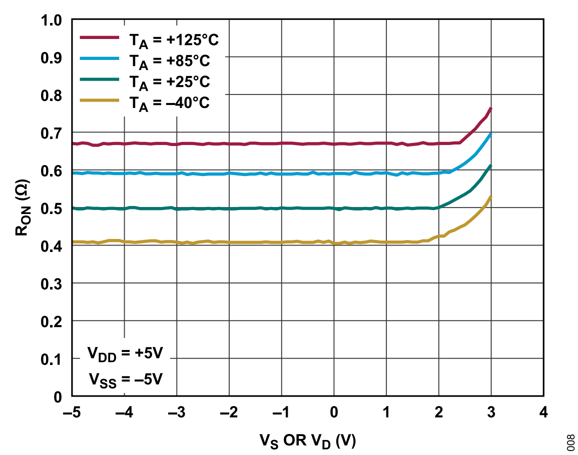

Figure 8. R_{ON} as a Function of V_S (V_D) for Different Temperatures, ±5 V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

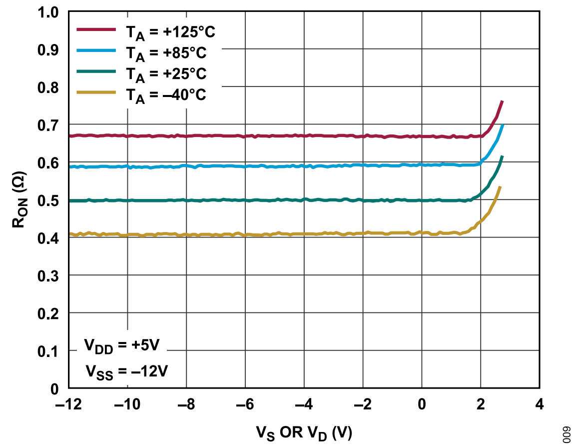

Figure 9. R_{ON} as a Function of V_S (V_D) for Different Temperatures, +5 V, −12 V Dual Supply

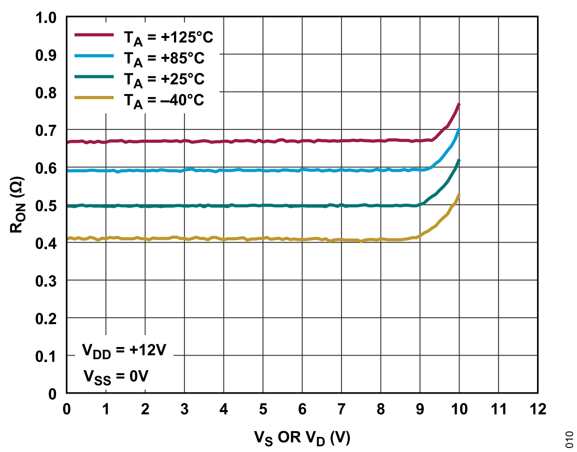

Figure 10. R_{ON} as a Function of V_S (V_D) for Different Temperatures, +12 V Single Supply

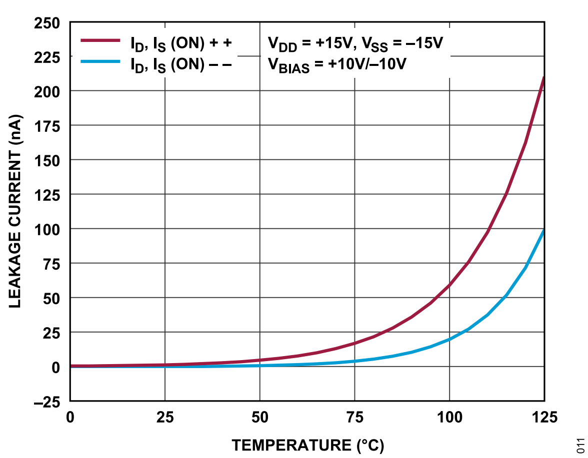

Figure 11. On Leakage Currents vs. Temperature, ±15 V Dual Supply

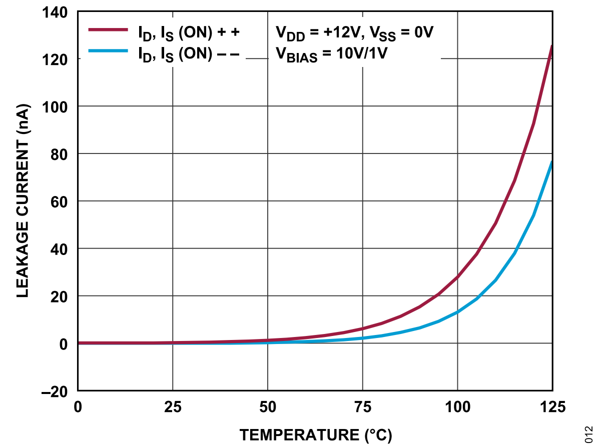

Figure 12. On Leakage Currents vs. Temperature, +12 V Single Supply

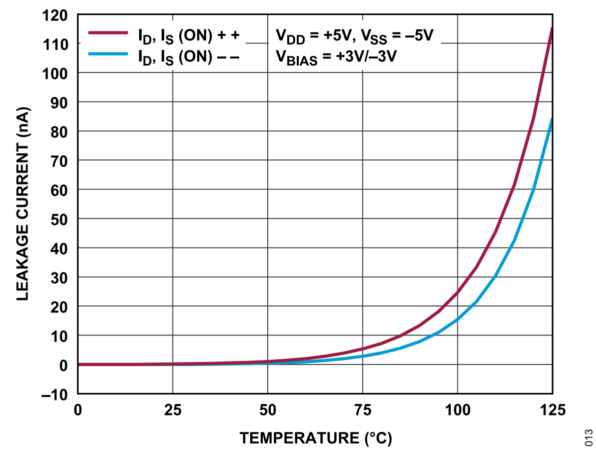

Figure 13. On Leakage Currents vs. Temperature, ±5 V Dual Supply

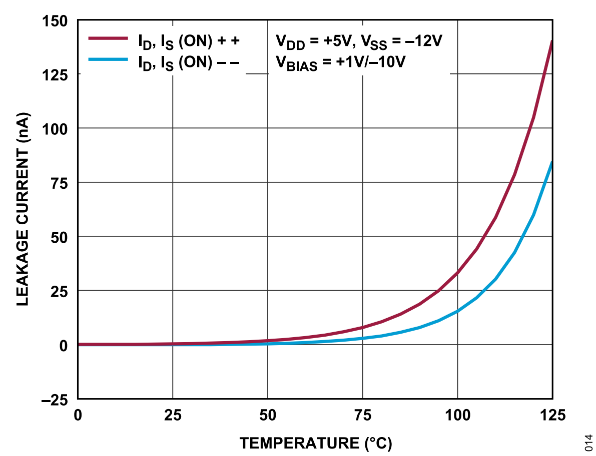

Figure 14. On Leakage Currents vs. Temperature, +5 V, −12 V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

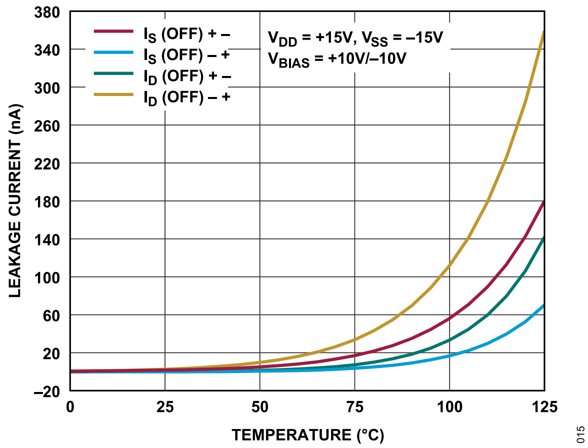

Figure 15. Off Leakage Currents vs. Temperature, ±15 V Dual Supply

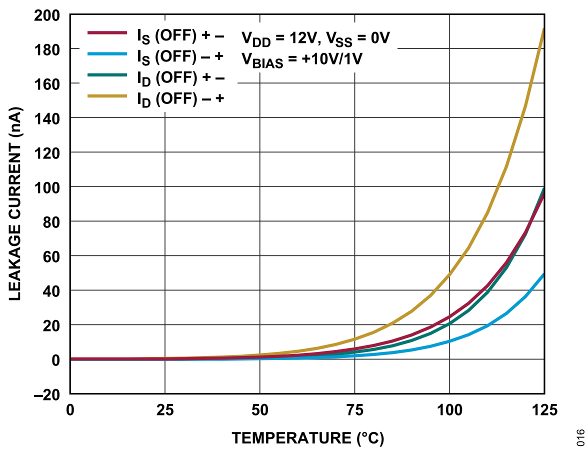

Figure 16. Off Leakage Currents vs. Temperature, +12 V Single Supply

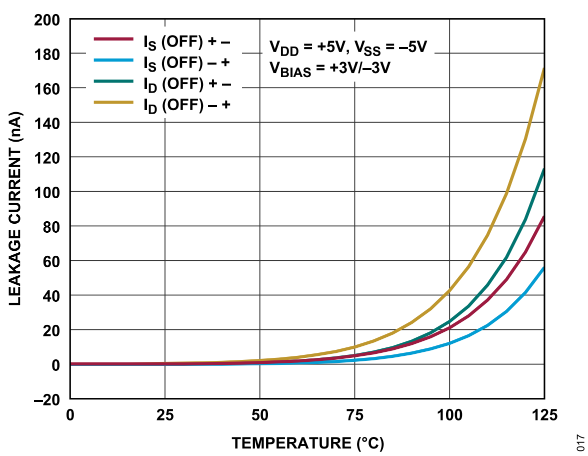

Figure 17. Off Leakage Currents vs. Temperature, ±5 V Dual Supply

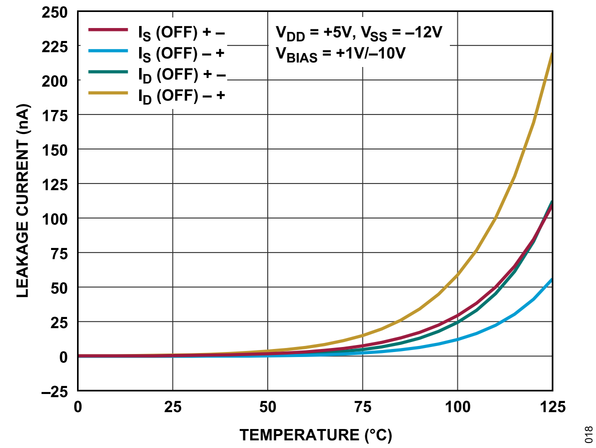

Figure 18. Off Leakage Currents vs. Temperature, +5 V, −12 V Dual Supply

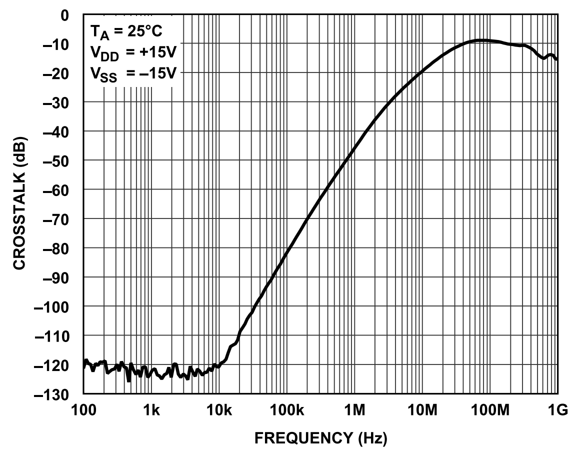

Figure 19. Crosstalk vs. Frequency, ±15 V Dual Supply

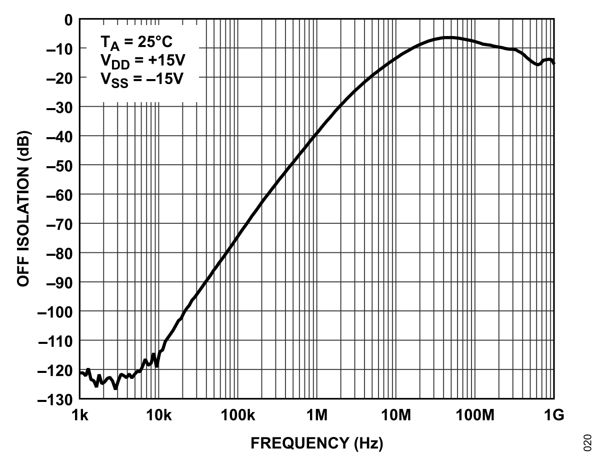

Figure 20. Off Isolation vs. Frequency, ±15 V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

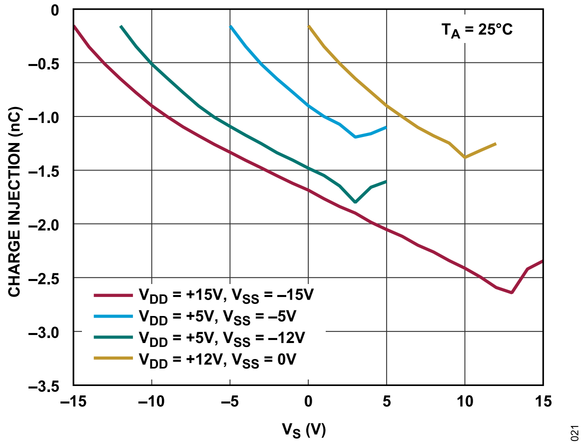

Figure 21. Charge Injection vs. V_S

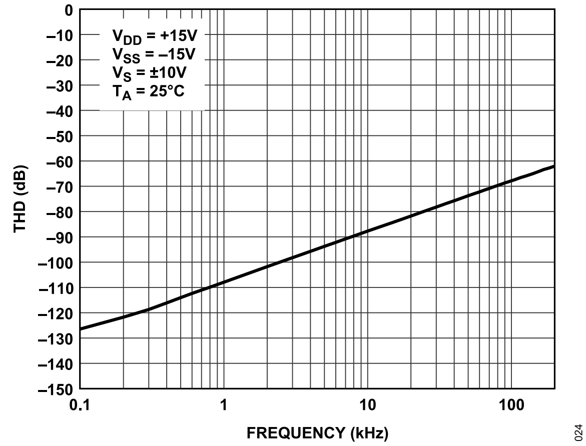

Figure 24. THD vs. Frequency, ±15 V Dual Supply

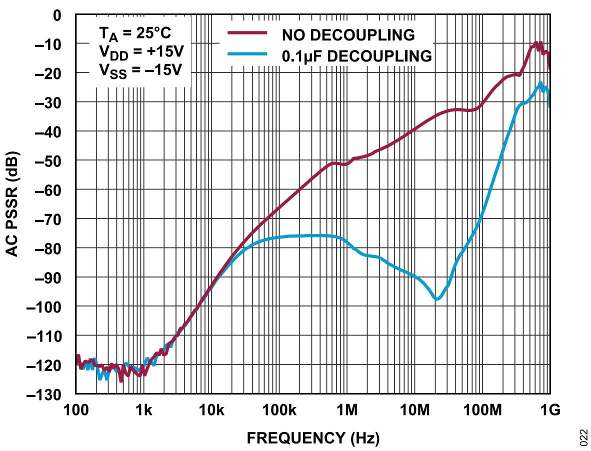

Figure 22. AC Power Supply Rejection Ratio (PSRR) vs. Frequency, ±15 V Dual Supply

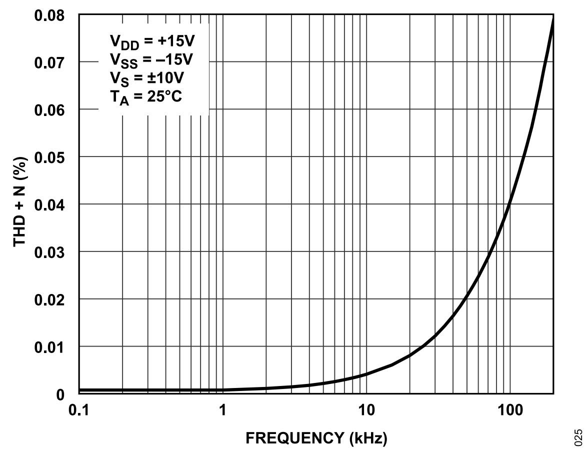

Figure 25. THD + N vs. Frequency, ±15 V Dual Supply

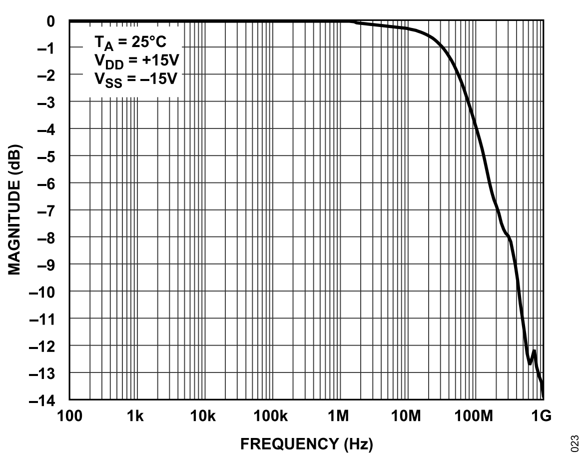

Figure 23. Insertion Loss vs. Frequency

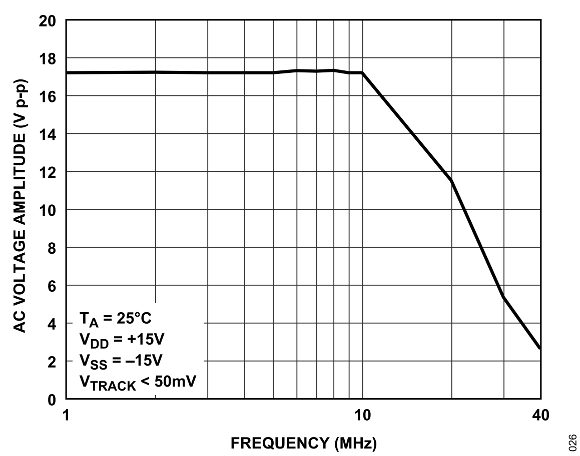

Figure 26. Large AC Signal Voltage vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

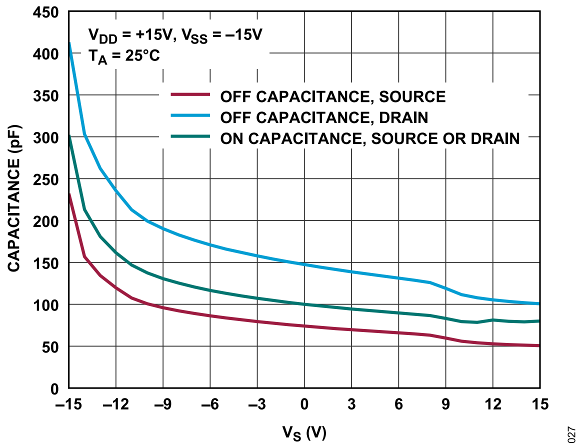

Figure 27. Capacitance vs. V_S, ±15 V Dual Supply

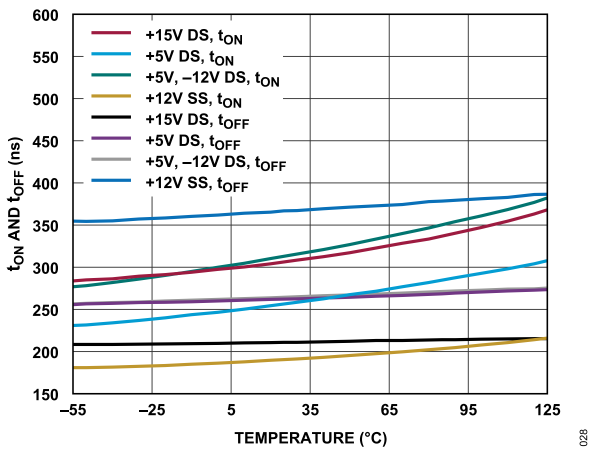

Figure 28. t_{ON} and t_{OFF} Times vs. Temperature

TEST CIRCUITS

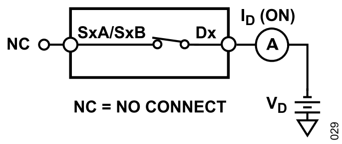

Figure 29. On Leakage

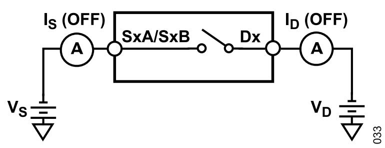

Figure 30. Off Leakage

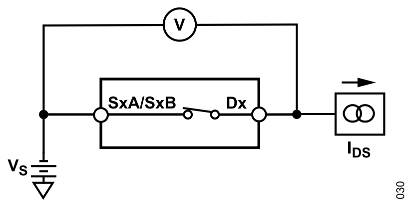

Figure 31. On Resistance

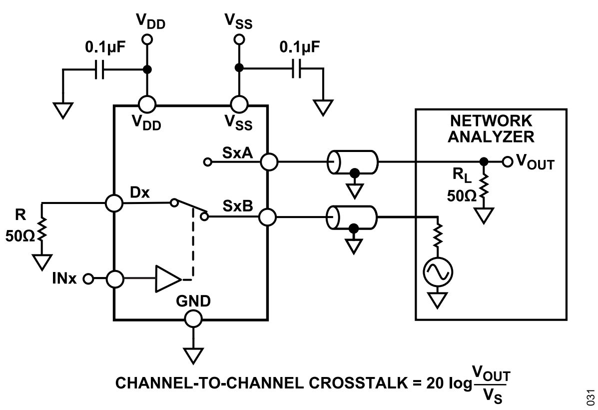

Figure 32. Channel-to-Channel Crosstalk

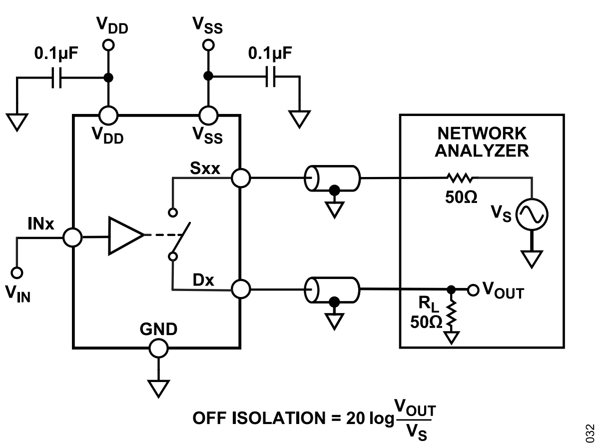

Figure 33. Off Isolation

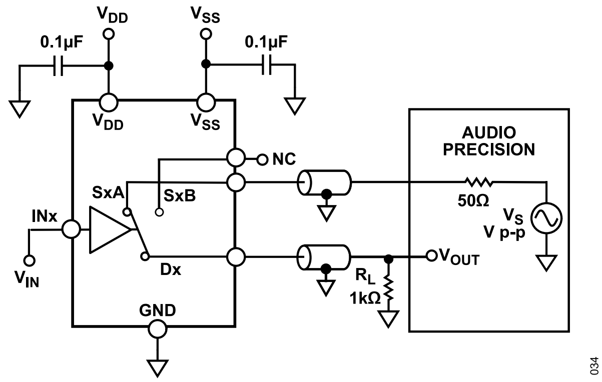

Figure 34. THD + Noise

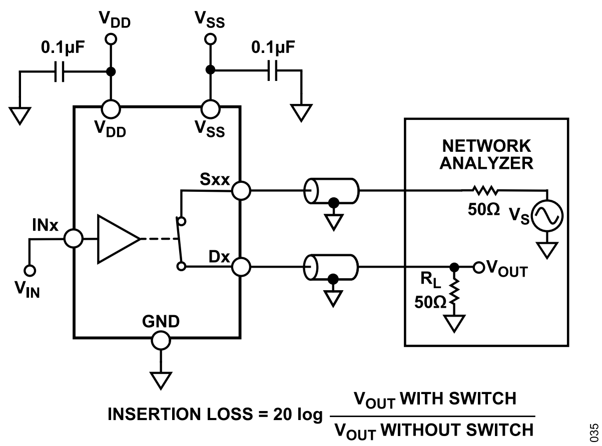

Figure 35. Bandwidth

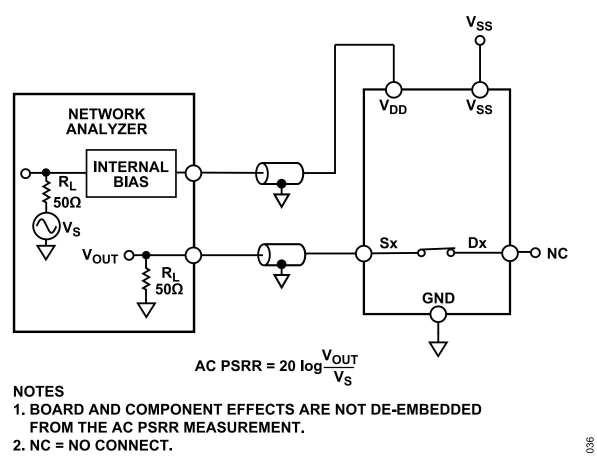

Figure 36. AC PSRR

TEST CIRCUITS

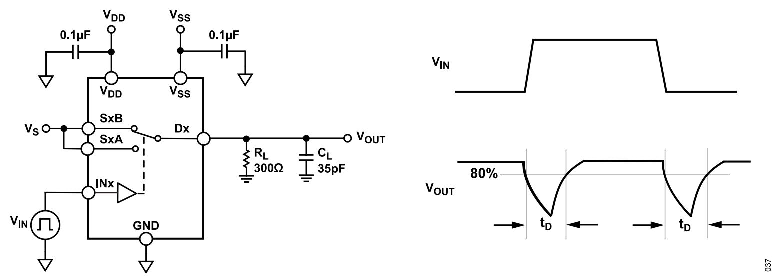

Figure 37. Break-Before-Make Time Delay, t_D

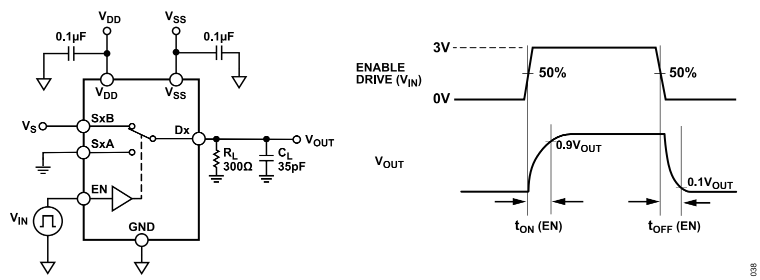

Figure 38. Enable Delay, t_{ON} (EN) and t_{OFF} (EN)

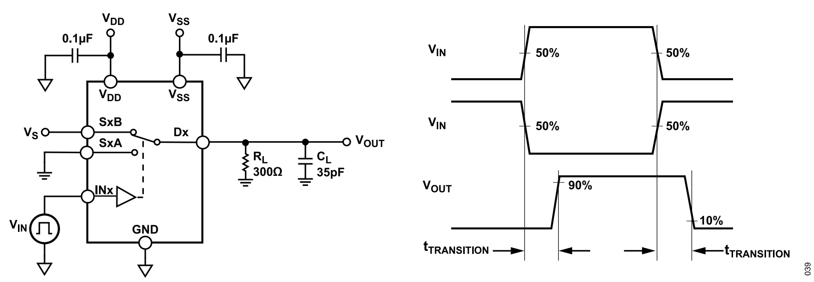

Figure 39. Switching Times

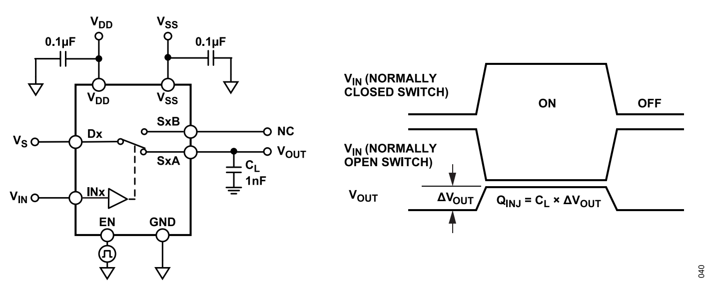

Figure 40. Charge Injection

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D and V_S

The analog voltage on Terminal D and Terminal S, respectively.

V_{TRACK}

The difference between V_S and V_D.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

The difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D (On) and I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL} and I_{INH}

The input current of the digital input when high or when low.

C_S (Off) and C_D (Off)

The off switch source and drain capacitance for the off condition, which is measured with reference to ground.

C_D (On) and C_S (On)

The on switch drain and source capacitance for the on condition, which is measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{ON}

The delay between applying the digital control input and the output switching on.

t_{OFF}

The delay between applying the digital control input and the output switching off.

t_D

The off-time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Channel-to-Channel Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)

The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The DC voltage on the device is modulated by a sine wave of 0.62 V p-p.

THEORY OF OPERATIONS

SWITCH ARCHITECTURE

The ADG2436 contains two independent SPDT, N-channel diffused metal-oxide semiconductor (NDMOS) switches that allow for excellent R_{ON} performance. Using an NDMOS only architecture results in a reduction of signal headroom, meaning the signals are limited to V_{DD} − 2 V. To achieve the lowest on resistance, on-resistance flatness, and total harmonic distortion, it is recommended the signal stays less than V_{DD} − 3.5 V.

To guarantee correct operation of the ADG2436, a minimum of 0.1 µF decoupling capacitors are required on both the V_{DD} and V_{SS} supply pins.

The ADG2436 is compatible with single-supply systems that have a V_{DD} of up to 16.5 V, dual-supply systems of up to ±16.5 V, as well as asymmetric power supplies.

1.8 V LOGIC COMPATIBILITY

For ease of use, the ADG2436 does not have a logic reference voltage (V_L). The digital inputs are compatible with 1.8 V logic levels over the full operating supply range. The limits for 1.8 V logic are as follows: V_{INH} = 1.3 V and V_{INL} = 0.8 V. The 1.8 V logic-level inputs enable the ADG2436 to be compatible with processors that have lower supply rails, eliminating the need for an external translator.

If full 1.8 V and 1.2 V JEDEC compliance is required, refer to the Analog Devices, Inc., L-range part numbers, such as the ADG1412L.

APPLICATIONS INFORMATION

LARGE VOLTAGE, HIGH FREQUENCY SIGNAL TRACKING

Figure 26 shows the voltage range and corresponding frequencies that the ADG2436 can reliably convey. The tracking voltage (V_{TRACK}) in the figure shows the source voltage and the drain voltage difference, which is less than 50 mV for a given amplitude and frequency. For large voltage, high frequency signals, the frequency must be kept below 10 MHz. If the required frequency is greater than 10 MHz, decrease the signal range appropriately to ensure signal integrity.

POWER SUPPLY RECOMMENDATIONS

Analog Devices has a wide range of power management products to meet the requirements of high performance signal chains.

An example of a bipolar solution is shown in Figure 41. The LT3463 (a dual switching regulator), generates a positive and negative supply rail for the ADG2436, an amplifier, and/or a precision converter in a typical signal chain. Also, two optional low-dropout regulators (LDOs), the ADP7142 and the ADP7182 (positive and negative LDOs, respectively) are shown in Figure 41, which can reduce the output ripple of the LT3463 in ultra-low noise sensitive applications.

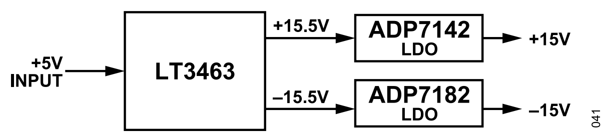

Figure 41. Bipolar Power Solution

Table 12. Recommended Power Management Devices

Product	Description
LT3463	Dual micropower, DC to DC converter with Schottky diodes
ADP7142	40 V, 200 mA, low noise, CMOS, LDO linear regulator
ADP7182	−28 V, −200 mA, low noise, LDO linear regulator

DATA ACQUISITION CALIBRATION

Figure 42 shows an example application for the ADG2436. In automated test equipment (ATE) and instrumentation applications, when using data acquisition (DAQ) systems, there is a requirement for precision and accuracy. Many factors such as drift over time and temperature may cause the system to lose this accuracy. The low on-resistance and charge injection of the ADG2436 is ideally suited to calibrate this system in real time before taking a measurement, thus, reducing error. The break-before-make feature of the ADG2436 allows the system to switch the calibration path without shorting the inputs together.

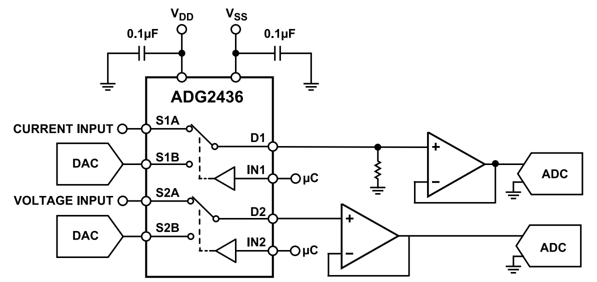

Figure 42. DAQ Calibration Application

OUTLINE DIMENSIONS

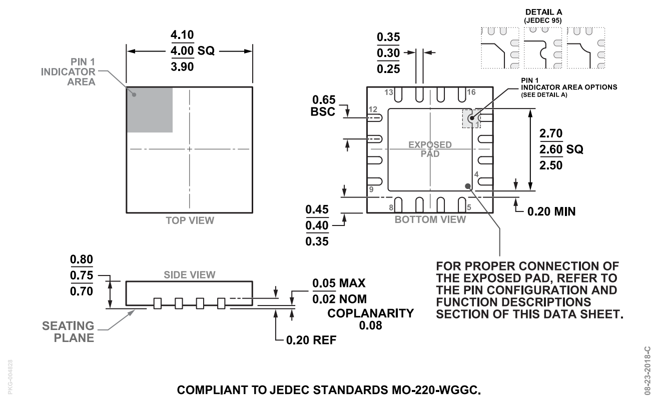

Figure 43. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADG2436BCPZ-REEL7	−40°C to +125°C	16-Lead LFCSP (4 mm × 4 mm)	Reel, 1500	CP-16-17

1 Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 13. Evaluation Boards

Model[1]	Description
EVAL-ADG2436EBZ	Evaluation Board

1 Z = RoHS-Compliant Part.