2ED1322S12M/2ED1321S12M

1200 V half-bridge gate driver with integrated bootstrap diode and OCP

Features

- Unique Infineon Thin-Film-Silicon On Insulator (SOI)-technology
  - Floating channel designed for bootstrap operation
- Maximum bootstrap voltage (VB node) of + 1225 V
- Operating voltages (VS node) upto + 1200 V
- Negative VS transient voltage immunity of 100 V
  - With repetive 700 ns pulses
- 2.3 A / 4.6 A peak output source / sink current capability
- Integrated ultra-fast over-current protection (OCP)
  - ± 5% high accuracy reference threshold
  - Less than 1 us over-current sens to output shutdown
- Integrated ultra-fast, low resistance bootstrap diode
- Integrated dead-time and shoot-through prevention logic(2ED1322S12M)
- Enable, Fault, and programmable Fault clear RFE input
- Logic operational up to –8 V on VS Pin
- Independent per channel undervoltage lockout (UVLO)
- 25 V VCC supply voltage (maximum)
- Separate Logic (VSS) and output ground (COM)
- Greater than 5 mm clearance / creepage
- 2 kV HBM ESD capability

Product summary

V_{S_OFFSET} = 1200 V (maximum)
I_{o+} / I_{o-} = 2.3 A / 4.6 A (peak)
V_{CC} = 13 V to 20 V (typical)
Propagation delay = 500 ns typ.
Dead-time = 380 ns typ.

Package

PG-DSO-16-U02 (300 mil)

Typical applications

- Industrial Drives
- Embedded inverters for Motor Control in Pumps, Fans
- Commercial and Lite Commercial Air Conditioning

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC78/20/22

Ordering information

Sales Product Name	Package type	Standard pack		Orderable part number
		Form	Quantity	
2ED1322S12M	PG-DSO-16-U02	Tape and Reel	1,000	2ED1322S12MXUMA1
2ED1321S12M	PG-DSO-16-U02	Tape and Reel	1,000	2ED1321S12MXUMA1

Description

The 2ED132x family contains devices, which control IGBT or SiC MOSFET power devices with a maximum blocking voltage of +1200 V in half bridge configurations. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, the design is very robust against parasitic latch up across the operating temperature and voltage range.
The two independent driver outputs are controlled at the low-side using two different CMOS resp. LSTTL compatible signals, down up to 3.3V logic. The device includes an under-voltage detection unit with hysteresis characteristic.
The 2ED132x has symmetric undervoltage lockout levels, which support strongly the integrated ultrafast bootstrap diode. Additionally, the offline gate clamping function provides an inherent protection of the transistors for parasitic turn-on by floating gate conditions, when the IC is not supplied via VCC.

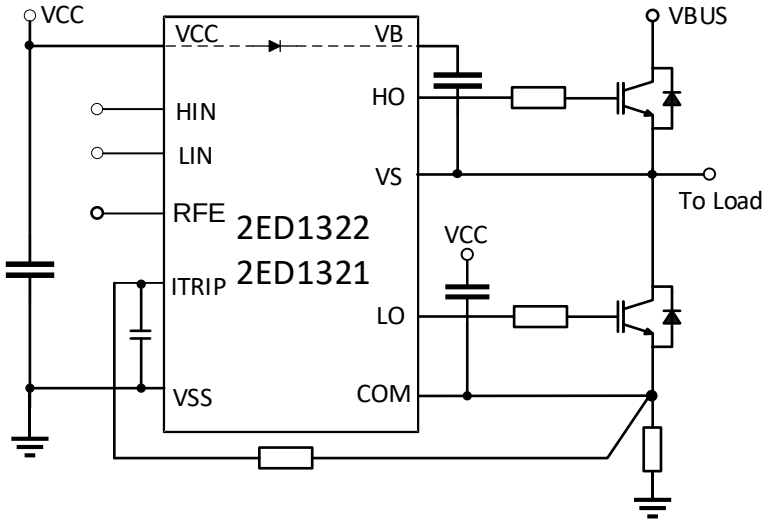

Figure 1 Typical application block diagram

Summary of feature comparison of the 2ED132x family:

Table 1

Sales Product Name	Package Type	Source / sink drive (peak - A)	Key Features	Cross conduction prevention	Integrated Deadtime	Integrated Bootstrap Diode	t_{ON} / t_{OFF} (typ)
2ED1324S12P	PG-DSO-20-U03	+ 2.3 / - 2.3	OCP, AMC, SCC, RFE	Yes	380 ns	Yes	500 ns
2ED1323S12P	PG-DSO-20-U03	+ 2.3 / - 2.3	OCP, AMC, SCC, RFE	No	None	Yes	350 ns
2ED1322S12M	PG-DSO-16-U02	+ 2.3 / - 4.6	OCP, RFE	Yes	380 ns	Yes	500 ns
2ED1321S12M	PG-DSO-16-U02	+ 2.3 / - 4.6	OCP, RFE	No	None	Yes	350 ns

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2 Block diagram

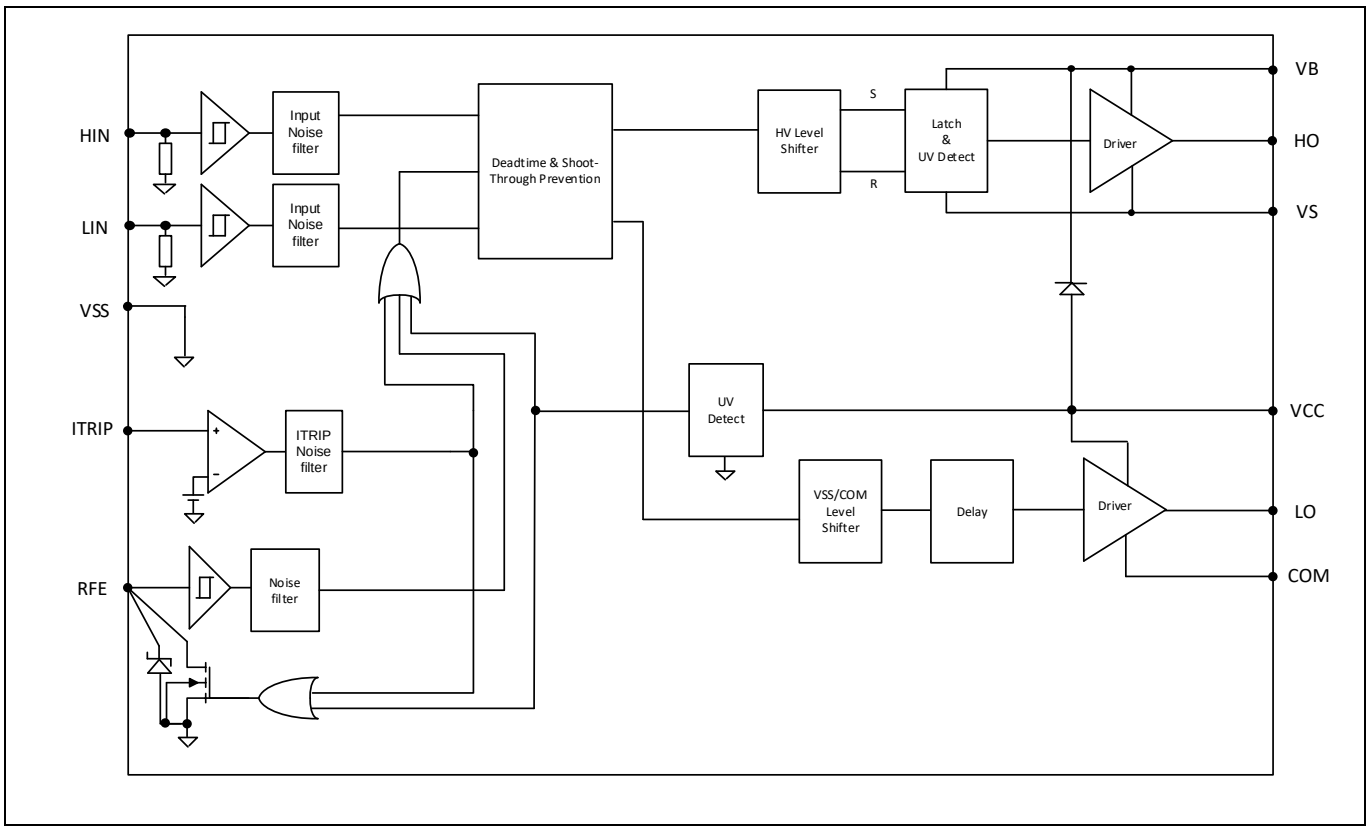
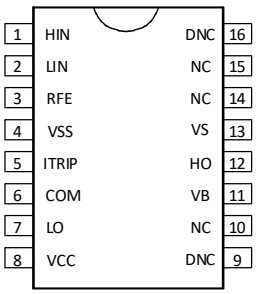


Figure 2 Block diagram of 2ED1322S12M

3 Pin configuration and functionality

3.1 Pin configuration



16-Lead PG-DSO-16-U02 (300 mil)
2ED1322S12M/2ED1321S12M

Figure 3 Pin assignment (top view)

3.2 Pin functionality

Table 2

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase with HO
LIN	Logic input for low side gate driver output (LO), in phase with LO
RFE	Integrated fault reporting function like over-current protection (OCP), or low-side undervoltage lockout and the fault clear timer. This pin has negative logic and an open-drain output. The use of over-current protection requires the use of external components
VSS	Logic ground
ITRIP	Analog input for over-current shutdown. When active, OCP shuts down outputs and activates RFE low. When OCP becomes inactive, RFE stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance)
COM	Low-side gate drive return
LO	Low-side driver output
VCC	Low-side and logic supply voltage
VS	High voltage floating supply return
HO	High-side driver output
VB	High-side gate drive floating supply
NC	Pin Not Connected
DNC	**Do Not Connect the pin to any electrical node**

4 Electrical parameters

4.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. (Ta = 25°C).

Table 3 Absolute maximum ratings

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating well supply voltage Note 1	-0.5	1225	V
V_S	High-side floating well supply return voltage Note 1	V_B – 25	V_B + 0.5	
V_{BS}	High-side floating supply voltage (V_B vs. V_S) (internally clamped)	-1	25	
V_{HO}	Floating gate drive output voltage	V_S – 0.5	V_B + 0.5	
V_{CCGND}	Low side supply voltage (V_{CC} vs. V_{SS}) (internally clamped)	-1	25	
V_{CC}	Low side supply voltage (V_{CC} vs. V_{COM}) (internally clamped)	-1	25	
V_{LO}	Low-side output voltage	–0.5	V_{CC} + 0.5	
V_{IN}	Logic input voltage (HIN, LIN, RFE, ITRIP)	V_{SS} - 5	V_{CC} + 0.5	
dV_S/dt	Allowable V_S offset supply transient relative to COM	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq$+25°C Note 2	—	1.6	W
Rth_{JA}	Thermal resistance, junction to ambient Note 3	—	78	°C/W
Ψ_{Jtop}	Characterization parameter junction to package top Note 3		4	
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Note 1: In case VCC > VB there is an additional power dissipation in the internal bootstrap diode between pins VCC and VB in case of activated bootstrap diode

Note 2: Consistent power dissipation of all outputs. All parameters inside operating range

Note 3: Obtained in a simulation on a JEDEC-standard and Ta = 50 °C, PD= 1W, PCB: JEDEC 2s2p (JESD 51-5)

4.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} – COM) = (V_B – V_S) = 15 V (Ta = 25°C).

Table 4 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_B	Bootstrap voltage	V_S + 13	V_S + 20	V
V_{BS}	High-side floating well supply voltage	13	20	
V_S	High-side floating well supply offset voltage Note 1	-8	1200	
V_{St}	Transient High-side floating well supply offer voltage (<700ns) Note 2	-100	1200	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{CC}	Low-side supply voltage	13	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN, LIN, RFE, ITRIP)	V_{SS}	V_{CC}	
V_{SS}	Logic ground	-5	5	
t_{IN}	Minimal pulse width for ON or OFF	0.3	—	µs
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -8 V to +1200 V

Note 2: In case V_{CC} > V_B there is an additional power dissipation in the internal bootstrap diode between pins V_{CC} and V_B. Insensitivity of bridge output to negative transient voltage up to –100 V is not subject to production test – verified by design / characterization

4.3 Static electrical characteristics

(V_{CC}– COM) = (V_B – V_S) = 15 V, V_{SS} = COM and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input leads: HIN and LIN. The V_O and I_O parameters are referenced to V_S / COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Table 5 Static electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	11.5	12.2	12.9	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	10.6	11.3	12		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	0.5	0.9	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	11.5	12.2	12.9		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	10.6	11.3	12		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	0.5	0.9	—		
I_{LK}	High-side floating well offset supply leakage	—	0.5	20	uA	V_B = 1215 V V_S = 1200 V
I_{QBS}	Quiescent V_{BS} supply current	—	180	350		V_{IN} = 0V or 3.3V
I_{QCC}	Quiescent V_{CC} supply current	—	600	1000		
V_{OH}	High level output voltage drop, V_{cc}- V_{LO} , V_B- V_{HO}	—	0.32	0.7	V	I_O = 100 mA
V_{OL}	Low level output voltage drop, V_O	—	0.18	0.4		
I_{o+mean}	Mean output current from 4.5 V to 7.5 V	1.4	2.0	—	A	C_L = 56 nF
I_{o+}[1]	Peak output current turn-on	—	2.3	—		R_L = 0 Ω PW ≤ 10 µs
I_{o-mean}	Mean output current from 7.5 V to 4.5 V	2.8	4.0	—		C_L = 56 nF
I_{o-}[1]	Peak output current turn-off	—	4.6	—		R_L = 0 Ω PW ≤ 10 µs
V_{IH}	Logic “1” input voltage (HIN, LIN, EN)	1.7	2.0	2.3	V	
V_{IL}	Logic “0” input voltage (HIN, LIN, EN)	0.7	0.9	1.1		
I_{IN+}	Input bias current (Output = High)	15	35	60	µA	V_{IN} = 3.3 V
I_{IN-}	Input bias current (Output = Low)	—	0	—		V_{IN} = 0 V
I_{RFE+}	Logic “1” Input bias current (RFE)	—	0	1		V_{RFE} = 3.3 V
I_{RFE-}	Logic “0” Input bias current (RFE)	—	0	—		V_{RFE} = 0 V
I_{ITRIP+}	Logic “1” Input bias current (ITRIP)	—	0	1		V_{IN} = 1 V
I_{ITRIP-}	Logic “0” Input bias current (ITRIP)	—	0	—		V_{IN} = 0 V
V_{FBSD}	Bootstrap diode forward voltage between Vcc and VB	—	1	1.2	V	I_F=0.3 mA
I_{FBSD}	Bootstrap diode forward current between Vcc and VB	40	70	100	mA	V_{CC}-V_B = 4 V
R_{BSD}	Bootstrap diode resistance	18	30	42	Ω	V_{F1} = 4 V, V_{F2} = 5 V
$R_{on,FLT}$	RFE low on resistance of the pull-down transistor	—	35	70		V_{RFE} = 0.5 V
V_{ACTSD}	Active shut-down voltage	—	2.1	2.4	V	I_{OUT-} = 200 mA V_{CC}/V_{BS} open
$V_{th,OCP}$	OCP comparator threshold	0.416	0.44	0.464		
$V_{th,OCPH}$	OCP comparator hysteresis	0.04	0.05	—		

[1] Not subjected to production test, verified by design/characterization

4.4 Dynamic electrical characteristics

V_{CC} = V_{BS}= 15 V, T_A = 25 °C and C_L = 1000 pF unless otherwise specified.

Table 6 Dynamic electrical characteristics

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	2ED1322	400	500	700	ns	V_{IN} = 0 V or 3.3 V V_S = 0 V or 1200 V
		2ED1321	250	350	500		
t_{OFF}	Turn-off propagation delay	2ED1322	400	500	700		
		2ED1321	250	350	500		
t_R	Turn-on rise time		—	48	80		V_{IN} = 0 or 3.3 V C_L = 4.9 nF
t_F	Turn-off fall time		—	48	80		
T_{EN}	RFE Enable propagation delay		400	500	700		V_{RFE} = 0.5 V, V_{LO}/V_{HO} = 20%
t_{FILIN}	Input filter time at LIN/HIN for turn-on and -off	2ED1322	100	150	—		V_{IN} = 0 & 3.3 V
		2ED1321	25	35	—		
t_{FILEN}	RFE Input filter time		100	150	220		
t_{FLTCLR}	RFE Fault-clear time		120	160	—	µs	V_{ITRIP} = 0.1 V, V_{RFE} = 2.1 V
t_{OCPfil}	ITRIP Filter time		0.3	0.5	0.7		V_{ITRIP} = 1 V
$t_{OCPOUT,LS}$	OCP Sense to Low-side OUT LOW delay		0.4	0.65	0.9		V_{ITRIP} = 1V V_{OUT} = 3V
$t_{OCPOUT,HS}$	OCP Sense to High-side OUT LOW delay		0.6	0.85	1.1		V_{ITRIP} = 1V V_{OUT} = 3V
t_{OCPFLT}	OCP Sense to RFE LOW delay		0.4	0.65	0.9		V_{ITRIP} = 1V V_{RFE} = 10%
$t_{UVLOFIL}$	UVLO Noise filter		1.0	1.5	—		
MT	Delay matching time (HS & LS turn-on/off)		—	10	60	ns	external dead time > 500 ns
DT	Dead time (2ED1322 only)		260	380	540		V_{IN} = 0 & 3.3 V
MDT	Matching Dead time (2ED1322 only)		—	10	80		external dead time 0ns
PM	Output pulse width matching		—	20	80		PW_{IN} > 1 µs

5 Application information and additional details

5.1 Gate drive

The 2ED132xS12 HVIC is designed to drive IGBTs or SiC MOSFETs. Figure 4 and Figure 5 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

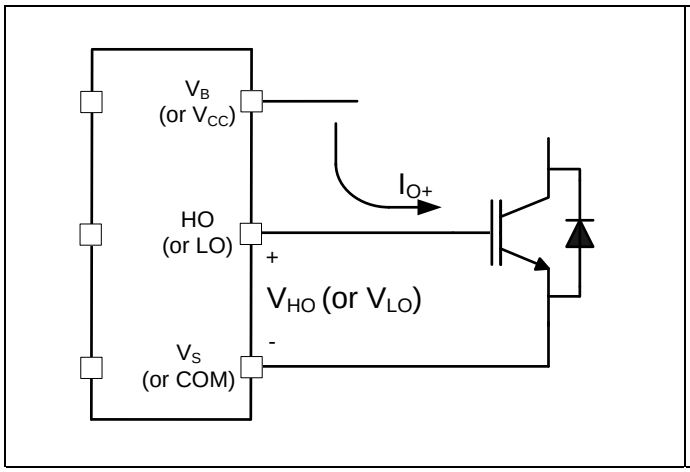


Figure 4 HVIC Sourcing current

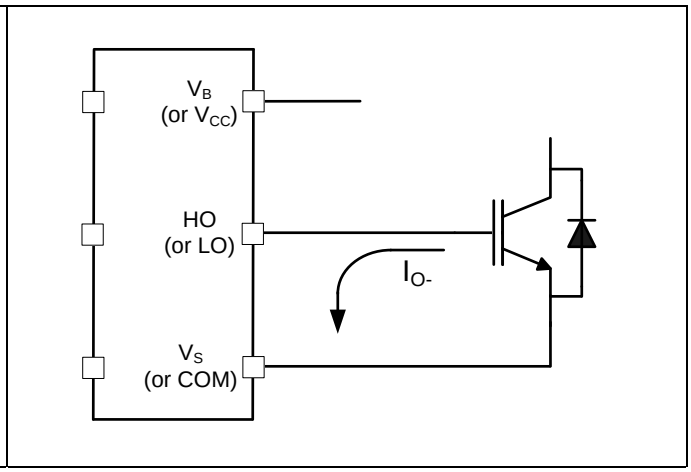


Figure 5 HVIC Sinking current

5.2 Switching relationships

The relationships between the input and output signals of the 2ED132xS12 are illustrated below in Figure 6 and Figure 7. From these figures, we can see the definitions of several timing parameters (i.e. t_{ON}, t_{OFF}, t_R, and t_F) associated with this device, and the input filter function that is used to reject noise.

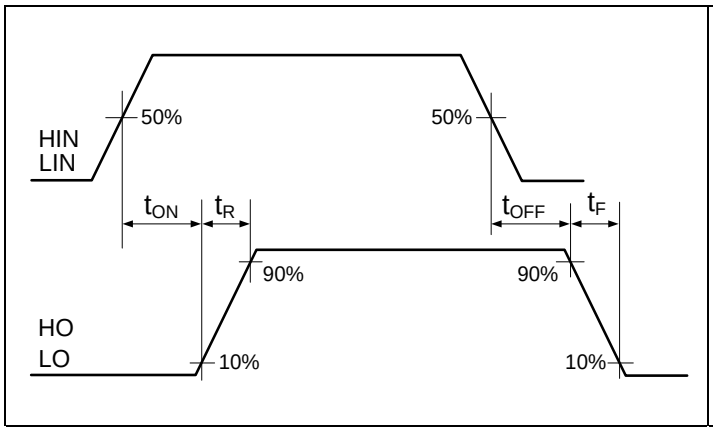


Figure 6 Switching timing diagram

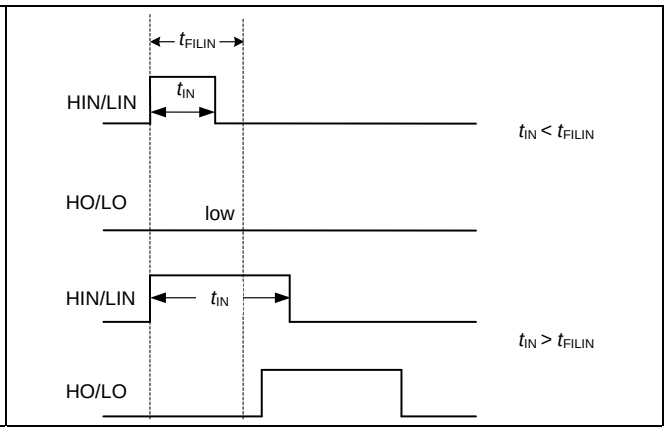


Figure 7 Input filter

5.3 Timing diagram

Here below Figure 8 and Figure 9 illustrate the timing relationships of some of the functionality of the 2ED1322S12M as an example; this functionality is described in further detail later in this document. During interval A of Figure 8, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition. HVIC is keeping on output channel that is already on ignoring the 2nd input signal.
Interval B of Figure 8 and Figure 9 shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HO has returned to the low state; LO is also held low), and a fault condition is reported on the RFE pin, which goes 0V. Once the ITRIP input has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RFE pin charges up to VRFE+ threshold; the charging characteristics are dictated by the RC network attached to the RFE pin. After fault clear time HVIC is waiting for a new input signal on LIN/HIN before activate the output stage (LO/HO).
During interval C of Figure 8 and Figure 10, we can see that the RFE pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); these results in the outputs (HO and LO) being held in the low state until the RFE pin is pulled high. After an enable event HVIC will wait for a new input signal on LIN/HIN before activate the output stage (LO/HO).

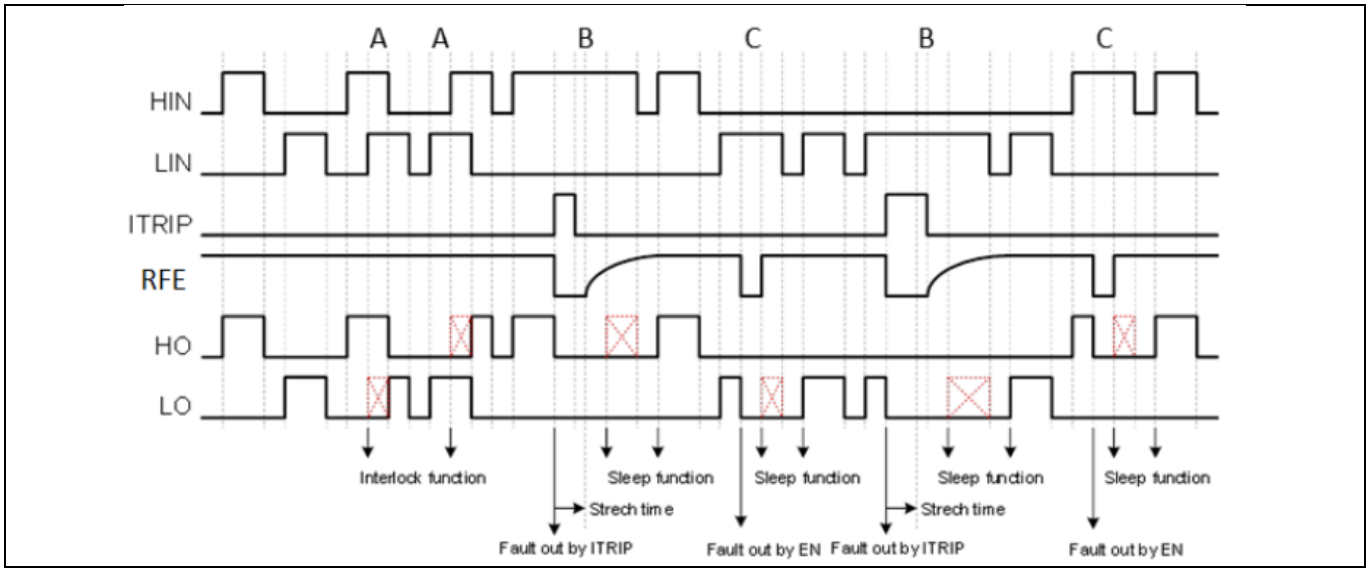


Figure 8 Input/ put timing diagram

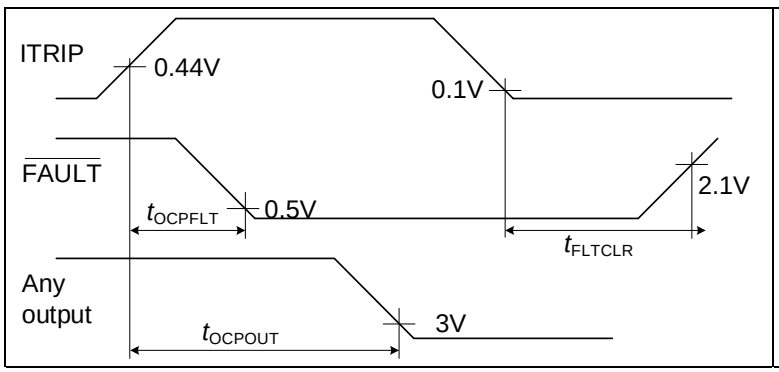


Figure 9 OCP timing (low-side)

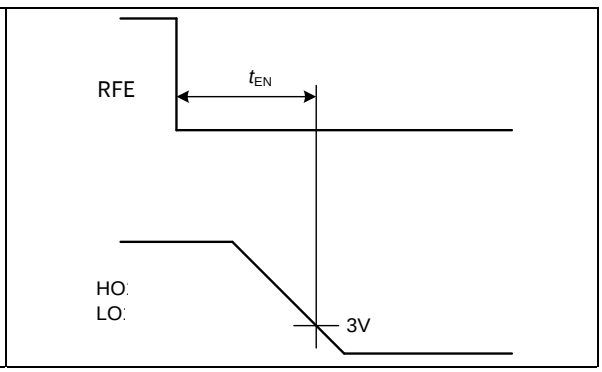


Figure 10 Enable delay time definition

5.4 Deadtime

This 2ED1322S12M features integrated deadtime protection circuitry. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than interal deadtime; external deadtimes larger than internal deadtime are not modified by the gate driver. Figure 11 illustrates the deadtime period and the relationship between the output gate signals.
The deadtime circuitry of 2ED1322S12M is matched with respect to the high- and low-side outputs. Figure 11 defines the two deadtime parameters (i.e., DT_{LO-HO} and DT_{HO-LO}); the deadtime matching parameter (MDT) associated with the 2ED1322S12M specifies the maximum difference between DT_{LO-HO} and DT_{HO-LO}.

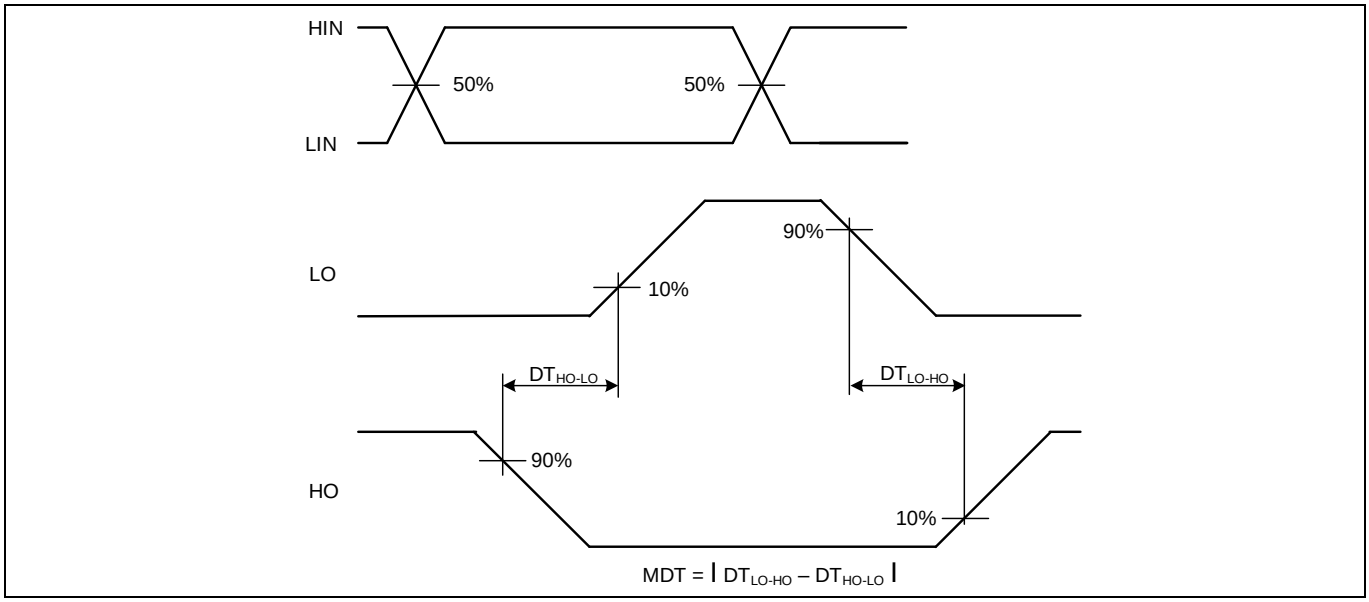


Figure 11 Deadtime matching waveform definition

5.5 Matched propagation delays

The 2ED132xS12 is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the 2ED132xS12 is matched to the propagation turn-on delay (t_{OFF}).

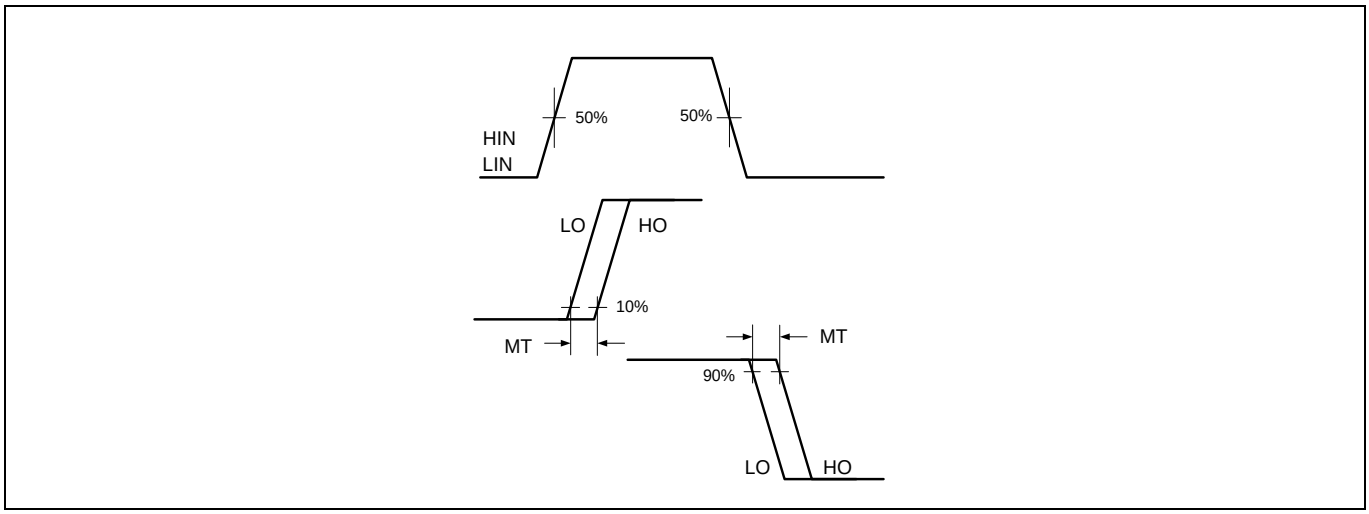


Figure 12 Delay matching waveform definition

5.6 Input logic compatibility

The input pins are based on a TTL and CMOS compatible input-threshold logic that is independent of the Vcc supply voltage. With typical high threshold (V_{IH}) of 2.0 V and typical low threshold (V_{IL}) of 0.9 V, along with very little temperature variation as summarized in Figure 13, the input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 1.1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. 2ED132xS12 also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The 2ED132xS12 features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved using pull-down resistors on all the input pins (HIN, LIN) as shown in the block diagram. The 2ED132xS12 has input pins that are capable of sustaining voltages higher than the bias voltage applied on the Vcc pin of the device.

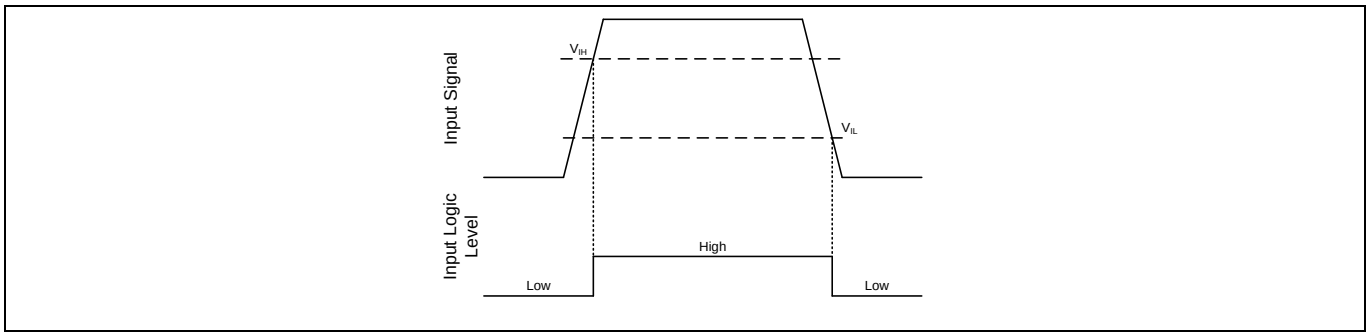


Figure 13 HIN & LIN input thresholds

5.7 Undervoltage lockout

This IC provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 14 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC won't turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV+} threshold, the IC won't turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

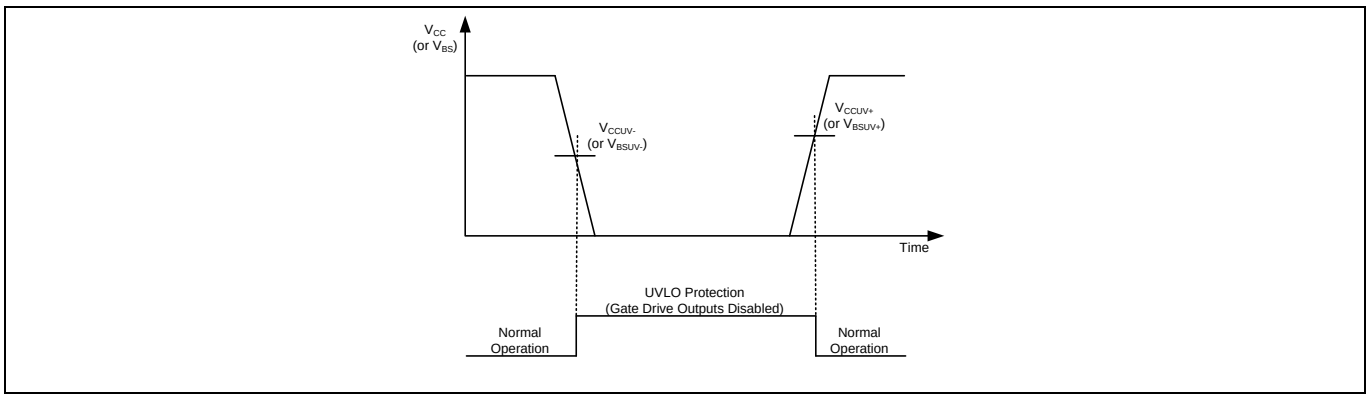


Figure 14 UVLO protection

5.8 Shoot-through protection

The 2ED1322S12M is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 15 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time.

Note: 2ED1321S12M no shoot-through protection because it is a high-side and low-side gate driver, HO and LO can turn on at the same time.

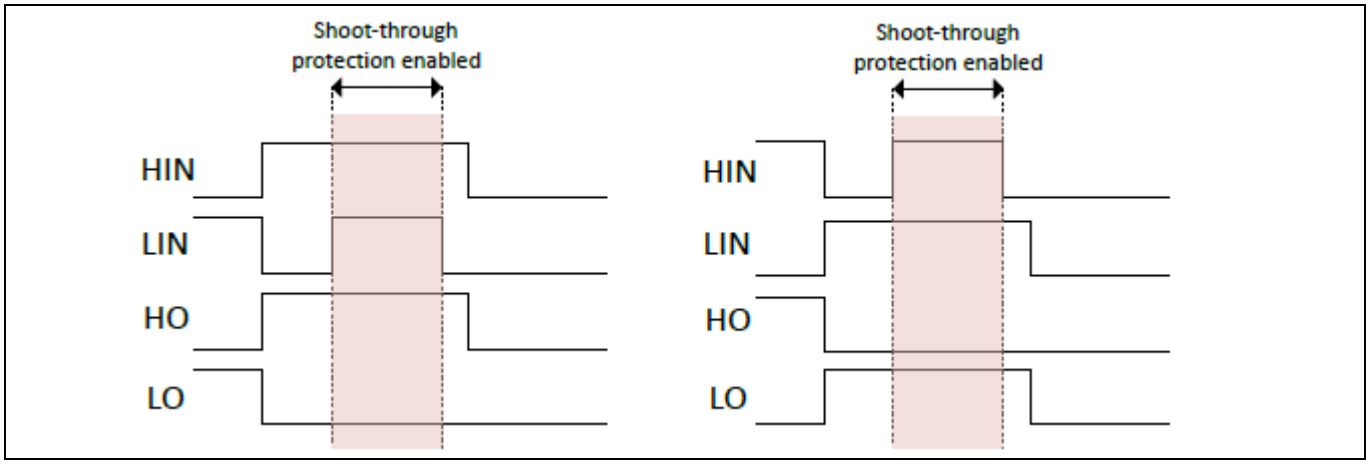


Figure 15 Illustration of shoot-through protection circuitry

5.9 Enable, Fault reporting and programmable fault clear timer

The 2ED132xS12 provides an enable functionality that allows it to shutdown or enable the HVIC and also provides an integrated fault reporting output along with an adjustable fault clear timer. There are two situations that would cause the IC to report a fault via the RFE pin. The first is an undervoltage condition of VCC and the second is if the over-current feature has recognized a fault. Once the fault condition occurs, the RFE pin is internally pulled to VSS and the fault clear timer is activated. The RFE output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the RFE pin will return to its external pull-up voltage.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RFE} and C_{RFE}. Figure 16 shows that R_{RFE} is connected between the external supply (V_{DD})[1)] and the RFE pin, while C_{RFE} is placed between the RFE and VSS pins.

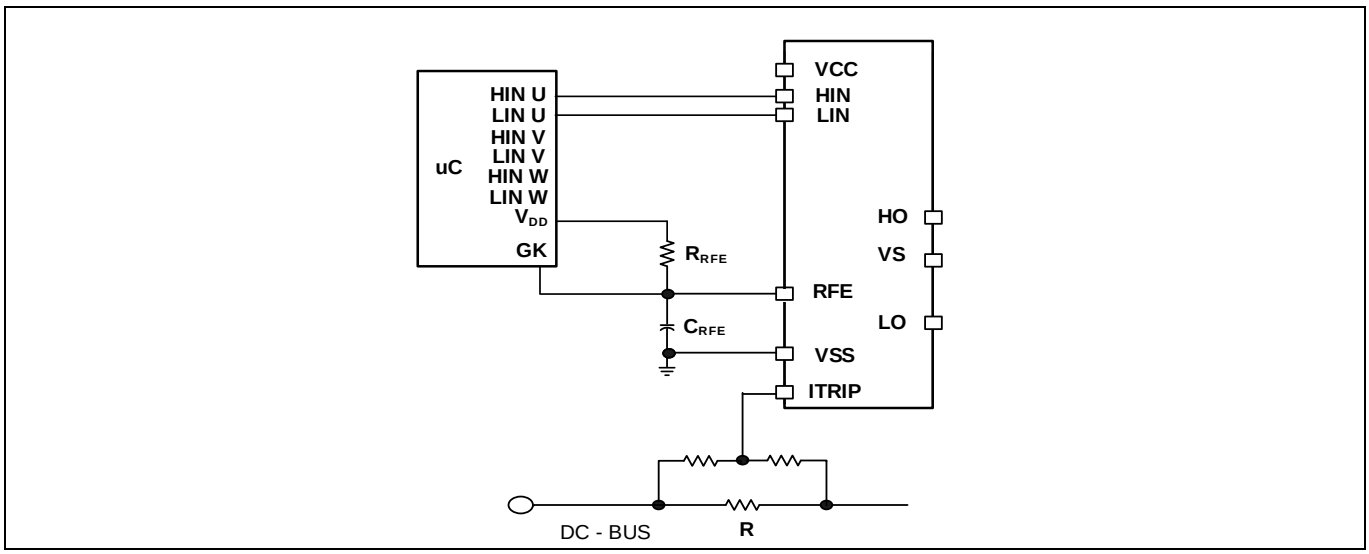


Figure 16 Programming the fault clear timer

The design guidelines for this network are shown in Table 7

Table 7 Design guidelines

C_{RFE}	≤ 1 nF
	Ceramic capacitor
R_{RFE}	0.5 MΩ to 2 MΩ
	>> $R_{ON,RCIN}$

The length of the fault clear time period can be determined by using the formula below.

$v_C(t) = V_{f*}(1-e^{-t/RC})$

$t_{FLTCLR} = - (R_{RFE*}C_{RFE}) *\ln (1-V_{IH}/V_{DD}) + 160us$

The voltage on the RFE pin should not exceed the VDD of the uC power supply.

[1] In case VDD is higher than 5V, the R_{RFE} resistor needs to be at least 200 kΩ in order to limit the IC power dissipation.

5.10 Over-current protection

The 2ED132xS12 is equipped with an over-current feature (ITRIP input pin). This functionality can sense over-current events in the DC- bus or low side power switch. Once the HVIC detects an over-current event, the outputs are shutdown, and RFE is pulled to VSS.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in Figure 17, and the OCP threshold ($V_{th,OCP}$). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold ($V_{th,OCP}$) at that current level.

$V_{th,OCP} = R_0*I_{DC-}*(R_1/ (R_1+R_2))$

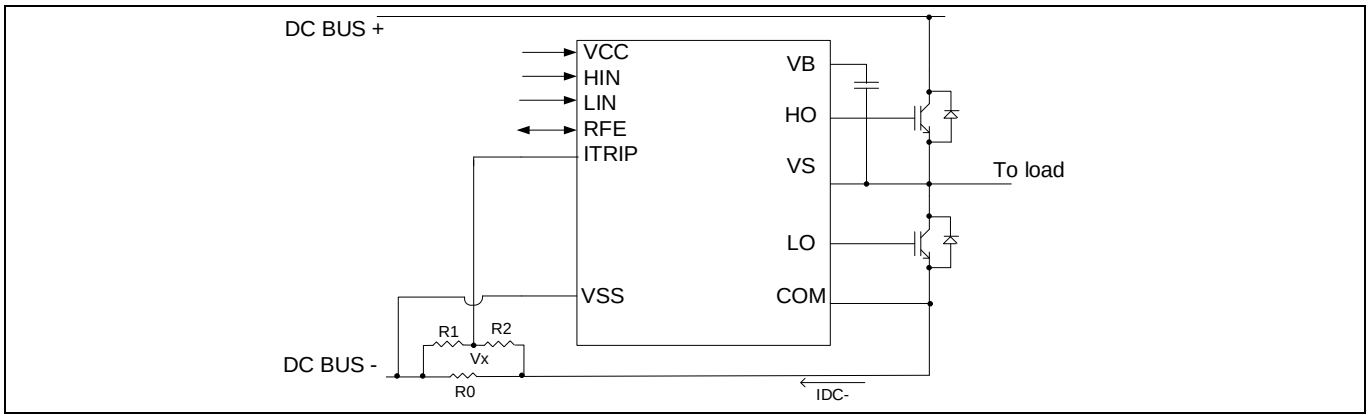


Figure 17 Programming the over-current protection

For example, a typical value for resistor R0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

5.11 Truth table: Undervoltage lockout, OCP and Enable

Table 8 provides the truth table for the 2ED132xS12. The first line shows that the UVLO for VCC has been tripped; the RFE output has gone low and the gate drive outputs have been disabled. VCCUV is not latched in this case and when VCC is greater than VCCUV, the FAULT output returns the driver is functional.

The second case shows that the UVLO for VBS has been tripped and that the high-side gate drive outputs have been disabled. After VBS exceeds the VBSUV threshold, HO will stay low until the HVIC input receives a new rising transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the OCP trip threshold has been reached and that the gate drive outputs have been disabled. This condition is stored in the external RC network waiting for fault clear time. The last case shows when the HVIC has received an external disable command through the RFE input to shutdown; as a result, the gate drive outputs have been disabled.

Table 8 2ED132xS12 UVLO, OCP, FLT/EN/RCIN

	VCC	VBS	ITRIP	RFE	LO	HO
UVLO V_{CC}	$<V_{CCUV}$	—	—	0	0	0
UVLO V_{BS}	15 V	$<V_{BSUV}$	0 V	HIGH	LIN	0
Normal operation	15 V	15 V	0 V	HIGH	LIN	HIN
OCP fault	15 V	15 V	$>V_{th,OCP}$	0	0	0
Disable command	15V	15V	0 V	0	0	0

5.12 Daisy Chain Multiple Devices

The 2ED132xS12 can be daisy chained together for applications which require more than one device, such as in the three phase circuit shown below. In Figure 18, the three 2ED132xS12 RFE pins are connected together. The ITRIP sensing is only used on the first HVIC; the other two ITRIP pins are disabled by tying them to VSS. The programmable fault clear timing components, R_{RFE} and C_{RFE}, are populated only once for the RFE pin. When a fault occurs, either from ITRIP or UVLO, or an external command, all three HVICs are disabled via the daisy chained RFE pin being pulled low to VSS.

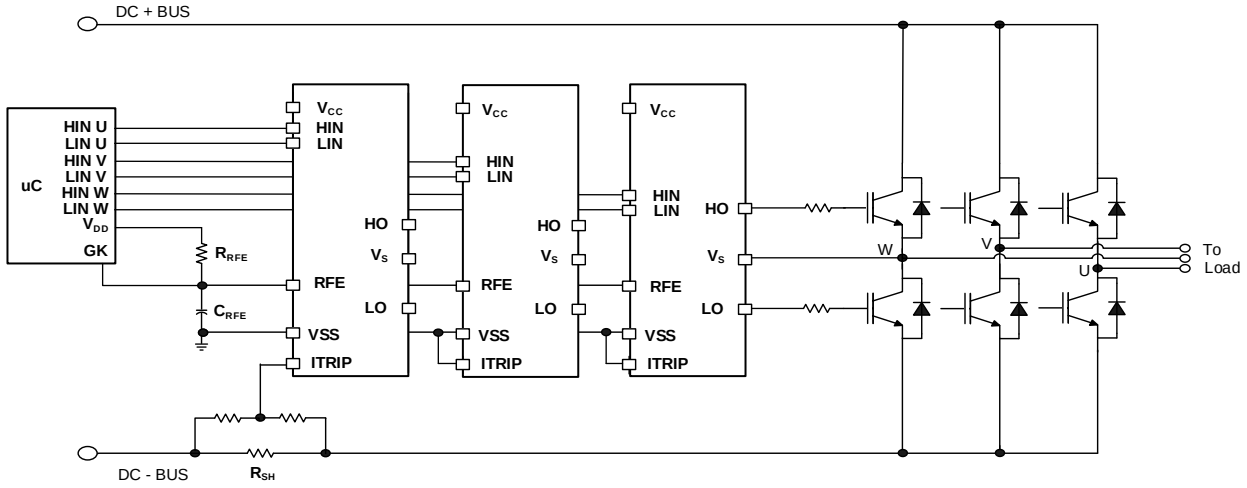


Figure 18 Figure 13: Daisy Chain Circuit with Single Shunt

In Figure 19 three of the individual leg currents of the three phases can be measured. The RFE pins are connected together with the components for the pin only populated for the first HVIC. Three of the ITRIP pins are used to monitor the three of the individual leg current. A fault can occur by the ITRIP sensing network for either of the three legs, shutting down all three 2ED132xS12 HVICs, which means all the three phases have over current protection indidvidually.

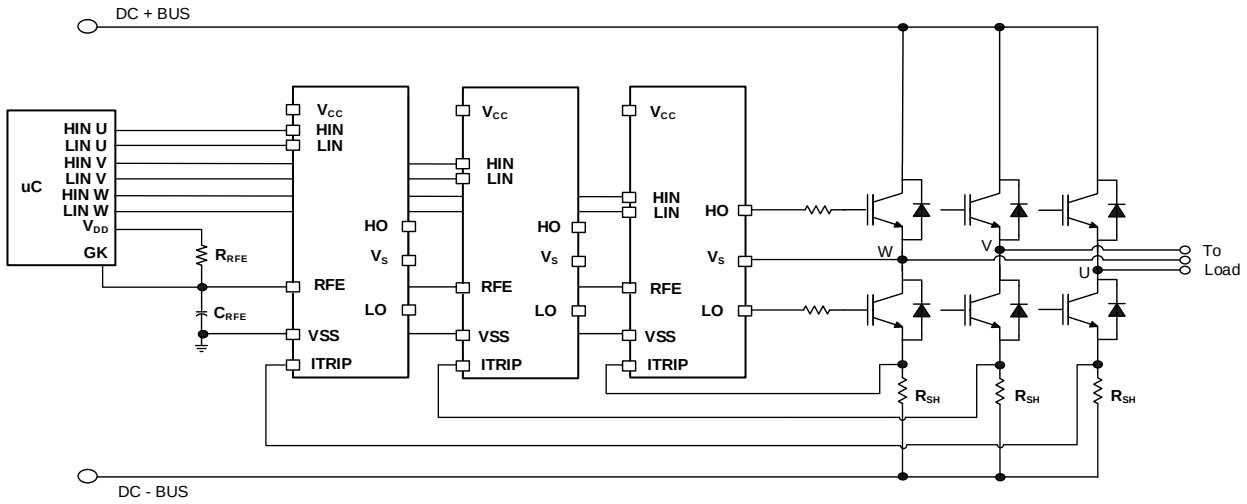


Figure 19 Daisy Chain circuit with Leg Shunt

5.13 Bootstrap diode

An ultra-fast bootstrap diode is monolithically integrated for establishing the high side supply. The dynamic resistor of the diode helps to avoid extremely high inrush currents when initially charging the bootstrap capacitor. The integrated diode with its resistrance helps save cost and improve reliability by reducing external components as shown below Figure 20.

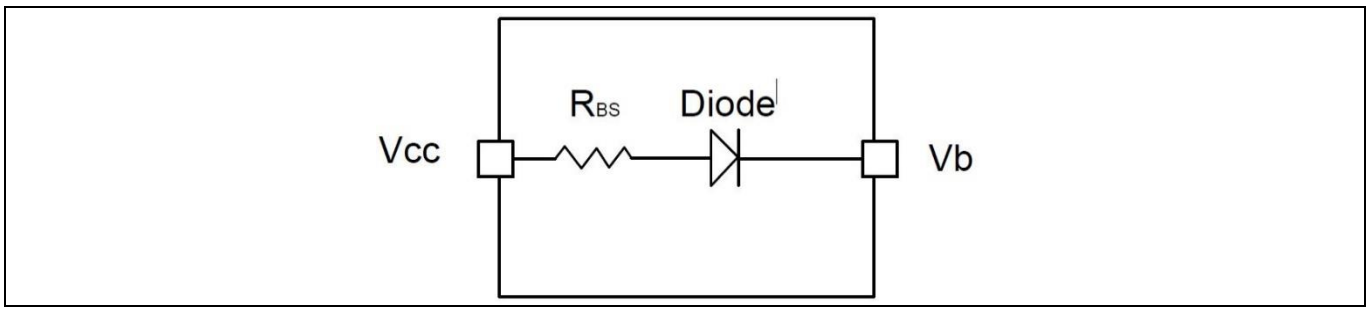


Figure 20 2ED132xS12 with integrated components

The low ohmic current limiting resistor provides essential advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 2ED132xS12 allows faster recharging of the bootstrap capacitor during periods of small duty cycles on the low side transistor. The bootstrap diode is usable for all kind power electronic converters. The bootstrap diode is a real pn-diode and is temperature robust. It can be used at high temperatures with a low duty cycle of the low side transistor.

The bootstrap diode of the 2ED132xS12 works with all control algorithms of modern power electronics, such as trapezoidal or sinusoidal motor drives control.

5.14 Calculating the bootstrap capacitance C_{BS}

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according toFigure 21. This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations.

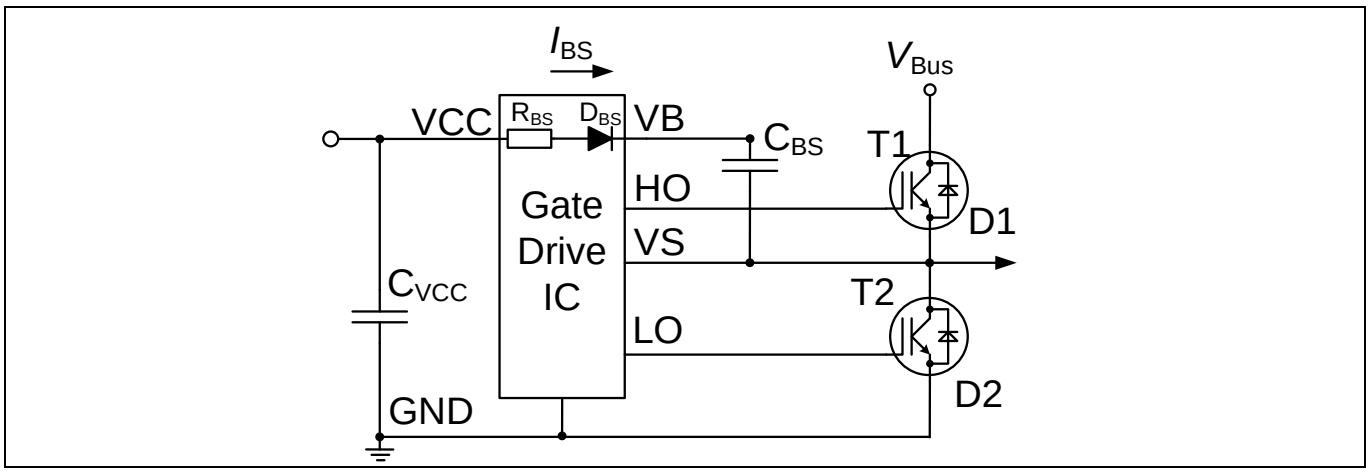


Figure 21 Half bridge bootstrap circuit in 2ED132xS12

When the low side power device turns on, it will force the potential of pin V_S to GND. The existing difference between the voltage of the bootstrap capacitor V_{CBS} and V_{CC} results in a charging current I_{BS} into the capacitor C_{BS}. The current I_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS} must be very small in order to avoid losses in the capacitor that result in lower lifetime of the capacitor. This pin is on high potential again after low side is turned off and high side is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor C_{VCC}. The bootstrap diode D_{BS} also takes over the blocking voltage between pin V_B and V_{CC}. The voltage of the bootstrap capacitor can now supply the high side gate drive sections. It is a general design rule for the location of bootstrap capacitors C_{BS}, that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes,

which may trigger the undervoltage lockout threshold of the individual high side driver section. However, all parts of the 2ED132xS12, which have the UVLO also contain a filter at each supply section in order to actively avoid such undesired UVLO triggers.

The current limiting resistor R_{BS} according to Figure 21 reduces the peak of the pulse current during the low side power device turn-on. The pulse current will occur at each turn-on of the low side power device, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: The high side quiescent current and the gate charge of the high side MOSFET to be turned on.

The minimum size of the bootstrap capacitor is given by

$$C_{BS} = \frac{Q_{GTOT}}{\Delta V_{BS}}$$

ΔV_{BS} is the maximum allowable voltage drop at the bootstrap capacitor within a switching period, typically 1 V. It is recommended to keep the voltage drop below the undervoltage lockout (UVLO) of the high side and limit

$$\Delta V_{BS} \leq (V_{CC} - V_F - V_{GSmin} - V_{DSon})$$

$V_{GSmin} > V_{BSUV-}$, V_{GSmin} is the minimum gate source voltage we want to maintain and V_{BSUV-} is the high-side supply undervoltage negative threshold.

V_{CC} is the IC voltage supply, V_F is bootstrapdiode forward voltage and V_{DSon} is drain-source voltage of low side power device.

Please note, that the value Q_{GTOT} may vary to a maximum value based on different factors as explained below and the capacitor shows voltage dependent derating behavior of its capacitance.

The influencing factors contributing V_{BS} to decrease are:

- Power device turn on required Gate charge (Q_G)
- Power device gate-source leakage current (I_{LK_GS})
- Floating section quiescent current (I_{QBS})
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE})
- Charge required by the internal level shifters (Q_{LS}): typical 1nC
- Bootstrap capacitor leakage current (I_{LK_CAP})
- High side on time (T_{HON})

Considering the above,

$$Q_{GTOT} = Q_G + Q_{LS} + \left(I_{QBS} + I_{LK_{GS}} + I_{LK} + I_{LK_{DIODE}} + I_{LK_{CAP}}\right) * T_{HON}$$

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic capacitor and low ESR ceramic capacitor may result in an efficient solution).

The above C_{BS} equation is valid for pulse by pulse considerations. It is easy to see, that higher capacitance values are needed, when operating continuously at small duty cycles of low side. The recommended bootstrap capacitance is therefore in the range up to 4.7 µF for most switching frequencies.

5.15 Tolerant to negative transients on input pins

Typically the driver's ground pin is connected close to the source pin of the power device. The microcontroller which sends the HIN and LIN PWM signals refers to the same ground and in most cases there will be an offset voltage between the microcontroller ground pin and driver ground because of ground bounce. The 2ED132xS12 can handle negative voltage spikes up to 5 V. Standard half bridge or high-side/low-side drivers only allow negative voltage levels down to -0.3 V. The 2ED132xS12 has much better noise immunity capability on the input pins.

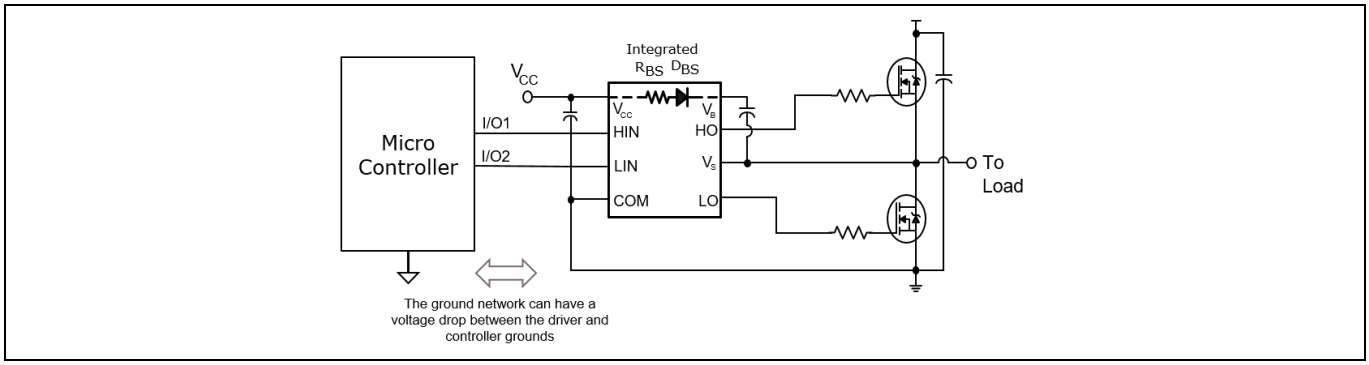


Figure 22 Negative voltage tolerance on inputs of upto –5 V

5.16 Negative voltage transient tolerance of VS pin

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 23, here we define the power switches and diodes of the inverter.
If the high-side switch (e.g., the IGBT Q1 in Figure 24) switches from on to off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

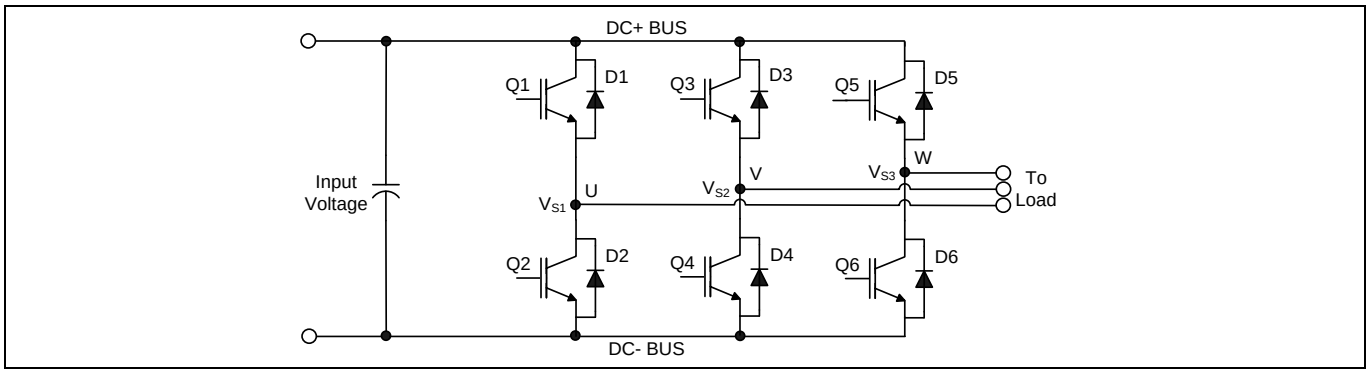


Figure 23 Three phase inverter

Also when the V phase current flows from the inductive load back to the inverter (see Figure 24 C) and D)), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient"

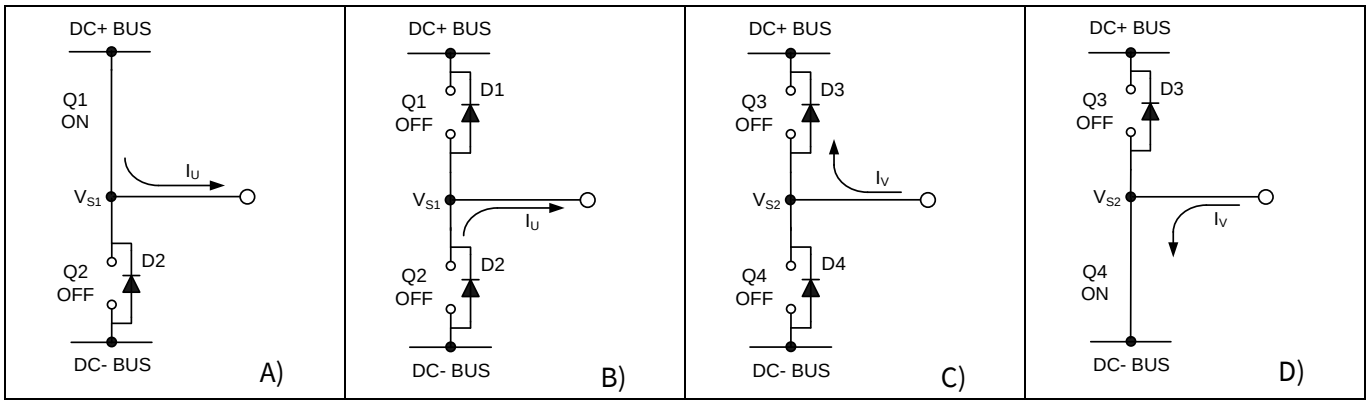


Figure 24 A) Q1 conducting B) D2 conducting C) D3 conducting D) Q4 conducting

The circuit shown in Figure 25-A depicts one leg of the three phase inverter; Figure 25-B and Figure 25-C show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

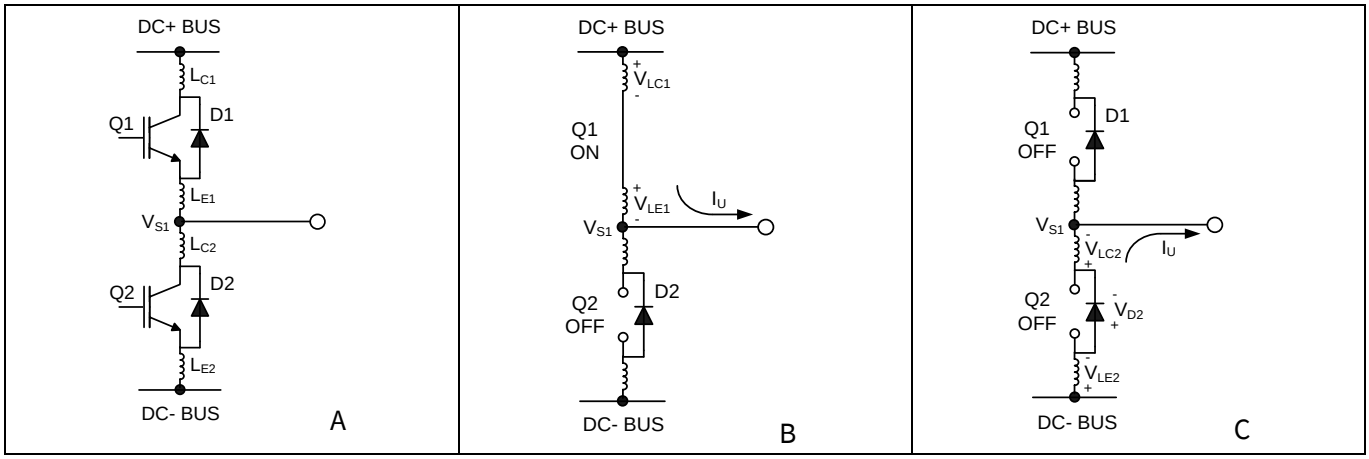


Figure 25 Figure A shows the Parasitic Elements. Figure B shows the generation of V_S positive. Figure C shows the generation of V_S negative

5.17 NTSOA – Negative Transient Safe Operating Area

In a typical motor drive system, dV/dt is typically designed to be in the range of 3 – 5 V / ns. The negative VS transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 2ED132xS12's robustness can be seen in Figure 26, where the 2ED132xS12's Safe Operating Area is shown at V_{BS}=15 V based on repetitive negative VS spikes. A negative VS transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

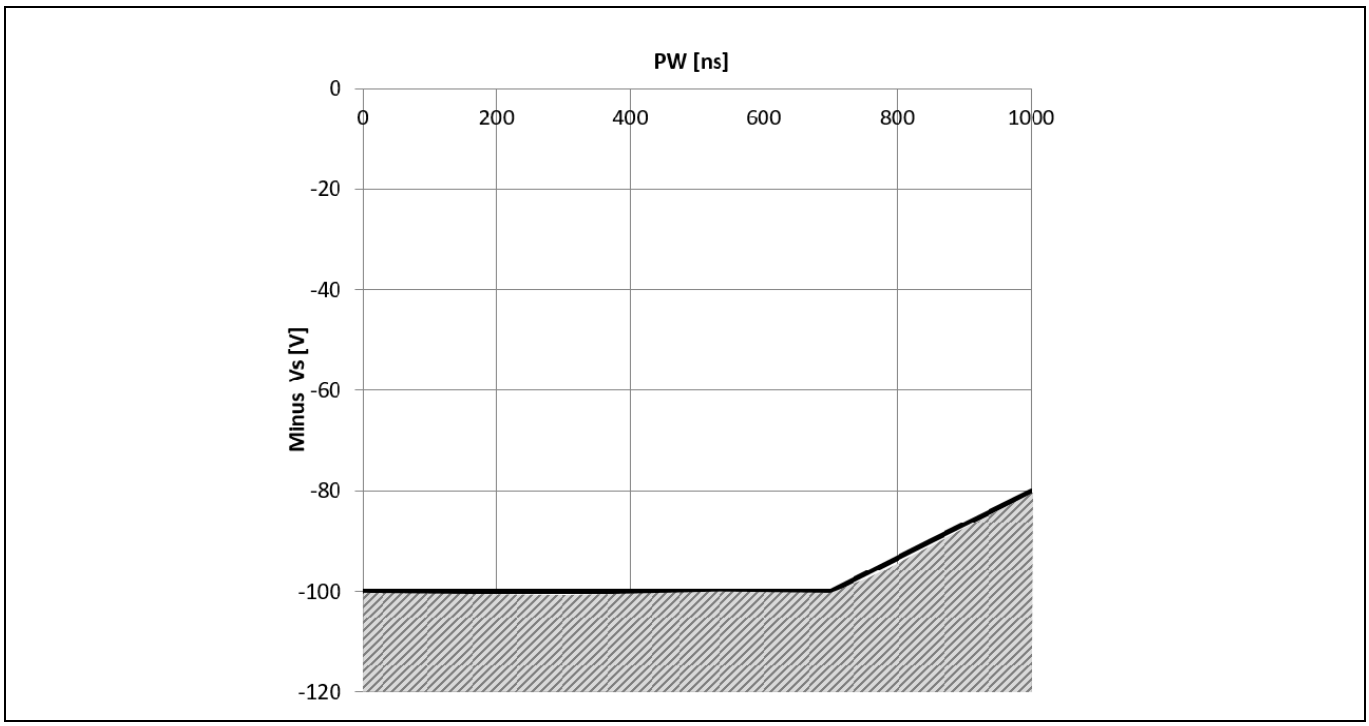


Figure 26 Negative VS transient SOA for 2ED132xS12

Even though the 2ED132xS12 has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative VS transients as much as possible by careful PCB layout and component use.

5.18 PCB layout tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 27). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

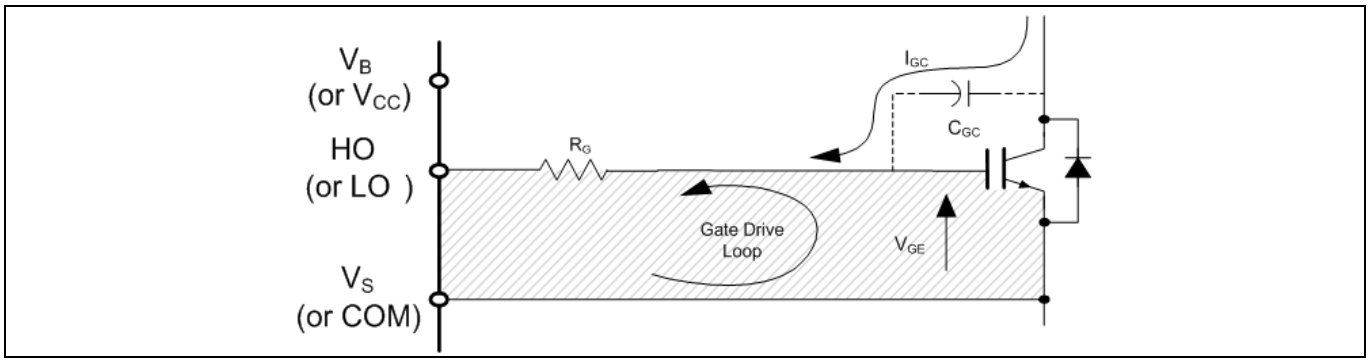


Figure 27 Avoid antenna loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and COM pins. A ceramic 1µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative VS spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the VS pin and the switch node (see Figure 28 - A), and in some cases using a clamping diode between COM and V_S (see Figure 28 - B). See DT04-4 at www.infineon.com for more detailed explanations.

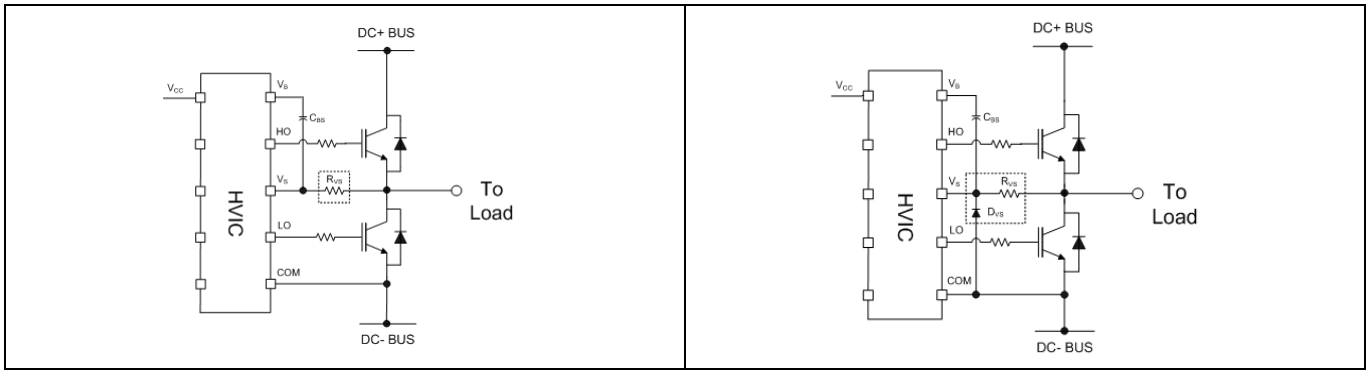


Figure 28 Resistor between the VS pin and the switch node and clamping diode between COM and V_S

6 Temperature trend charts

Figures illustrated in this chapter provide information on the experimental performance of the 2ED1322S12M/2ED1321S12M. The line plotted in each figure is generated from actual lab data unless otherwise specified. A large number of individual samples were tested sweeping the temperature in order to generate the experimental curve. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of each parameter.

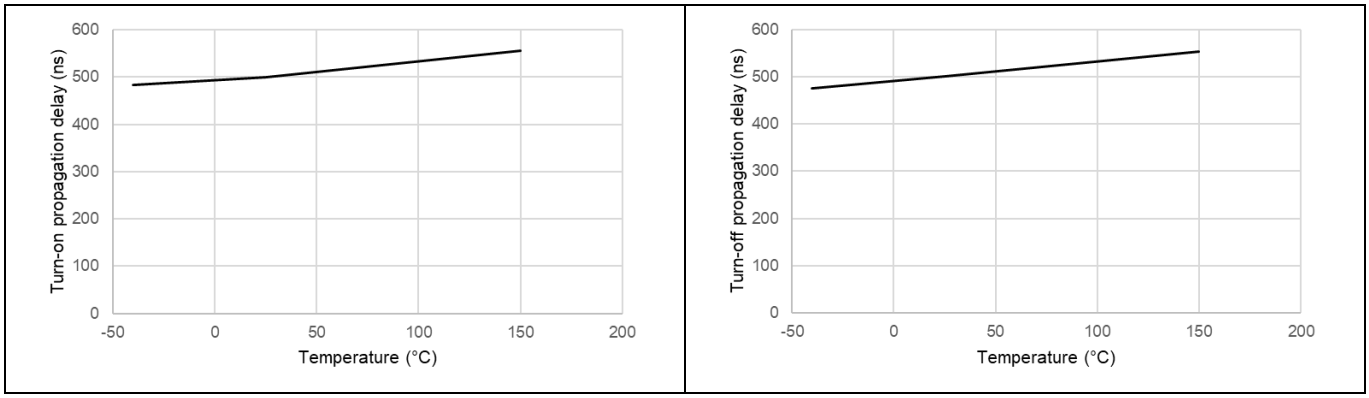


Figure 29 Turn-on/Turn-off propagation delay (2ED1322S12M)

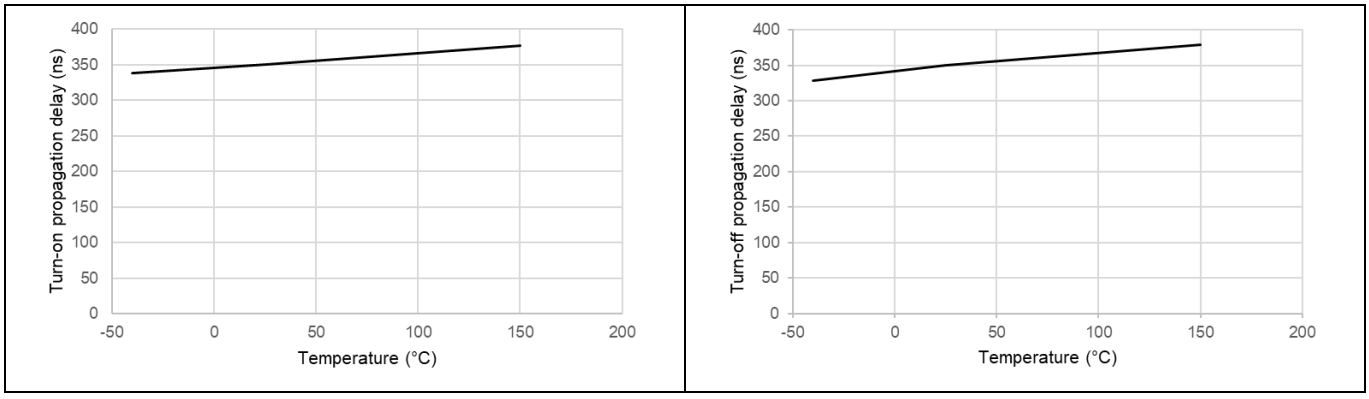


Figure 30 Turn-on/Turn-off propagation delay (2ED1321S12M)

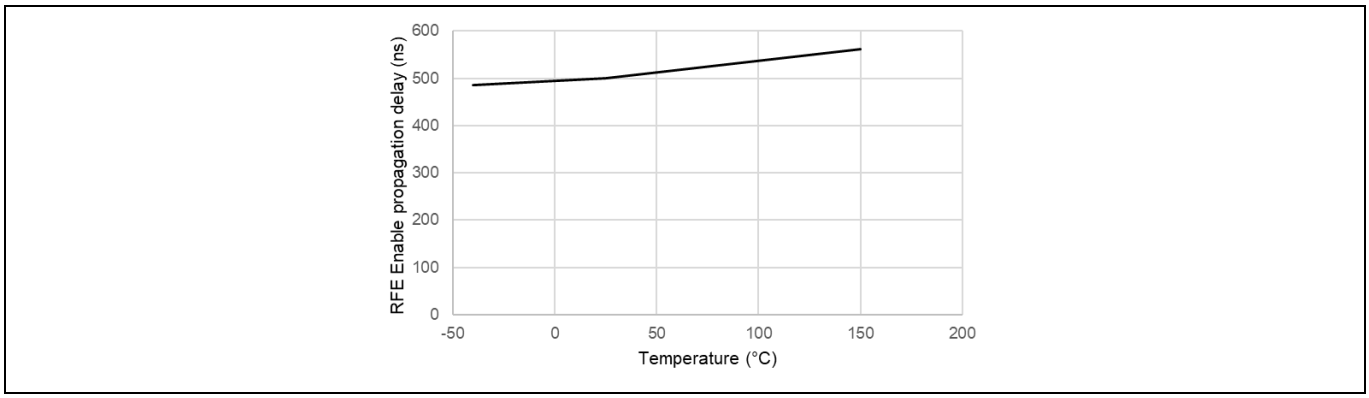


Figure 31 RFE Enable propagation delay

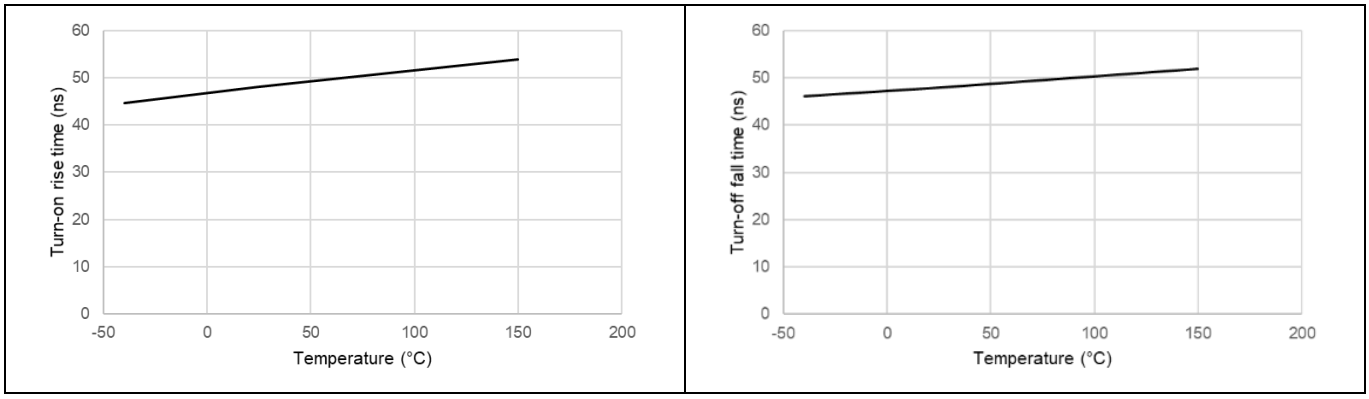


Figure 32 Turn-on rise time and Turn-off fall time

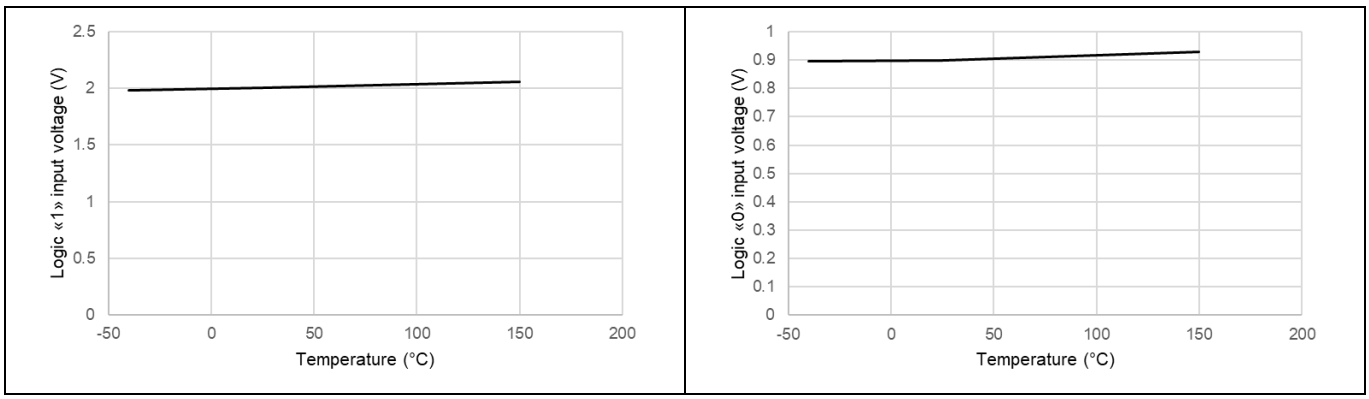


Figure 33 Logic “1” and logic “0” input voltage

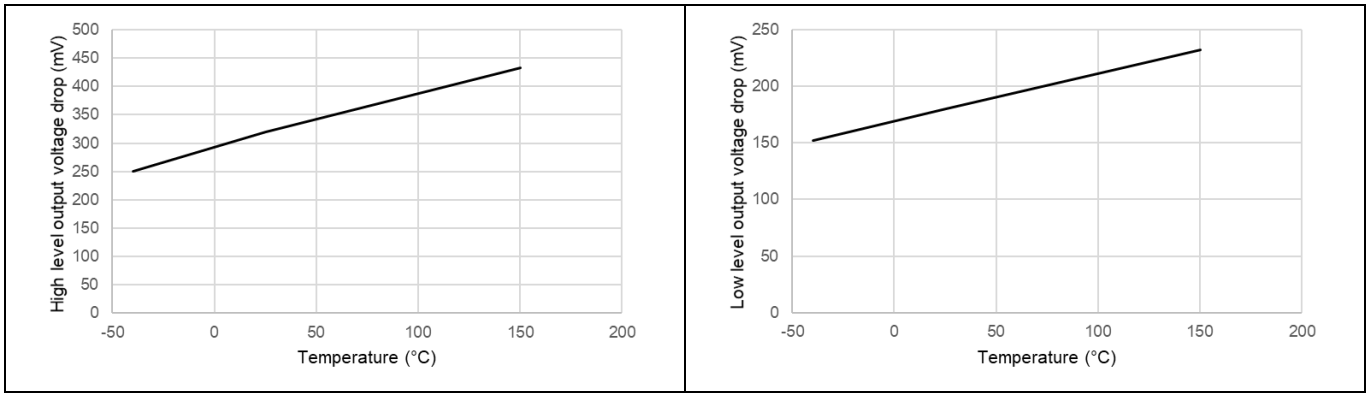


Figure 34 High/Low level output voltage drop

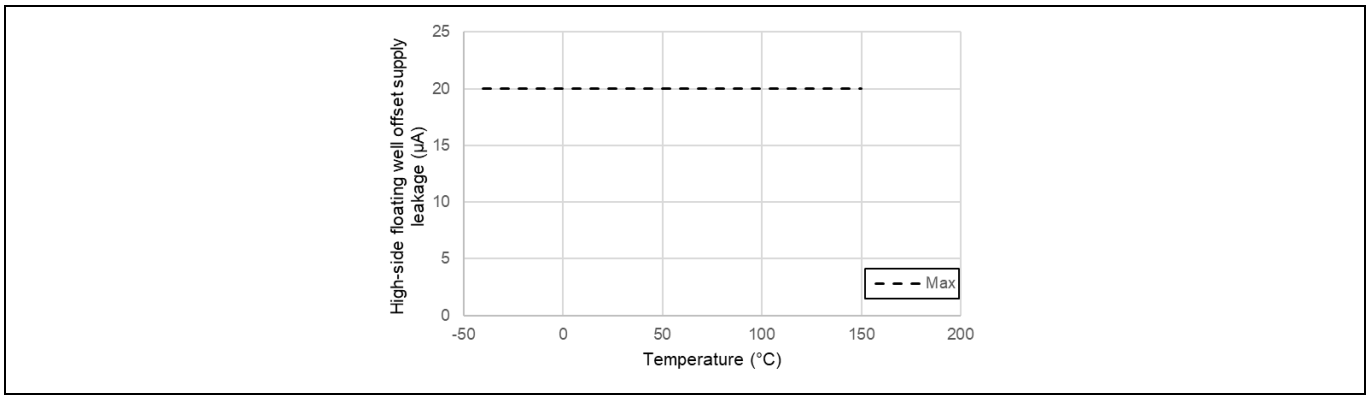


Figure 35 High-side floating well offset supply leakage

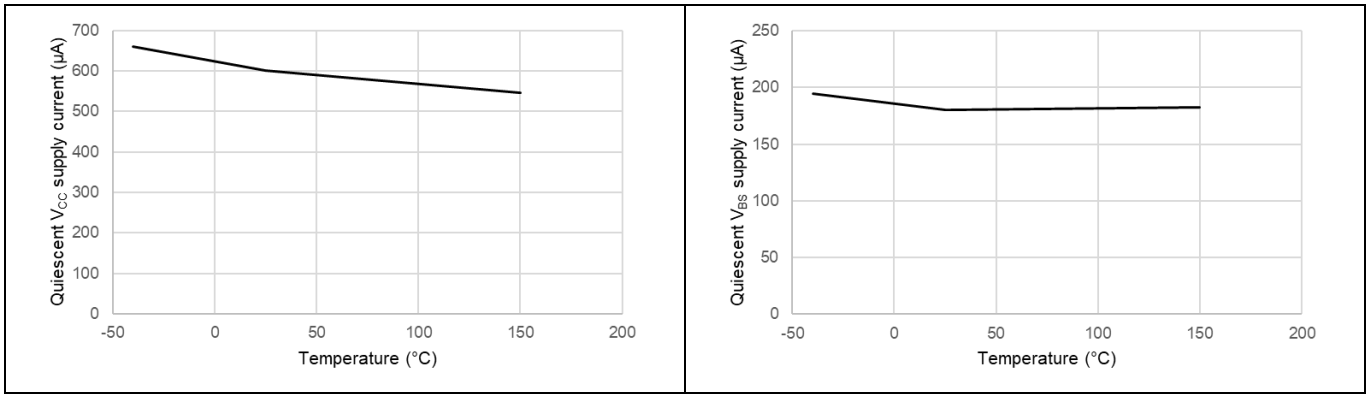


Figure 36 Quiescent V_{CC} and V_{BS} supply current

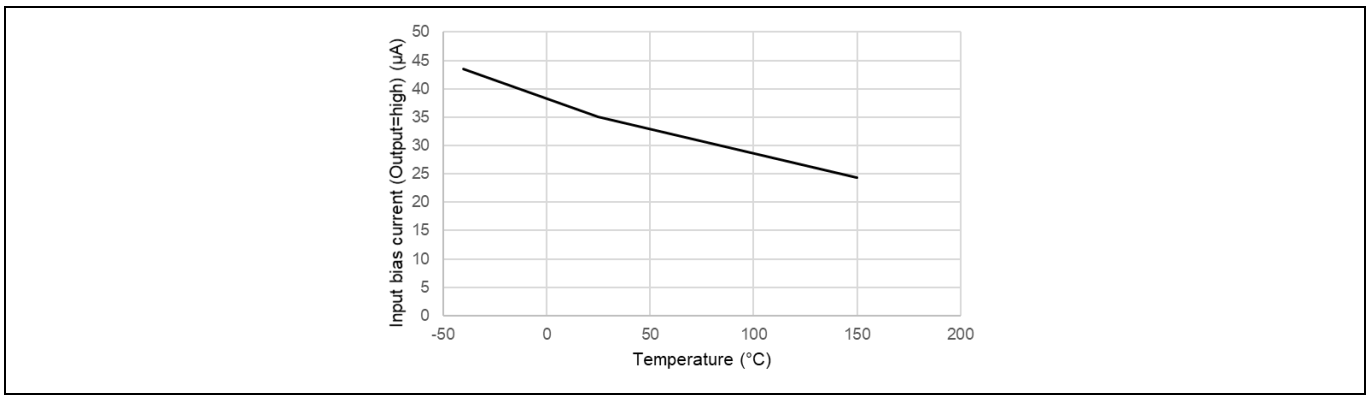


Figure 37 Input bias current

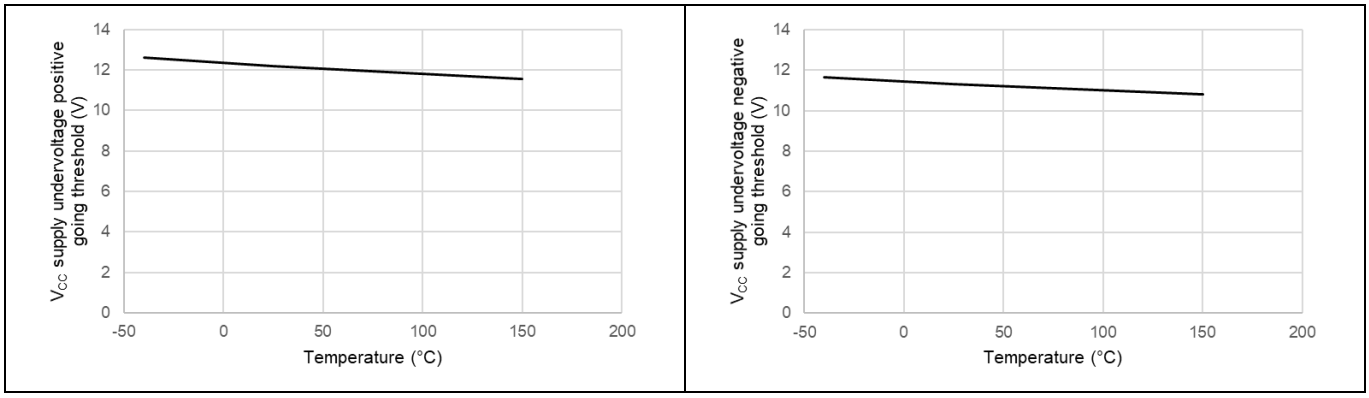


Figure 38 V_{CC} supply undervoltage positive/negative going threshold

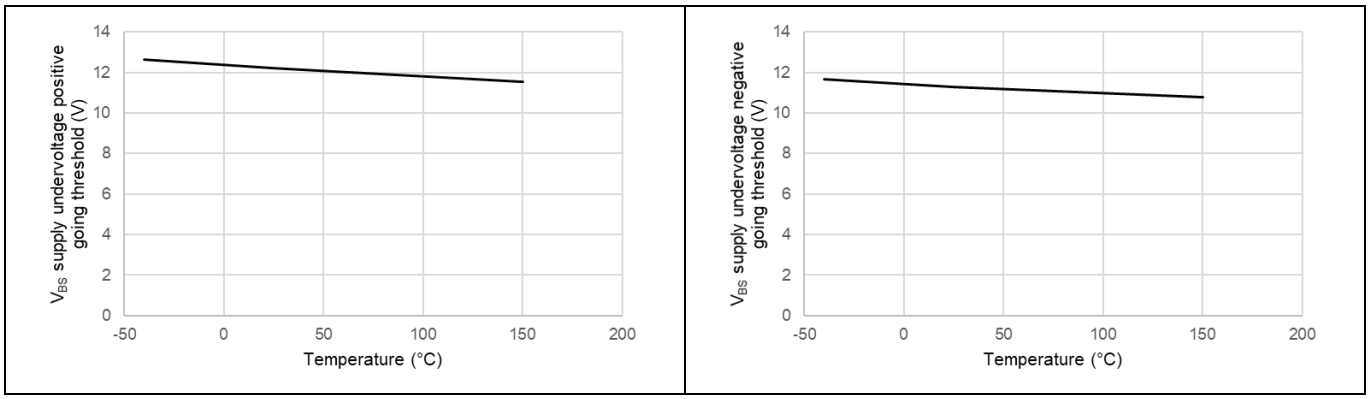


Figure 39 V_{BS} supply undervoltage positive/negative going threshold

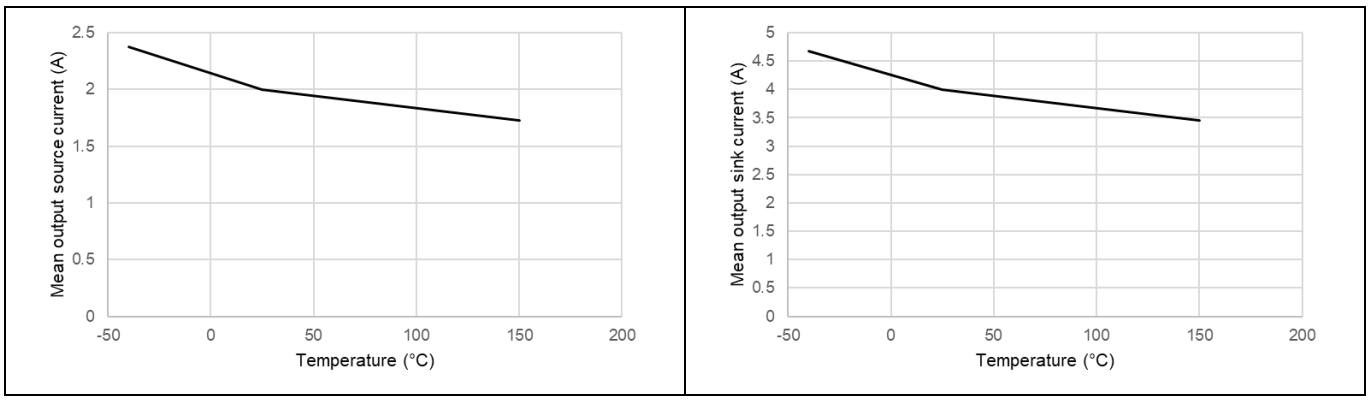


Figure 40 Mean source/sink output current

7 Qualification information[1]

Table 9 Qualification information

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		DSO-16-44	MSL2a[3], 260°C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (1.0 kV) (per JESD22-C101)	
	Human body model	Class 2 (2 kV) (per JEDEC standard JESD22-A115)	
IC latch-up test		Class II Level A (per JESD85)	
RoHS compliant		Yes	

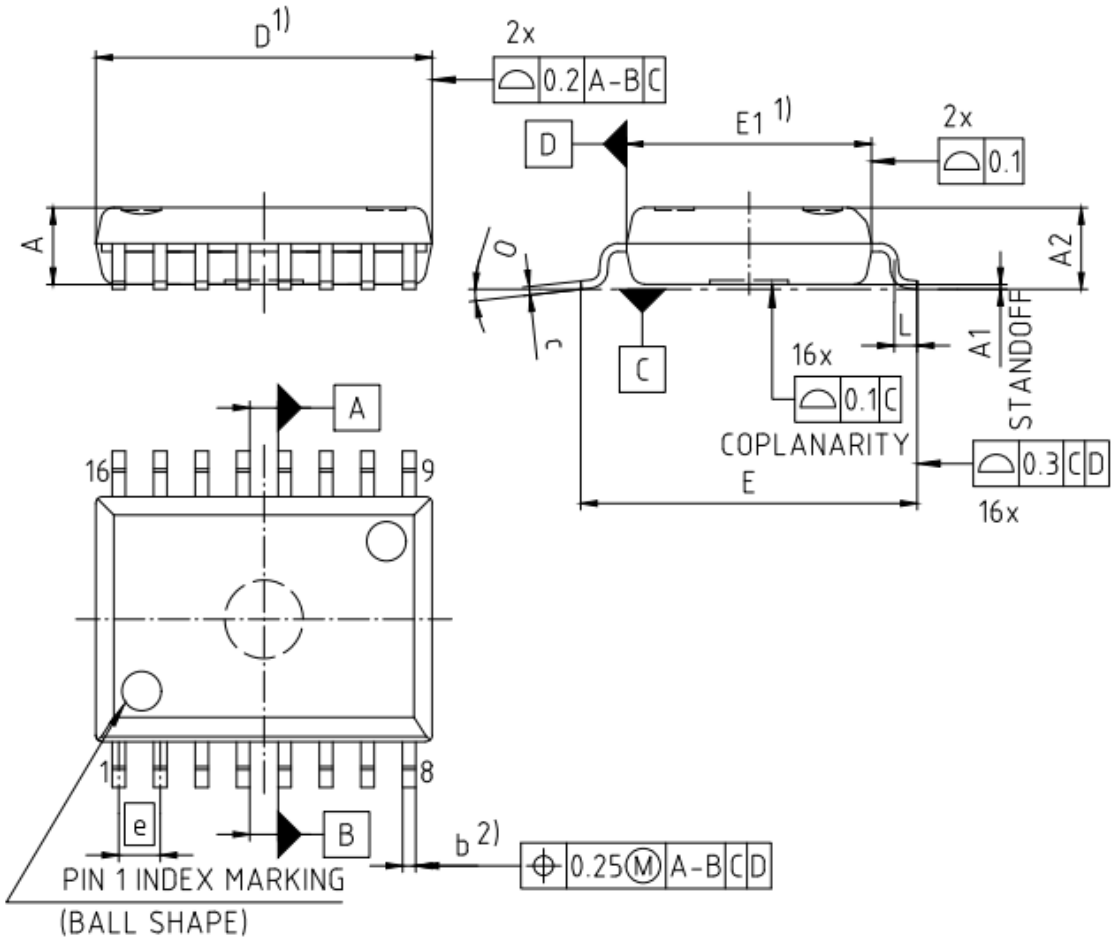
[1] Qualification standards can be found at Infineon's web site www.infineon.com
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
[3] Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

8 Related products

Table 10

Product	Description
Gate Driver ICs	
6ED2230S12T 6ED2231S12T	1200 V, 3 phase level shift thin-film SOI gate driver with integrated bootstrap diodes, over-current protection (OCP), 350/650 mA source/sink current drive, Fault reporting, and Enable for IGBT switches.
Power Switches	
IKW40T120	1200 V IGBT in TRENCHSTOP™ and Fieldstop technology with anti-parallel diode
IKY50N120CH3	1200 V IGBT in Highspeed3 technology with anti-parallel diode
IKQ75N120CT2	1200 V IGBT in TRENCHSTOP™ 2 technology with anti-parallel diode
FP75R12KT3	1200 V EconoPIM™3 module with fast Trench/Fieldstop IGBT3 and Emitter Controlled diode
FP75R12KT4P	1200 V EconoPIM™3 module with fast Trench/Fieldstop IGBT4 and Emitter Controlled 4 diode
FP25R12W1T7_B11	1200 V EasyPIM™ module with TRENCHSTOP™ IGBT7 and Controlled 7 diode
FP35R12W2T7	1200 V EasyPIM™ module with TRENCHSTOP™ IGBT7 and Controlled 7 diode
FP50R12W2T7	EasyPIM™ 2B 1200 V, 50 A three phase input rectifier PIM (Power Integrated Modules) IGBT module with TRENCHSTOP™ IGBT7, Emitter Controlled 7 diode and NTC.
FP75R12N2T7	EconoPIM™ 2 1200 V, 75 A three phase PIM IGBT module with TRENCHSTOP™ IGBT7, Emitter Controlled 7 diode and NTC
FP100R12N3T7	EconoPIM™ 3 1200 V, 100 A three phase PIM IGBT module with TRENCHSTOP™ IGBT7, Emitter Controlled 7 diode and NTC.
FS55MR12W1M1H_B11	EasyPACK™ 1B 1200 V / 55 mΩ sixpack module with CoolSiC™ MOSFET with enhanced generation 1, NTC and PressFIT Contact Technology.
IMW/Z120R350M1H IMW/Z120R220M1H IMW/Z120R140M1H IMW/Z120R090M1H IMW/Z120R060M1H IMW/ZA120R040M1H IMW/Z120R030M1H IMW/ZA120R020M1H IMW/ZA120R014M1H	The CoolSiC™ 1200 V, 350 mΩ ~ 14 mΩ SiC MOSFET in TO247-3 or TO247-4 package build on a state-of-the-art trench semiconductor process optimized to combine performance with reliability. In comparison to traditional silicon (Si) based switches like IGBTs and MOSFETs, the SiC MOSFET offers a series of advantages. These include, the lowest gate charge and device capacitance levels seen in 1200 V switches, no reverse recovery losses of the internal commutation proof body diode, temperature independent low switching losses, and threshold-free on-state characteristic.
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

9 Package details



PACKAGE - GROUP NUMBER:	PG-DSO-16-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.25	2.35
A1	0.10	0.20
A2	2.55	2.65
b	0.32	0.48
c		0.25
D	10.10	10.50
E	10.10	10.50
E1	7.30	7.70
e	1.27	
L	0.50	0.90
θ	0°	8°

1) DOES NOT INCLUDE PLASTIC OR METAL PRUTRUSION OF 0.15 MAX. PER SIDE
2) DOES NOT INCLUDE DAMBAR PROTRUSION OF 0.1 MAX.

Figure 41 300mil 16 leads PG-DSO-16-U02

10 Part marking information

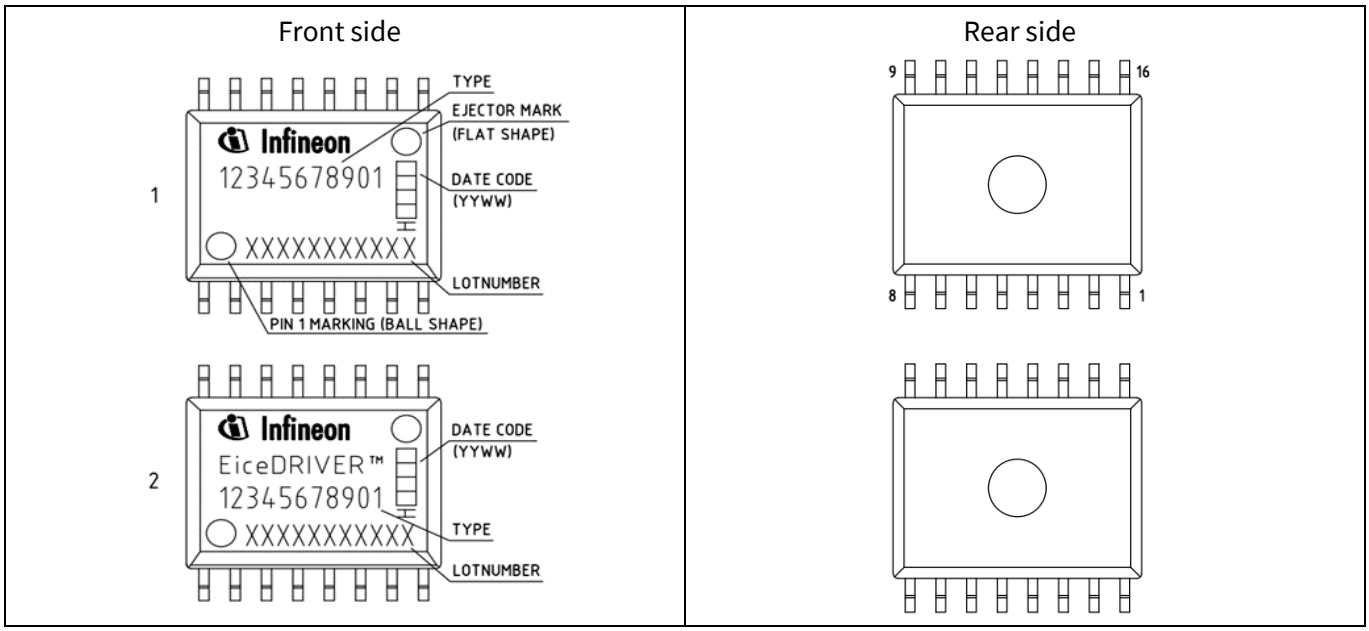


Figure 42 Marking information PG-DSO-16-U02

11 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:
Understanding HVIC Datasheet Specifications
HV Floating MOS-Gate Driver ICs
Use Gate Charge to Design the Gate Drive Circuit for SiC MOSFETs and IGBTs
Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:
Using Monolithic High Voltage Gate Drivers
Alleviating High Side Latch on Problem at Power Up
Keeping the Bootstrap Capacitor Charged in Buck Converters
Managing Transients in Control IC Driven Power Stages
Simple High Side Drive Provides Fast Switching and Continuous On-Time

11.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

12 Revision history

Document version	Date of release	Description of changes
1.0	March 07, 2023	Final Datasheet
1.1	March 16, 2023	Updated the photo of package
1.2	April 18, 2023	Figure 9, OCP threshold changed, Changed, V_{RF+} to V_{IH} for the fomula of t_{FLTCLR} calculation
1.3	September 6, 2023	Created the new paragraph “Temperature trend charts”

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