Navitas Energy • Efficiency • Sustainability **GaNFast™** **NV6269M**

Half Bridge GaNFast™ Power IC
with GaNSense™ Technology

1. Features

GaNFast™ Power IC

- Wide V_{CC} range (10 to 24 V)
- 3.3, 5, 12 V PWM input compatible
- Floating high-side with internal level shift
- Two independent logic inputs with hysteresis
- Integrated high-side bootstrap
- Shoot-through protection
- Turn-on dV/dt slew rate control (low-side and high-side)
- Slow high- & low-side turn-off dV/dt rate for EMI filter reduction
- 800 V transient voltage rating
- 650 V continuous voltage rating
- 70 mΩ high-side FET, 70 mΩ low-side FET
- Zero reverse recovery charge
- 2 KV ESD Rating (HBM)
- 500 kHz operation

GaNSense™ Technology

- Integrated loss-less current sensing
- Over-current protection
- Over-temperature protection
- Autonomous low-current standby mode
- Auto-standby enable input

Small, low profile SMT QFN

- 8x10 mm footprint, 0.85 mm profile
- Minimized package inductance
- Enlarged cooling pads

Sustainability

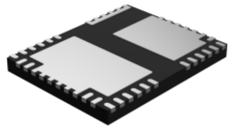
- RoHS, Pb-free, REACH-compliant
- Up to 40% energy savings vs Si solutions
- System level 4kg CO_2 Carbon Footprint reduction

Product Reliability

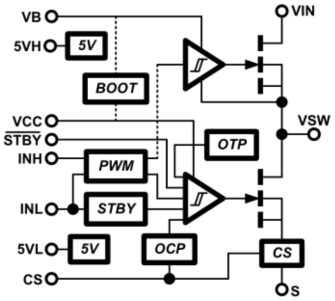
- 20-year warranty

2. Topologies / Applications

- Motor Drive



QFN 8 x 10 mm



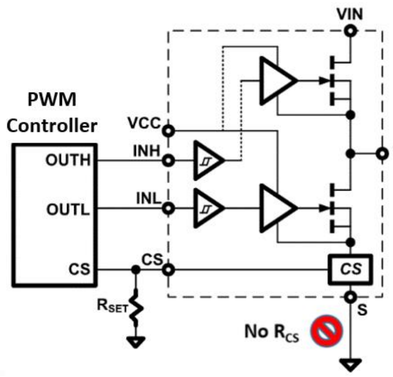
Simplified schematic

3. Description

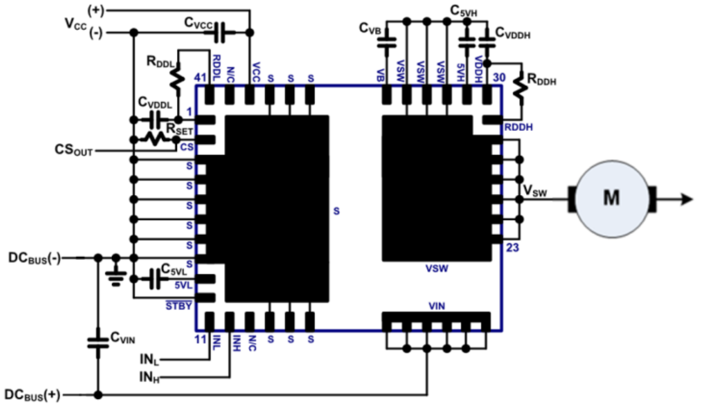
This half-bridge GaNFast™ power IC integrates high performance eMode GaN FETs with integrated gate drive, control and protection to achieve unprecedented high-frequency and high efficiency operation. GaNSense™ technology is also integrated which enables real-time, accurate sensing of voltage, current and temperature to further improve performance and robustness not achieved by any discrete GaN or discrete silicon device. GaNSense™ enables integrated loss-less current sensing which eliminates external current sensing resistors and increases system efficiency. GaNSense™ also enables short circuit and over-temperature protection to increase system robustness, while auto-standby mode increases light, tiny & no-load efficiency. These GaN ICs combine the highest dV/dt immunity, high-speed integrated drive and thermally optimized, low-inductance, QFN packaging to enable designers to achieve simple, quick, and reliable solutions. Navitas' GaN IC technology extends the capabilities of 1-ph and 3-ph motor drive applications with very high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

4. Typical Application Circuits

Loss-less Current Sensing



Motor Drive



5. Table of Contents

6. Specifications

6.1. Absolute Maximum Ratings (1) (with respect to PGND unless noted)

SYMBOL	PARAMETER	MAX	UNITS
V_{IN}	HV input	0 to +650	V
$V_{SW(CONT)}$	Switch Node Continuous Voltage Rating	-7 to +657	V
$V_{SW(TRAN)}$ (2)	Switch Node Transient Voltage Rating	-10 to +800	V
I_{DSL} @ T_C=100ºC	Continuous Output Current (Low-side FET)	14	A
I_{DSL} PULSE@ T_C=25ºC	Pulsed Output Current (Low-side FET)	28	A
I_{DSH} @ T_C=100ºC	Continuous Output Current (High-side FET)	14	A
I_{DSH} PULSE@ T_C=25ºC	Pulsed Output Current (High-side FET)	28	A
V_B (to V_{SW})	High-side Gate Driver Bootstrap Rail	30	V
V_{DDH} (to V_{SW})	High-side Gate Drive Supply Voltage	7	V
V_{5VH} (to V_{SW})	High-side 5V Supply Voltage	6	V
V_{CC}	Supply Voltage	30	V
V_{DDL}	Low-side Drive Supply Voltage	7	V
R_{DDL}	Low-side Gate Drive Supply Resistor Setting Input	7	V
V_{5VL}	Low-side 5V Supply Voltage	6	V
$V_{\overline{STBY}}$	Auto-Standby Mode Pin Voltage	-0.6 to +20 or V_{CC}	V
V_{INH}, V_{INL}	PWM Input Pin Voltages	-0.6 to +20 or V_{CC}	V
V_{CS}	CS Pin Voltage	5.3	V
T_J	Junction Temperature	-55 to 150	ºC
T_{STOR}	Storage Temperature	-55 to 150	ºC

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS\ (TRAN)}$ rating allows for surge ratings during non-repetitive events that are <100us (for example start-up, line interruption). $V_{DS\ (TRAN)}$ rating allows for repetitive events that are <300ns, with 80% derating required (for example repetitive leakage inductance spikes).

6.2. Recommended Operating Conditions(3)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	10	15	24	V
V_{INH}, V_{INL}	PWM Input Pin Voltage	0	5	15 or V_{CC}	V
$V_{\overline{STBY}}$	Auto-Standby Mode Pin Voltage	0	5	15 or V_{CC}	V
R_{DDL}	Low-side gate drive turn-on current set resistor	300		1,500	Ω
R_{DDH}	High-side gate drive turn-on current set resistor	300		1,500	Ω
Dead-time	Between INH and INL input	500			ns
T_J	Operating Junction Temperature	-40		125	ºC

(3) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.

6.3. ESD Ratings

SYMBOL	PARAMETER	MAX	UNITS
HBM	Human Body Model (per JS-001-2014)	2,000	V
CDM	Charged Device Model (per JS-002-2014)	500	V

6.4. Thermal Resistance

SYMBOL	PARAMETER	TYP	UNITS
$R_{\theta JC}$ (4)	Junction-to-Case	0.98	ºC/W
$R_{\theta JA}$	Junction-to-Ambient	40	ºC/W

(4) R_{θ} measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

6.5. Electrical Characteristics

Typical conditions: V_{IN}=400V, V_{CC} =15V, F_{SW}=50KHz, T_{AMB}=25ºC, I_D=7A (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC}, V_{DDL}, V_B and V_{DDH} Supply Characteristics						
V_{CCUV+}	V_{CC} UVLO Rising Threshold	8.0	8.6	9.3	V	
V_{CCUV-}	V_{CC} UVLO Falling Threshold		7.4		V	
$I_{QCC-STBY}$	V_{CC} Standby Current	200	400	560	µA	$\overline{STBY}$ = 0 V, V_{SW} >=V_{CC}
I_{QCC}	V_{CC} Quiescent Current		2.5		mA	V_{INL} = V_{INH} = 0 V, $\overline{STBY}$ = 5 V
I_{QCC-SW}	V_{CC} Operating Current		5		mA	F_{SW} = 50 KHz (INL and INH @ 50% Duty cycle), V_{SW} = 0 V
V_{DDL}	V_{DD} Supply Voltage	5.9	6.1	6.6	V	V_{CC} = 15 V, V_{INL} = VI_{NH} = 0 V
V_{DDLUV+}	V_{DDL} UVLO Rising Turn-On Threshold		4.9		V	
$V_{DDLUV-HYS}$	V_{DDL} UVLO Hysteresis		0.6		V	
V_{BUV+}	V_B UVLO Rising Threshold (V_B – V_{SW})	8.0	8.6	9.3	V	
V_{BUV-}	V_B UVLO Falling Threshold (V_B – V_{SW})		7.8		V	
I_{QVB}	V_B Quiescent Current		1.7		mA	V_{INH} = V_{INL} = 0 V, V_{SW} = 0 V, V_B = 15 V
V_{DDH}	V_{DD} Supply Voltage	5.9	6.1	6.6	V	V_B = 15 V
5V Output (5V pin)						
V_{5VL}, V_{5VH}	5V Output Voltage	4.4	5.1	5.5	V	
Input Logic Characteristics (INL,INH, $\overline{STBY}$)						
$V_{LOGIC-H}$	Input Logic High Threshold (rising edge)		2.5	2.8	V	
$V_{LOGIC-L}$	Input Logic Low Threshold (falling edge)	1.1	1.2		V	
$V_{LOGIC-HYS}$	Input Logic Hysteresis		1.4		V	
Switching Characteristics						
F_{SW}	Switching Frequency			500	kHz	R_{DDH}=R_{DDL}=300 Ω
t_{PW}(1)	Pulse width	0.05			us	
t_{ONHS}	Prop Delay (IN_H from Low to High, V_{SW} pulled to V_{IN})		55		ns	Fig. 3
t_{OFFHS}	Prop Delay (IN_H from High to Low, V_{SW} tri-stated)		120		ns	Fig. 3
t_{ONLS}	Prop Delay (IN_L from Low to High, V_{SW} pulled to P_{GND})		58		ns	Fig. 4
t_{OFFLS}	Prop Delay (IN_L from High to Low, V_{SW} tri-stated)		120		ns	Fig. 4
High side turn on dvdt	High side turn-on dV/dt slew rate		6		V/ns	R_{DDH} = 300 Ω
Low side turn on dvdt	Low side turn-on dV/dt slew rate		4		V/ns	R_{DDL} = 300 Ω

(1) Min Pulse width limitation is only for the high side FET

6.6. Electrical Characteristics (2, cont.)

Typical conditions: V_{DS}=400V, V_{CC} =15V, F_{SW}=50KHz, T_{AMB}=25ºC, I_D=7A (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Current Sense Characteristics (CS pin)						
I_{CS}	CS Pin Output Current	1.16	1.25	1.34	mA	V_{INL} = 5 V, I_{DS} = 11 A
Offset	CS Output Offset		+18		µA	V_{INL} = 5 V, I_{DS} = 0 A
t_{CSDLY}	CS Pin Delay (from I_{DS} to V_{CS}, at 10% rated current)		55		ns	di/dt = 40 A/us, R_{SET} = 400 Ohm, C_{CS} = 25 pF
Over-Current Protection						
OCP_{TH}	OCP Threshold Voltage (V_{CS} Pin)		1.9		V	
Standby Mode Characteristics						
t_{TO_STBY}	Time Out Delay Entering Standby Mode		90		µs	V_{INL} = 0 V
t_{ON_FP}	First Pulse Propagation Delay		460	650	ns	V_{INL} = 5 V pulse, $\overline{STBY}$ = 0 V
Over-Temperature Protection						
T_{OTP+}	OTP Shutdown Threshold		165		ºC	
T_{OTP_HYS}	OTP Restart Hysteresis		60		ºC	
Bootstrap FET Characteristics						
I_{BOOT}	Bootstrap Charging Current		2		A	V_{CC} = 12 V, V_B = 0 V, V_{SW} = 0 V

6.7. Electrical Characteristics (3, cont.)

Typical conditions: V_{DS}=400V, V_{CC} =15V, F_{SW}=50KHz, T_{AMB}=25ºC, I_D=7A (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	Low side GaN FET Characteristics					
I_{DSS}	Drain-Source Leakage Current		0.2	25	µA	V_{DS} = 650 V, V_{INL} = 0 V
I_{DSS}	Drain-Source Leakage Current, TC =150 ºC		10		µA	V_{DS} =650V, V_{INL} =0V, T_C =150 ºC
$R_{DS(ON)}$	Low-side FET Drain-Source Resistance		70	98	mΩ	V_{INL} = 5 V, I_D = 7 A
V_{SD}	Source-Drain Reverse Voltage		3.2	5	V	V_{INL} = 0 V, V_{INH} = 0 V, I_{SD} = 7 A
Q_{OSS}	Output Charge		41.5		nC	V_{DS} = 400 V, V_{INL} = 0V, V_{INH} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	V_{DS} = 400 V
C_{OSS}	Output Capacitance		59		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(er)}$ (1)	Effective Output Capacitance, Energy Related		75.5		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(tr)}$ (2)	Effective Output Capacitance, Time Related		103.8		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
	High side GaN FET Characteristics					
I_{DSS}	Drain-Source Leakage Current		0.2	25	µA	V_{DS} = 650 V, V_{INL} = 0 V
I_{DSS}	Drain-Source Leakage Current, TC =150 ºC		10		µA	V_{DS} =650V, V_{INL} =0V, T_C =150 ºC
$R_{DS(ON)}$	High-side FET Drain-Source Resistance		70	98	mΩ	V_{INL} = 5 V, I_D = 7 A
V_{SD}	Source-Drain Reverse Voltage		3.2	5	V	V_{INL} = 0 V, V_{INH} = 0 V, I_{SD} = 7 A
Q_{OSS}	Output Charge		37.5		nC	V_{DS} = 400 V, V_{INL} = 0V, V_{INH} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	V_{DS} = 400 V
C_{OSS}	Output Capacitance		50		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(er)}$ (1)	Effective Output Capacitance, Energy Related		66.6		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(tr)}$ (2)	Effective Output Capacitance, Time Related		93.8		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V

(1) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(2) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

6.8. Switching Waveforms

(T_C = 25 ºC unless otherwise specified)

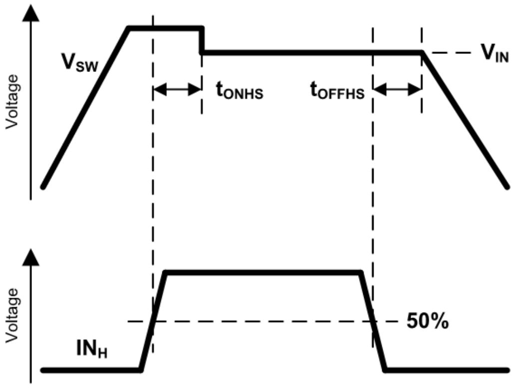


Fig. 1. Propagation Delay ZVS Mode $t_{ONHS/OFFHS}$

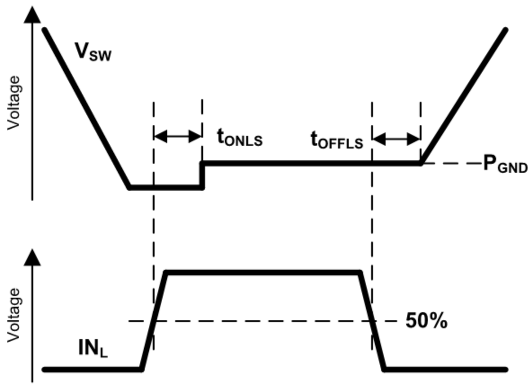


Fig. 2. Propagation Delay ZVS Mode $t_{ONLS/OFFLS}$

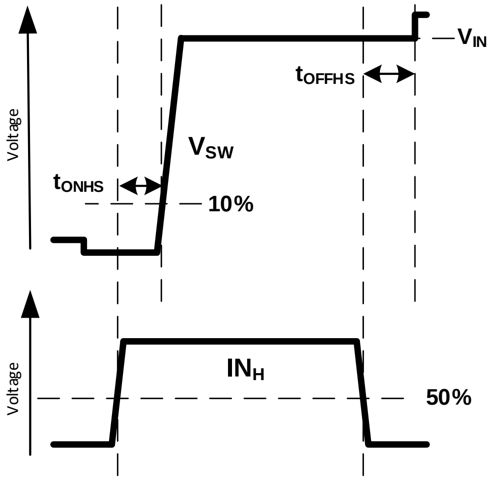


Fig. 3. Propagation Delay Hard Switching $t_{ONHS/OFFHS}$

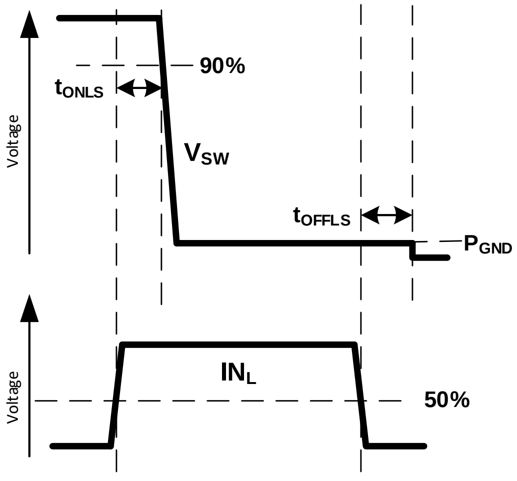


Fig. 4. Propagation Delay Hard Switching $t_{ONLS/OFFLS}$

6.9. Characteristic Graphs

(GaN FET, T_C = 25 ºC unless otherwise specified)

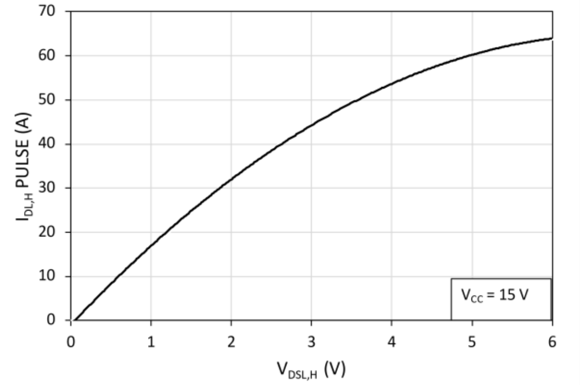


Fig. 5. Pulsed Drain current ($I_{DSL,H}$ PULSE) vs. drain-to-source voltage ($V_{DSL,H}$) at T = 25 °C

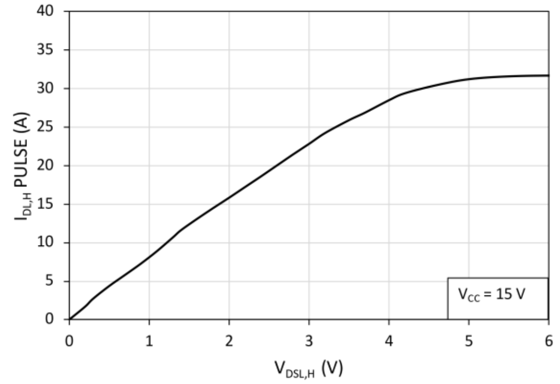


Fig. 6. Pulsed Drain current ($I_{DSL,H}$ PULSE) vs. drain-to-source voltage ($V_{DSL,H}$) at T = 125 °C

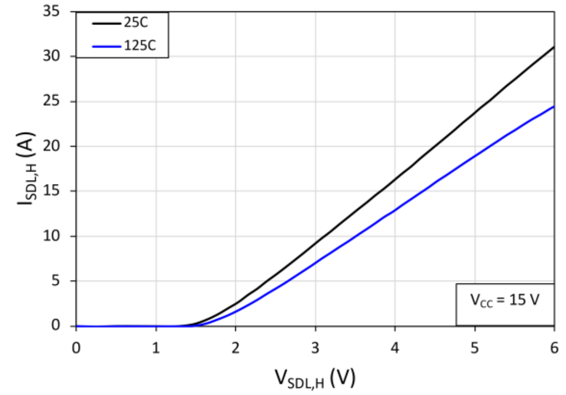


Fig. 7. Source-to-drain reverse conduction voltage ($I_{SDL,H}$)

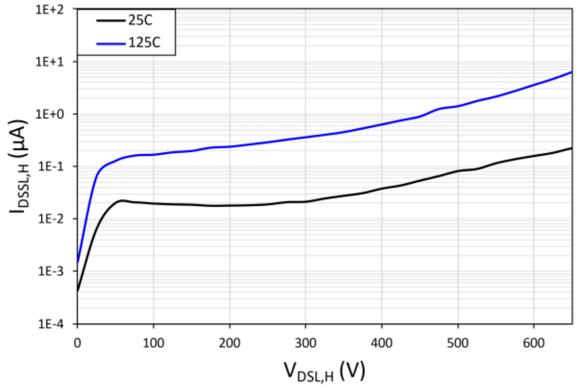


Fig. 8. Drain-to-source leakage current ($I_{DSSL,H}$) vs.drain-to-source voltage ($V_{DSL,H}$)

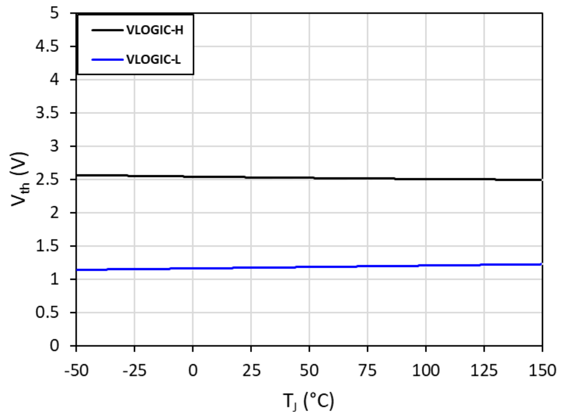


Fig. 9. $V_{LOGIC-H}$ and $V_{LOGIC-L}$ vs. junction temperature (T_J)

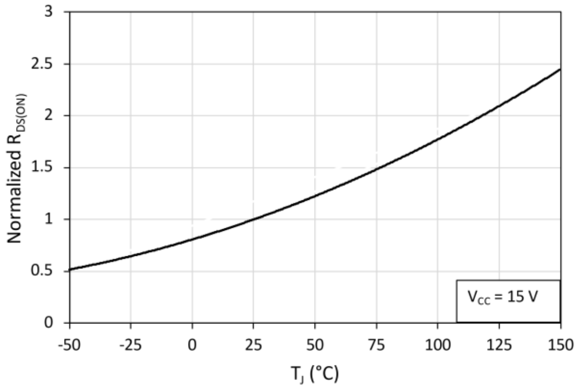


Fig. 10. Normalized on-resistance ($R_{DSL,H(ON)}$) vs. junction temperature (T_J)

Characteristic Graphs (Cont.)

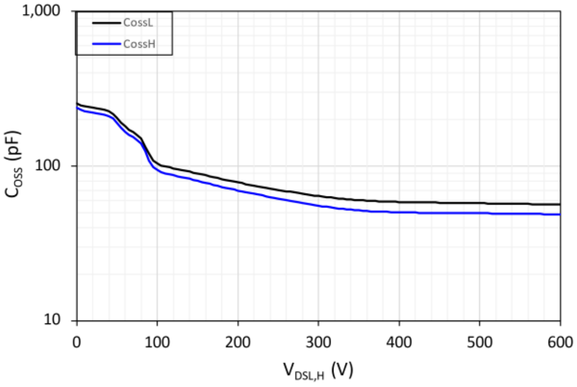


Fig. 11. Output capacitance ($C_{OSSL,H}$) vs. drain-to-source voltage ($V_{DSL,H}$)

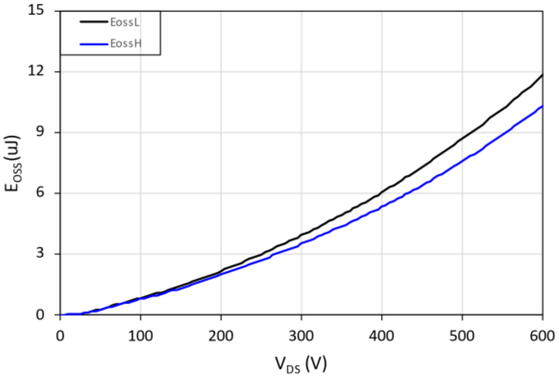


Fig. 12. Energy stored in output capacitance ($E_{OSSL,H}$) vs. drain-to-source voltage ($V_{DSL,H}$)

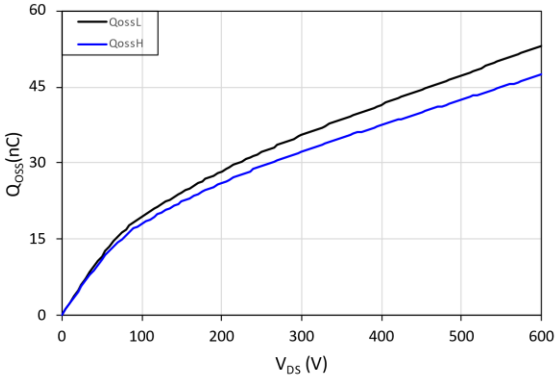


Fig. 13. Charge stored in output capacitance (Q_{OSS}) vs. drain-to-source voltage (V_{DS})

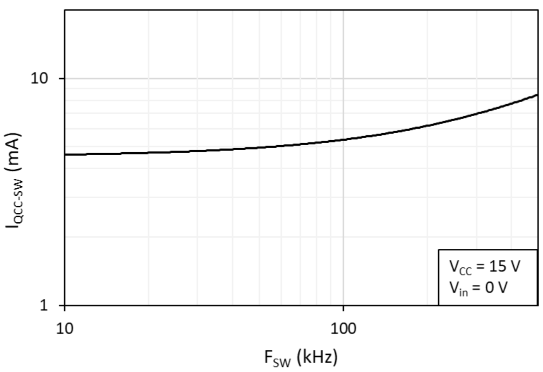


Fig. 14. V_{CC} operating current (I_{QCC-SW}) vs. operating frequency (F_{SW})

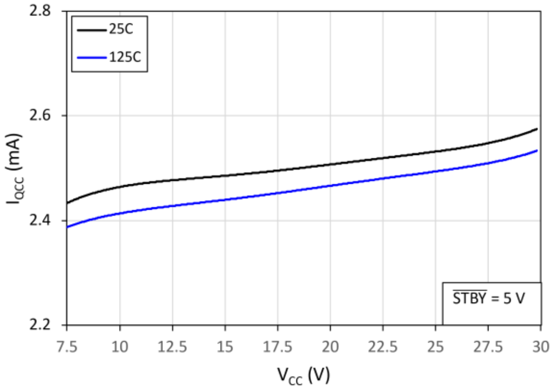


Fig. 15. V_{CC} quiescent current (I_{QCC}) vs. supply voltage (V_{CC})

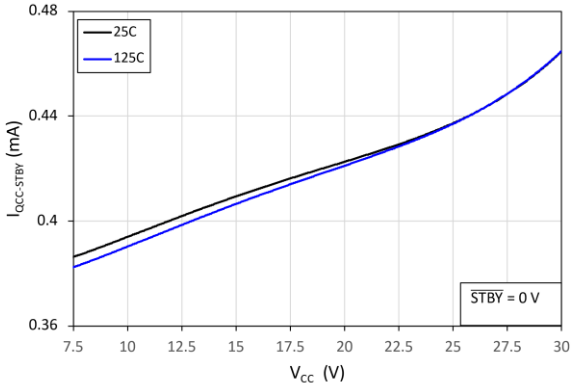


Fig. 16. V_{CC} stand-by quiescent current (I_{QCC}) vs. supply voltage (V_{CC})

Characteristic Graphs (Cont.)

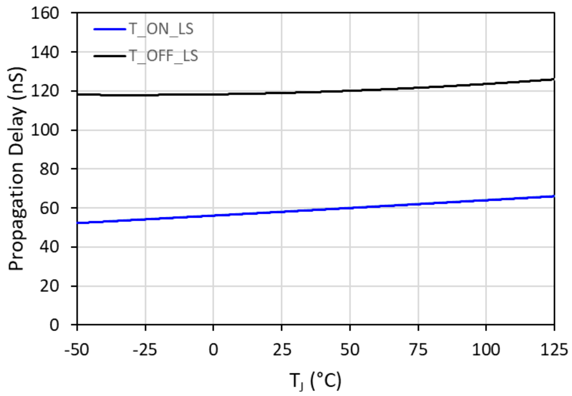


Fig. 17. Propagation delay (T_{ON} and T_{OFF}) vs. junction temperature (T_J) – low side

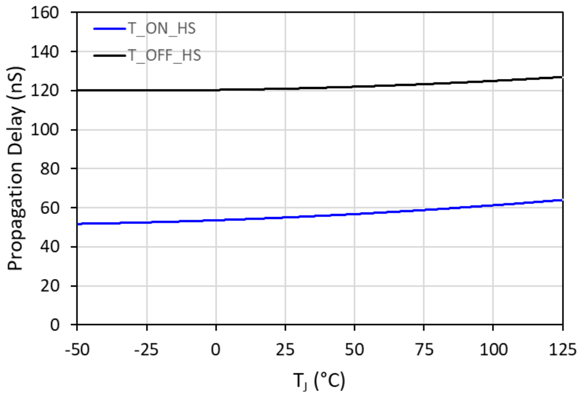


Fig. 18. Propagation delay (T_{ON} and T_{OFF}) vs. junction temperature (T_J) – high side

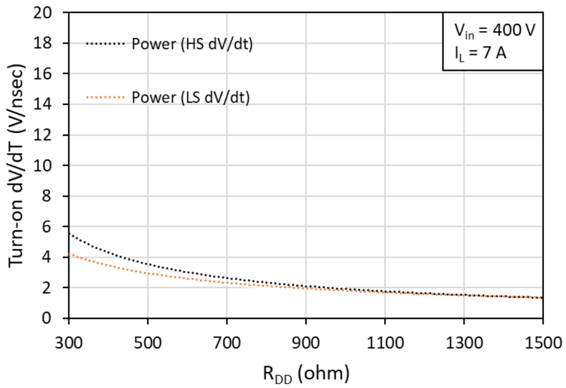


Fig. 19. Slew rate (dV/dt) vs. gate drive turn-on current set resistance (R_{DDL}) at T = 25 °C

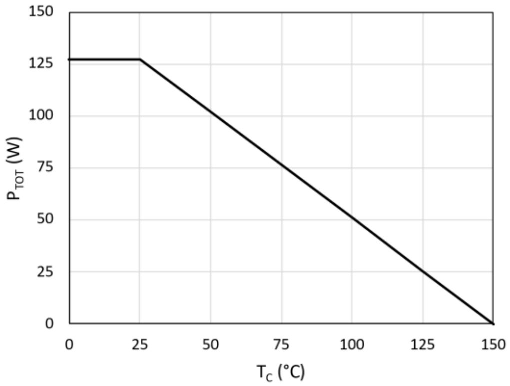


Fig. 20. Power dissipation (P_{TOT}) vs. case temperature (T_C)

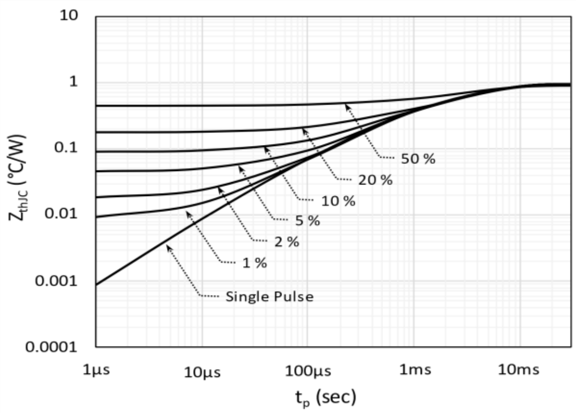


Fig. 21. Max. thermal transient impedance (Z_{thJC}) vs. pulse width (t_P)

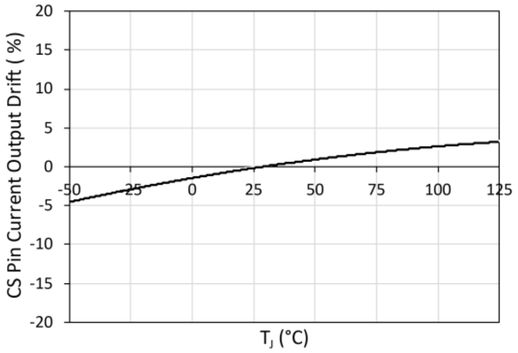


Fig. 22. CS Pin Current Output Drift vs. case temperature (T_C)

7. Pin Configurations and Functions

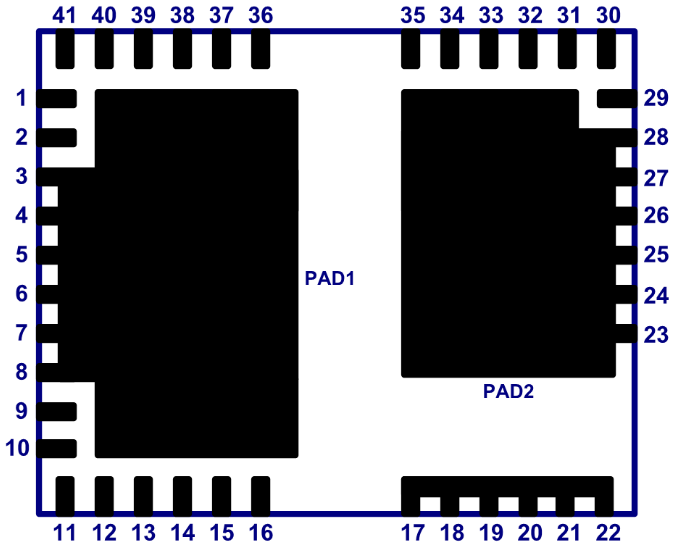


Fig. 23 Package Top View

Pin		I/O(1)	Description
Number	Symbol		
3-8,14-16,36-38 (and PAD1)	P_{GND}	G	Power ground
1	V_{DDL}	P	Low-side drive supply
2	CS	O	GaN FET IDS current sensing set pin. Internal current source and external resistor R_{SET} sets current measurement level. Connect resistor from CS to SGND.
9	$5V_L$	P	Low-side 5 V supply
10	STBY	I	Auto-standby enable input (0=ON)
11	IN_L	I	Low-side drive input
12	IN_H	I	High-side drive input
13, 40	N/C		No connect
17 – 22	V_{IN}	P	HV input
23-28,32-34 (and PAD2)	V_{SW}	O	Half-bridge switch node
29	R_{DDH}	I	High-side gate drive turn-on current set resistor (using R_{DD} resistor connected from R_{DDH} pin to V_{DDH} pin)
30	V_{DDH}	P	High-side drive supply
31	$5V_H$	P	High-side 5 V supply
35	V_B	P	High-side gate driver bootstrap rail
39	V_{CC}	P	IC supply voltage
41	R_{DDL}	I	Low-side gate drive turn-on current set resistor (using R_{DD} resistor connected from R_{DDL} pin to V_{DDL} pin)

(1) I = Input, O = Output, P = Power, G = Ground, NC = No Connect

8. Functional Description

The functional description contains additional information regarding the IC operating modes and pin functionality.

8.1. GaN Power IC Connections and Component Values

The typical connection diagram for this GaN Half-Bridge IC is shown in Fig. 24. The IC pins include the drain of the high-side GaN power FET (V_{IN}), the half-bridge mid-point switched node (V_{SW}), the source of the low-side GaN power FET and IC GND (P_{GND}), low-side IC supply (V_{CC}), low-side gate drive supply (V_{DDL}), low-side turn-on dV/dt control (R_{DDL}), low-side 5V supply ($5V_L$), low-side referenced PWM inputs (IN_L, IN_H), low-side current sensing output (CS), auto-standby enable input ($\overline{STBY}$), high-side supply (V_B), high-side gate drive supply (V_{DDH}), and high-side 5V supply ($5V_H$). The external low-side components around the IC include V_{CC} supply capacitor (C_{VCC}) connected between V_{CC} pin and P_{GND}, V_{DDL} supply capacitor (C_{VDDL}) connected between V_{DDL} pin and P_{GND}, turn-on dV/dt set resistor (R_{DDL}) connected between V_{DDL} pin and R_{DDL} pin, current sense amplitude set resistor (R_{SET}) connected between CS pin and P_{GND}, 5V supply capacitor (C_{5VL}) connected between $5V_L$ pin and P_{GND}, and the auto-standby enable pin ($\overline{STBY}$) connected to P_{GND} to enable auto-standby mode or connected to $5V_L$ to disable auto-standby mode. The external high-side components around the IC include V_B supply capacitor (C_{VB}) connected between V_B pin and V_{SW}, V_{DDH} supply capacitor (C_{VDDH}) connected between V_{DDH} pin and V_{SW}, turn-on dV/dt set resistor (R_{DDH}) connected between V_{DDH} pin and R_{DDH} pin, and 5V supply capacitor (C_{5VH}) connected between $5V_H$ pin and V_{SW}. The high side V_B, $5V_H$ and V_{DDH} bypass capacitors must be chosen carefully to accommodate various system considerations such as high side wake up time, high side hold up time and standby power.

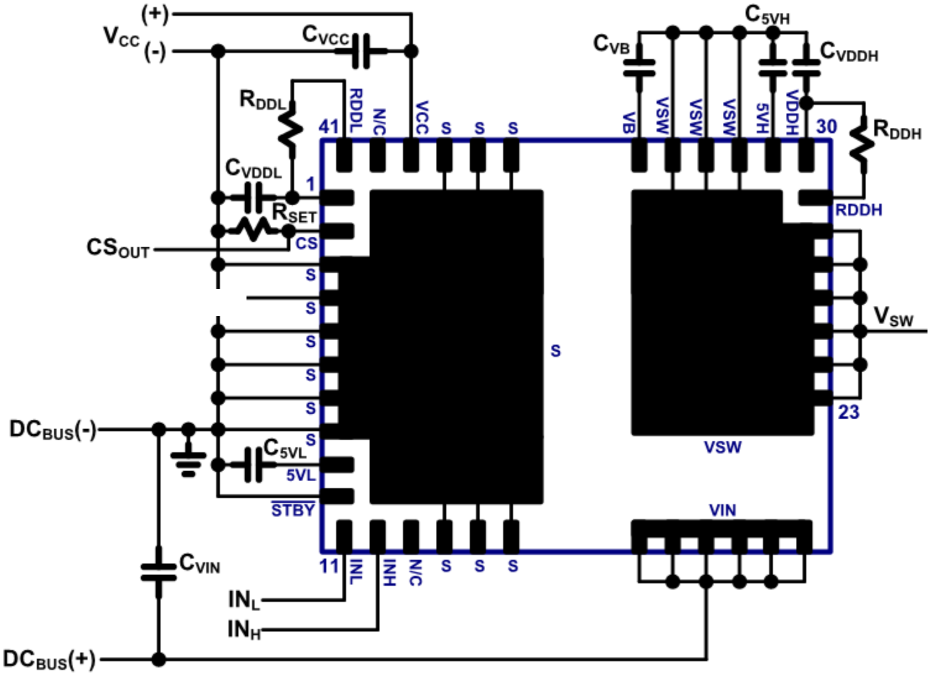


Fig. 24. IC connection diagram

The following table (Table I) shows the recommended component values (typical only) for the external components connected to the pins of this Half-Bridge GaN power IC. These components should be placed as close as possible to the IC. Please see PCB Layout Guidelines for more information.

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} supply capacitor	0.1	µF
C_{VDD}	V_{DD} supply capacitor	0.01	µF
R_{DDL}	Low-side gate drive turn-on current set resistor	300	Ω
R_{SET}	Current sense amplitude set resistor	See Section 8.6 , Equation 1	Ω
C_{5VL}	$5V_L$ supply capacitor	0.022	µF
C_{VB}	V_B supply capacitor	0.01	µF
C_{VDDH}	V_{DDH} supply capacitor	0.01	µF
R_{DDH}	High-side gate drive turn-on current set resistor	300	Ω
C_{5VH}	$5V_H$ supply capacitor	0.01	µF

Table I. Recommended component values (typical only).

8.2. UVLO Mode

This GaN Power IC includes under-voltage lockout (UVLO) circuits for both the high side and low side power supplies for properly disabling all the internal circuitry while ensuring that the gates of power FETs are kept in their OFF state. While V_{CC} is below the V_{CCUV+} threshold (8.6V, typical) and V_{DDL} is below the V_{DDLUV+} threshold (4.9V, typical) the low side power FET gate is kept in its OFF state while an analogous situation is applicable for the high side power FET gate while V_B and V_{DDH} are below their respective UVLO thresholds. As the V_{CC} supply voltage increases (Fig. 25), the voltage at the V_{DDL} pin also increases and exceeds V_{DDUV+}. V_{DDL} voltage continues to increase with V_{CC} until it gets limited to a constant voltage level (6.1V, typical) by the internal regulator. The V_{CC} voltage continues to increase until it exceeds V_{CCUV+} and the IC enters Normal Operating Mode. The gate drive is enabled and the control signal at the IN_L input turns the internal low side power FET on and off normally. While the low side power FET is ON the bootstrap capacitor (V_B) is charged through the internal bootstrap FET. Analogous to the low side situation, as V_B and consequently V_{DDH} rise above their respective UVLO thresholds the high side gate driver is enabled and can respond to IN_H. During system power off, when V_{CC} decreases below the V_{CCUV-} threshold (7.4V, typical), the low side gate drive is disabled, and the IC enters UVLO Mode.

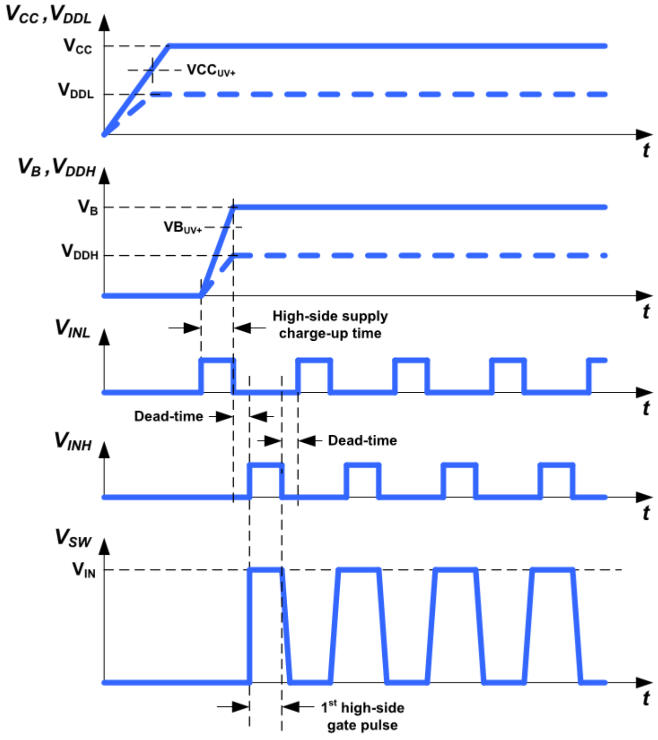


Fig. 25. UVLO Mode timing diagram

8.3. Normal Operating Mode

During normal operating mode, V_{CC} is set at a sufficient level (15 V typical) by the auxiliary power supply of the power converter, and V_B is at a sufficient level (as set by V_{CC} and the internal bootstrap circuit). The PWM input signals at the IN_L and IN_H pins turn the gates of the internal high- and low-side GaN power FETs on and off at the desired duty-cycle, frequency, and dead-time. The input logic signal at the IN_L pin turns the low-side half-bridge power FET on and off (0=OFF, 1=ON), and the input logic signal at the IN_H pin turns the high-side half-bridge power FET on and off (0=OFF, 1=ON). As the PWM inputs are turned on and off in a complementary manner each switching cycle, the V_{SW} pin (half-bridge mid-point) is then switched between P_{GND} (IN_L=1, IN_H=0) and V_{IN} (IN_L=0, IN_H=1) at the given frequency and duty-cycle (Fig. 26). This GaN Half-Bridge IC includes shoot-through protection circuitry that prevents both power FETs from turning on simultaneously. This IC also includes an internal bootstrap FET for supplying the high-side circuitry. The bootstrap FET is enabled during normal operating mode and is turned on each PWM switching cycle only when the IN_L pin is 'HIGH' and the low-side power FET is on. This will allow the V_B capacitor to be charged up each switching cycle for properly maintaining the necessary floating high-side supply voltage. The V_B capacitor value should be sized correctly such that the V_B voltage is maintained at a sufficient level above UVLO- during normal operation. Should the V_B-V_{SW} voltage decrease below the VB_{UV-} falling UVLO threshold

(7.8 V typical) at any time, then the high-side GaN power FET will turn off and become disabled until V_B-V_{SW} increases again above the VB_{UV+} rising threshold (8.6 V typical).

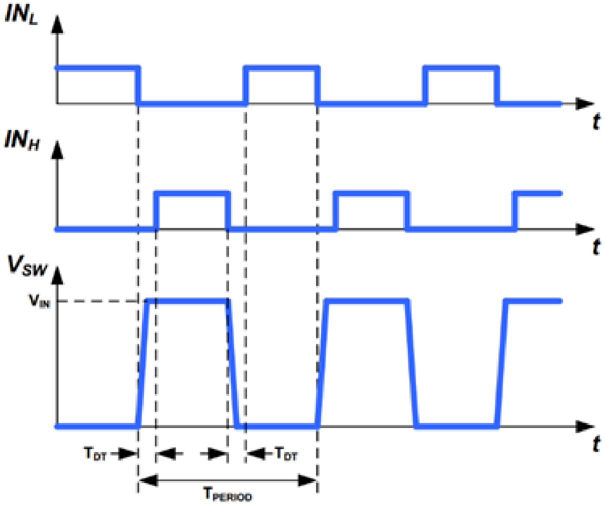


Fig. 26. Normal operating mode timing diagram

8.4. Low Power Standby Mode

This GaN Half-Bridge IC includes an autonomous low power standby mode for disabling the IC and reducing the V_{CC} current consumption. During normal operating mode, the PWM input signals at the IN_L and IN_H pins turn the gates of the internal high- and low-side GaN power FETs on and off at the desired duty-cycle, frequency, and dead-time. If the input pulses at the IN_L pin stop and stay below the lower V_{INL-} turn-off threshold (1.1V, typical) for the duration of the internal timeout standby delay (t_{TO_STBY}, 90usec, typical), then the IC will automatically enter low power standby mode (Fig. 27). This will disable the gate drive and other internal circuitry and reduce the V_{CC} supply current to a low level (300uA, typical). When the IN_L pulses restart, the IC will wake up after a delay (typically around 490ns) at the first rising edge of the IN_L input and enter normal operating mode again. To enable auto standby mode, the $\overline{\text{STBY}}$ pin should be connected to Source (set low). To disable auto standby mode, $\overline{\text{STBY}}$ pin should be connected to the $5V_L$ pin 7 (set high).

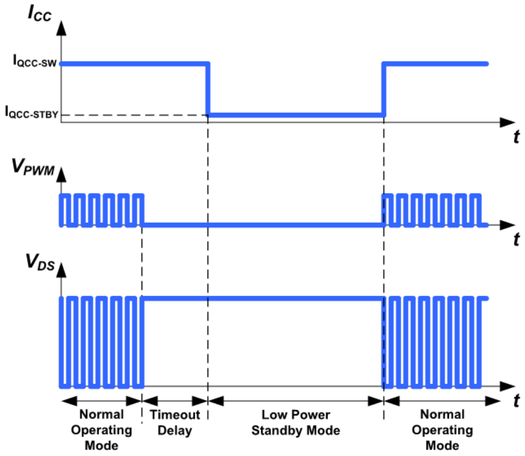


Fig. 27. Autonomous Low Power Standby Mode timing diagram

8.5. Programmable Turn-on dV/dt Control

During first start-up pulses or during hard-switching conditions, it is desirable to limit the slew rate (dV/dt) of the drain of the power FET during turn-on. This is necessary to reduce EMI or reduce circuit switching noise. To program the turn-on dV/dt rate of the internal power FET, a resistor ($R_{DDL,H}$) is placed in between the $V_{DDL,H}$ pin and the $R_{DDL,H}$ pin. This resistor ($R_{DDL,H}$) sets the turn-on current of the internal gate driver and therefore sets the turn-on falling edge dV/dt rate of the drain of the power FET (Fig. 28). This resistor value should be 300Ω minimum (see Table II).

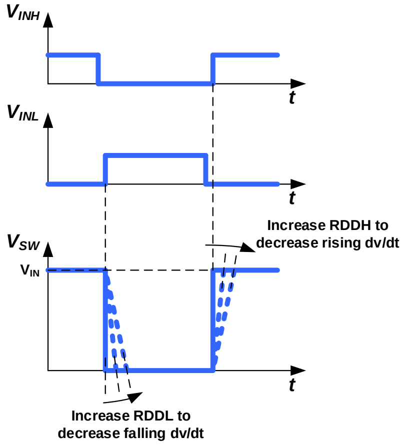


Fig. 28. Turn-on dV/dt slew rate control

SYM	DESCRIPTION	MIN	TYP	MAX	UNITS
$R_{DDL,H}$	$R_{DDL,H}$ resistor	300		1,500	Ω

Table II. Recommended $R_{DDL,H}$ values

8.6. Internal Turn-off dV/dt Control

To reduce EMI and reduce circuit switching noise, it is desirable to limit the turn-off dV/dt slew rate of the drain of the low-side and high-side GaN power FETs. This GaN IC includes low-side and high-side turn-off dV/dt slew rates that are optimized for motor drive applications. The turn-off speed of the low-side and high-side GaN power FETs are internally set to a slow dV/dt rate. This slow turn-off dV/dt rate dramatically reduces conducted and radiated EMI noise across a wide frequency spectrum, especially with motor drive applications where high di/dt and dV/dt induced common mode noise exists due to motor cables. This common mode noise typically requires external common mode filters to reduce EMI but these filters can be reduced or eliminated due to the limited high-side dV/dt slew rate.

8.7. GaNSense^{TM} Technology Loss-Less Current Sensing

For many applications it is necessary to sense the cycle-by-cycle current flowing through the low-side GaN power FET. Existing current sensing solutions require a current sensing resistor to be placed in between the source of the low-side GaN power FET and P_{GND}. This resistor method increases system conduction power losses, creates a hotspot on the PCB, and lowers overall system efficiency. To eliminate this external resistor and hotspot, and increase system efficiency, this GaN Half-Bridge IC includes GaNSense^{TM} Technology for integrated and accurate loss-less current sensing. The current flowing through the internal low-side GaN power FET is sensed internally and then converted to a current at the current sensing output pin (CS). An external resistor (R_{SET}) is connected from the CS pin to the Source (P_{GND}) and is used to set the amplitude of the CS pin voltage signal (Fig. 29). This allows for the amplitude of the CS pin signal to be programmed so it is compatible with different controllers with different current sensing input thresholds.

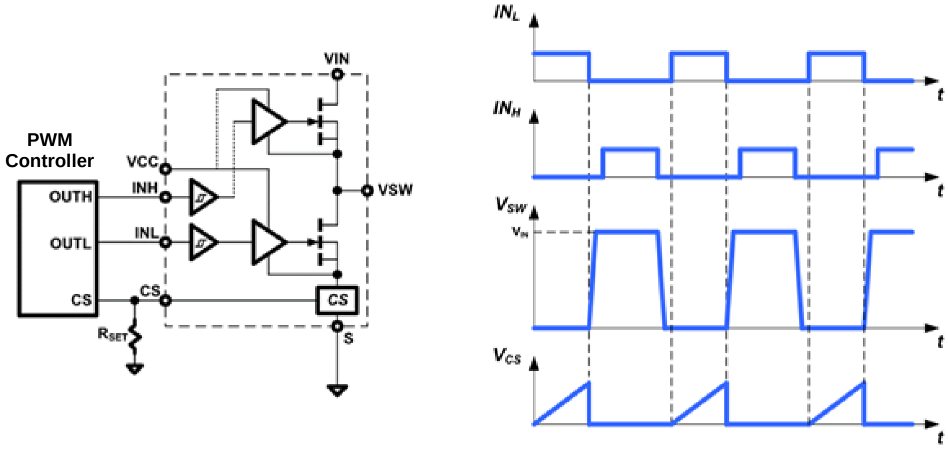


Fig. 29. External resistor sensing vs. GaNSense^{TM} Technology

To select the correct R_{SET} resistor value, the following equation (Equation 1) can be used. This equation uses the equivalent desired external current sensing resistor value (R_{CS}), together with the gain of the internal sensing circuitry, to generate the equivalent R_{SET} resistor value. This R_{SET} value will give then give the correct voltage level at the CS pin to be compatible with the internal current sensing threshold of the system controller.

$$I_{OUT}\ Ratio = \frac{I_{DS}}{I_{CS}} = \frac{11A}{0.00125A} = 8800$$

$$R_{SET} = 8800 * R_{CS}$$

Equation 1. R_{SET} resistor value equation

When comparing GaNSense^{TM} Technology versus existing external current sensing resistor method (Fig. 30), the total ON resistance, $R_{ON(TOT)}$, can be substantially reduced, and the external R_{CS} resistors can be eliminated. For the example shown, $R_{ON(TOT)}$ is reduced from 140m to 70m. This gives lower R_{CS} power losses and thermals, eliminates external op-amp and comparator sensing circuits, reduces component count, and lowers overall system cost.

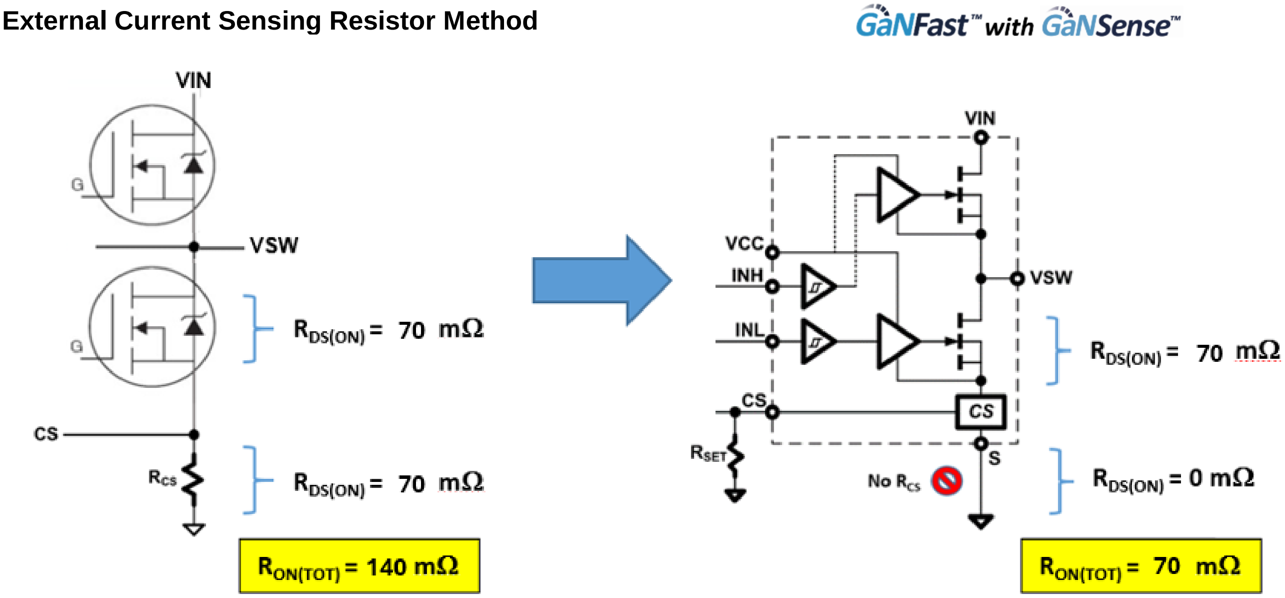


Fig. 30. External current sensing resistor vs. GaNSense^{TM} Technology

8.8. Over Current Protection (OCP)

This GaN Power IC includes cycle-by-cycle over-current detection and protection (OCP) circuitry to protect the GaN power FET against high current levels. During the on-time of each switching cycle, should the peak current exceed the internal OCP threshold (1.9V, typical), the internal gate drive will turn the GaN power FET off quickly and truncate the on-time period to prevent damage occurring to the IC. The IC will then turn on again at the next PWM rising edge at the start of the next on-time period (Fig. 31). This OCP protection feature will self-protect the IC each switching cycle against fast peak over current events and greatly increase the robustness and reliability of the system. The actual peak current threshold can be calculated using Equation 2 and is a function of the internal current-sensing ratio and the external R_{SET} resistor. The internal OCP threshold (1.9V, typical) is much higher than the OCP thresholds of many popular QR, ACF and PFC controllers. This ensures good compatibility of this IC with existing controllers without OCP threshold conflicts.

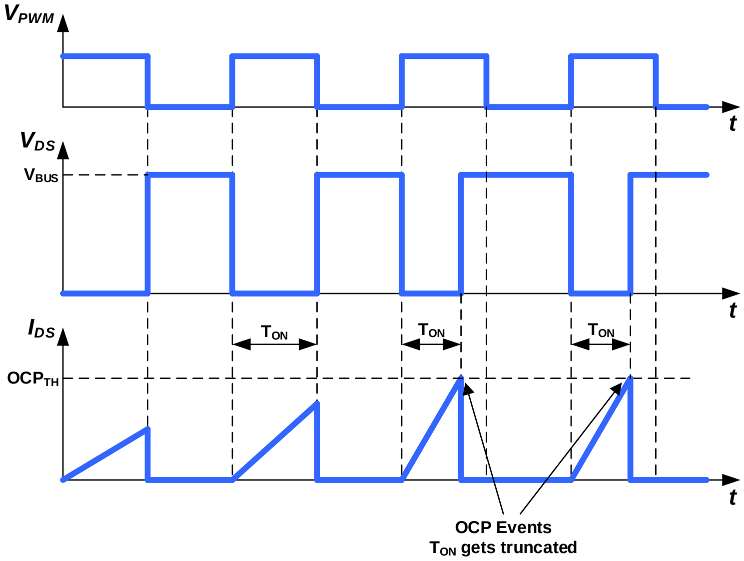


Fig. 31. OCP threshold timing diagram

$$I_{OCP} = \frac{[\,1.9\ \text{V}\ \text{x}\ 8800\,]}{R_{SET}}$$

Equation 2. OCP trip current threshold equation

8.9. Over Temperature Protection (OTP)

This GaN Power IC includes over-temperature detection and protection (OTP) circuitry to protect the IC excessively high junction temperatures (T_J). High junction temperatures can occur due to overload, high ambient temperatures, and/or poor thermal management. Should T_J exceed the internal T_{OTP+} threshold (165C, typical) the IC will latch off safely. When T_J decreases again and falls below the internal T_{OTP-} threshold (105C, typical), then the OTP latch will be reset. Until then, internal OTP latch is guaranteed to remain in the correct state while is greater than 5V. During an OTP event, this GaN IC will latch off and the system V_{CC} supply voltage will due to the loss of the aux winding supply. The system V_{CC} will fall below the lower UV- threshold of the controller and the high-voltage start-up circuit will turn-on and V_{CC} will increase again (Fig. 32). V_{CC} will increase above the rising UV+ threshold and the controller will turn on again and deliver PWM pulses again.

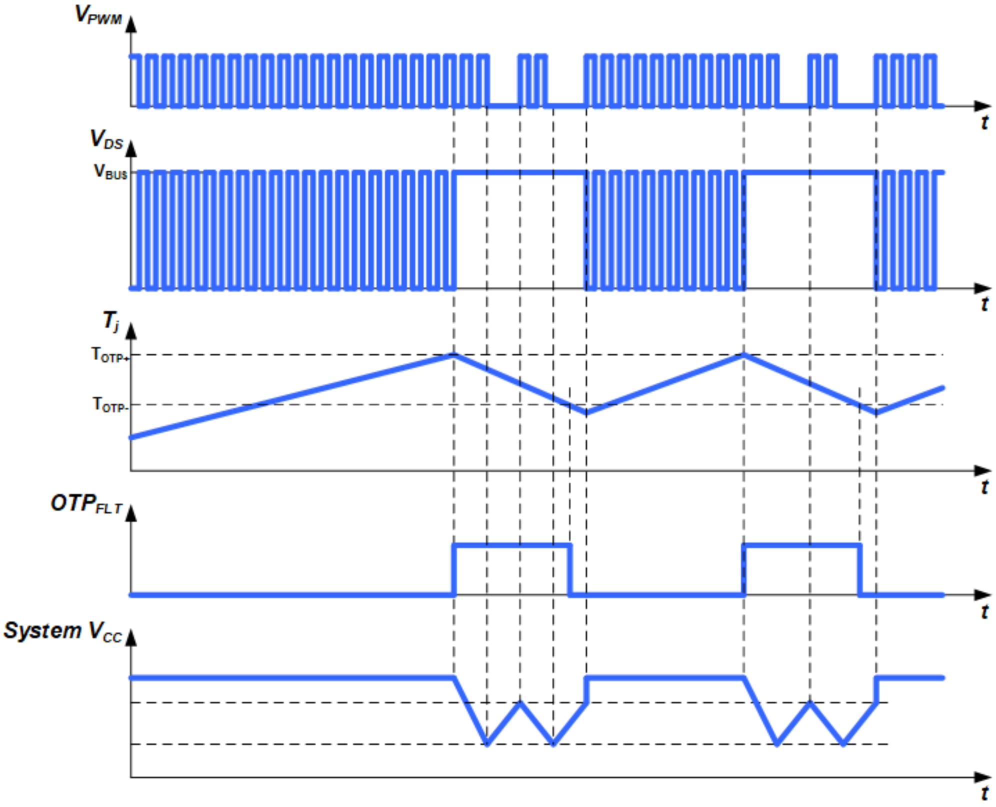


Fig. 32. OTP threshold timing diagram

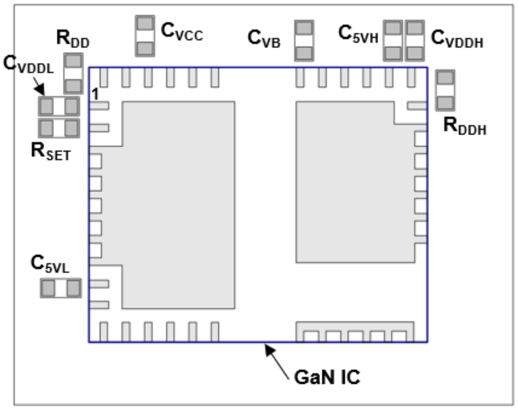
9. PCB Layout Guidelines

For best electrical and thermal results, these PCB layout guidelines (and 4 steps below) must be followed:

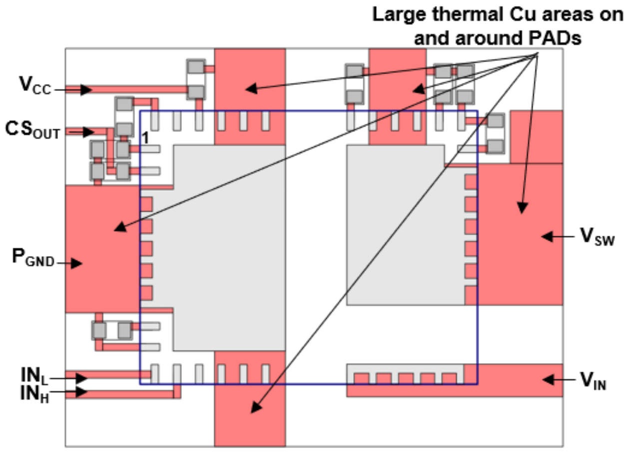
1) Place IC components as close as possible to the GaN IC. Place R_{SET} resistor directly next to CS pin to minimize high frequency switching noise.
2) Connect the ground of IC components to Source to minimize high frequency switching noise. Connect controller ground also to Source (P_{GND}).
3) Route all connections on single layer. This allows for large thermal copper areas on other layers.
4) Place large copper areas on and around Pad1 and Pad2.
5) Place many thermal vias inside Pad1 and Pad2 and inside Pad1 and Pad2 copper areas.

Place large possible copper areas on all other PCB layers (bottom, top, mid1, mid2).

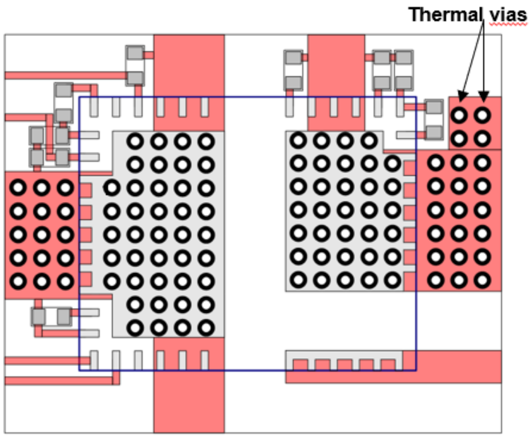
Do not extend copper planes from the low-side across the components or pads of the high-side; do not extend copper planes from the high-side across the components or pads of the low-side! Keep high and low-side layouts separate. Do not overlap!



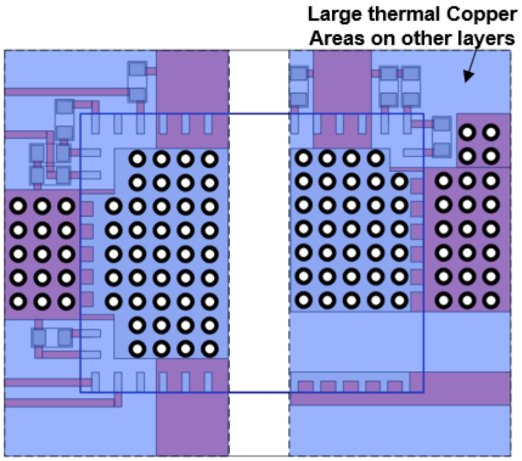
Step 1. Place GaN IC and components on PCB. Place components as close as possible to IC



Step 2. Route all connections on single layer. Make large copper areas on and around Source pad

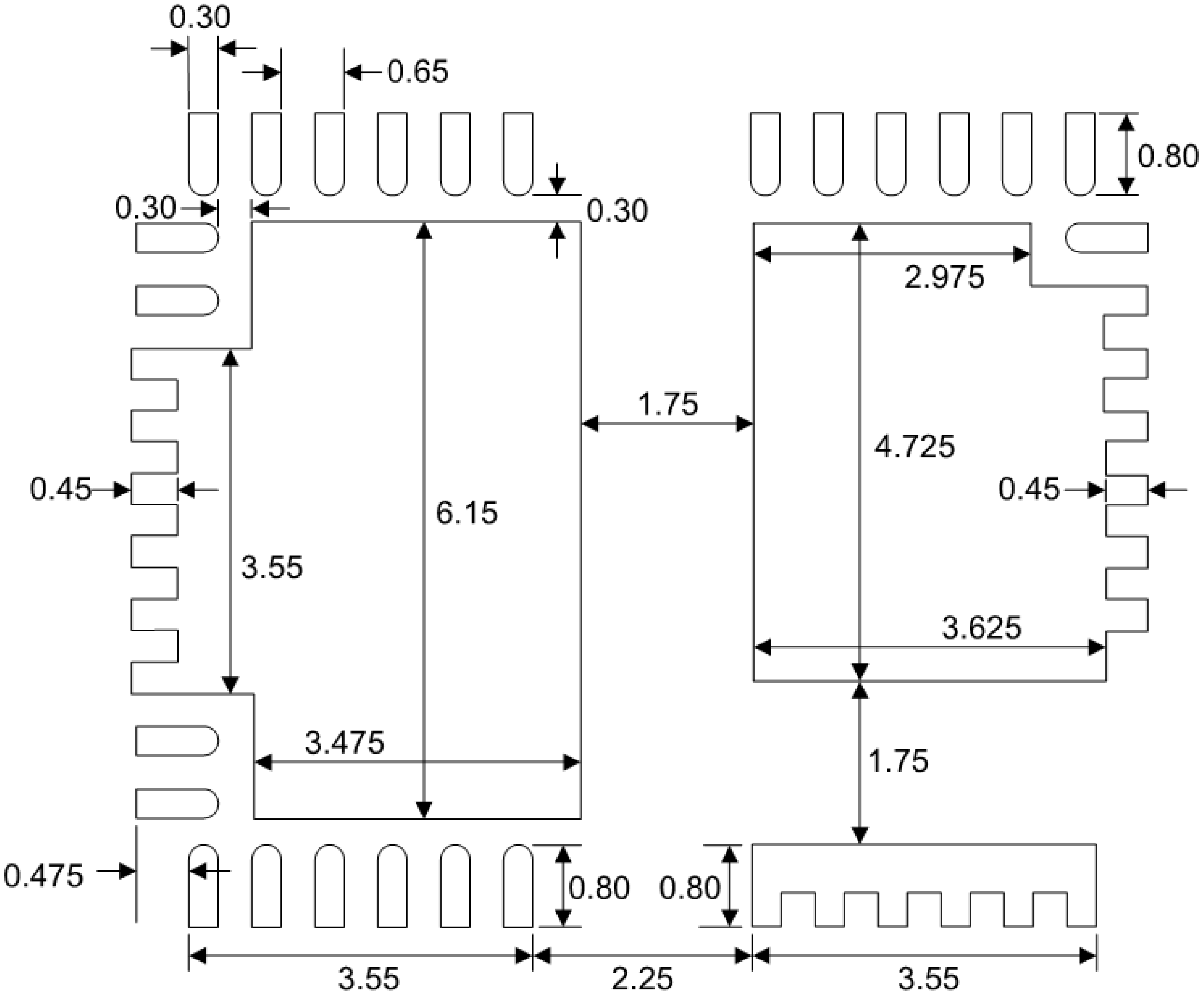


Step 3. Place many thermal vias inside source pad and inside source copper areas. (dia=0.65mm, hole=0.33mm, pitch=0.925mm, via wall=1mil)



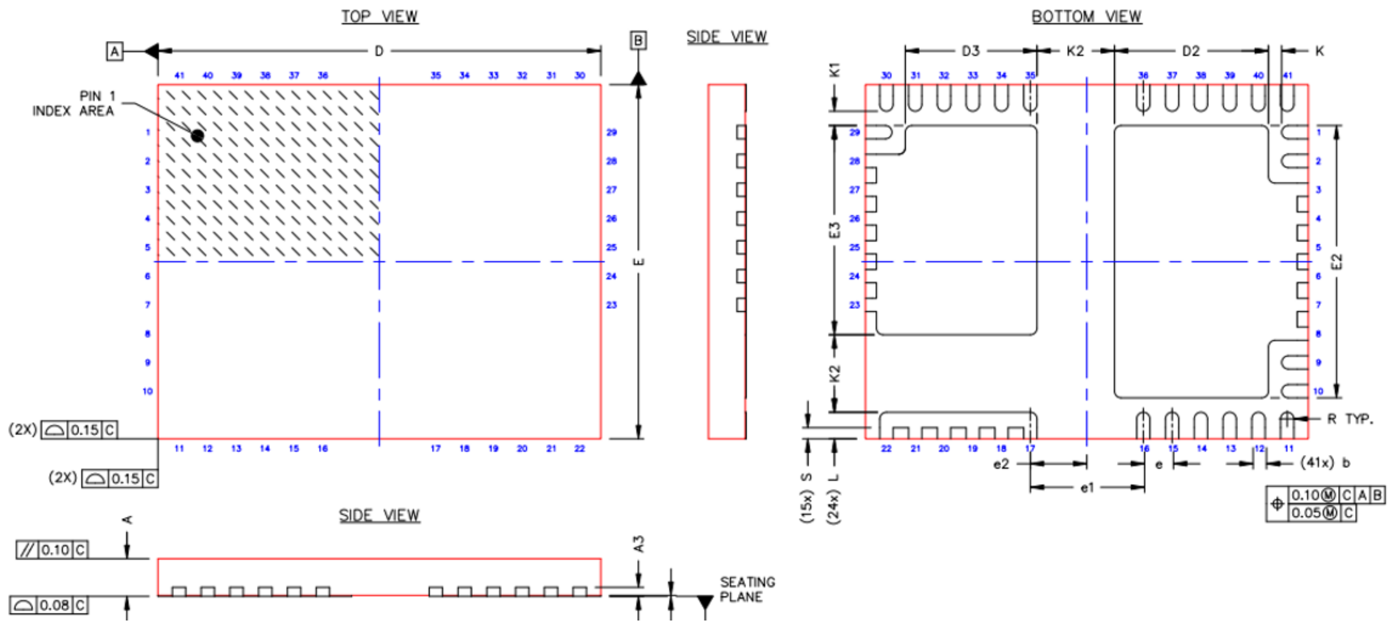
Step 4. Place large copper areas on other layers. Make all thermal copper areas as large as possible!

10. Recommended PCB Land Pattern



Top View
All dimensions are in mm

11. Package Outline (Power QFN)

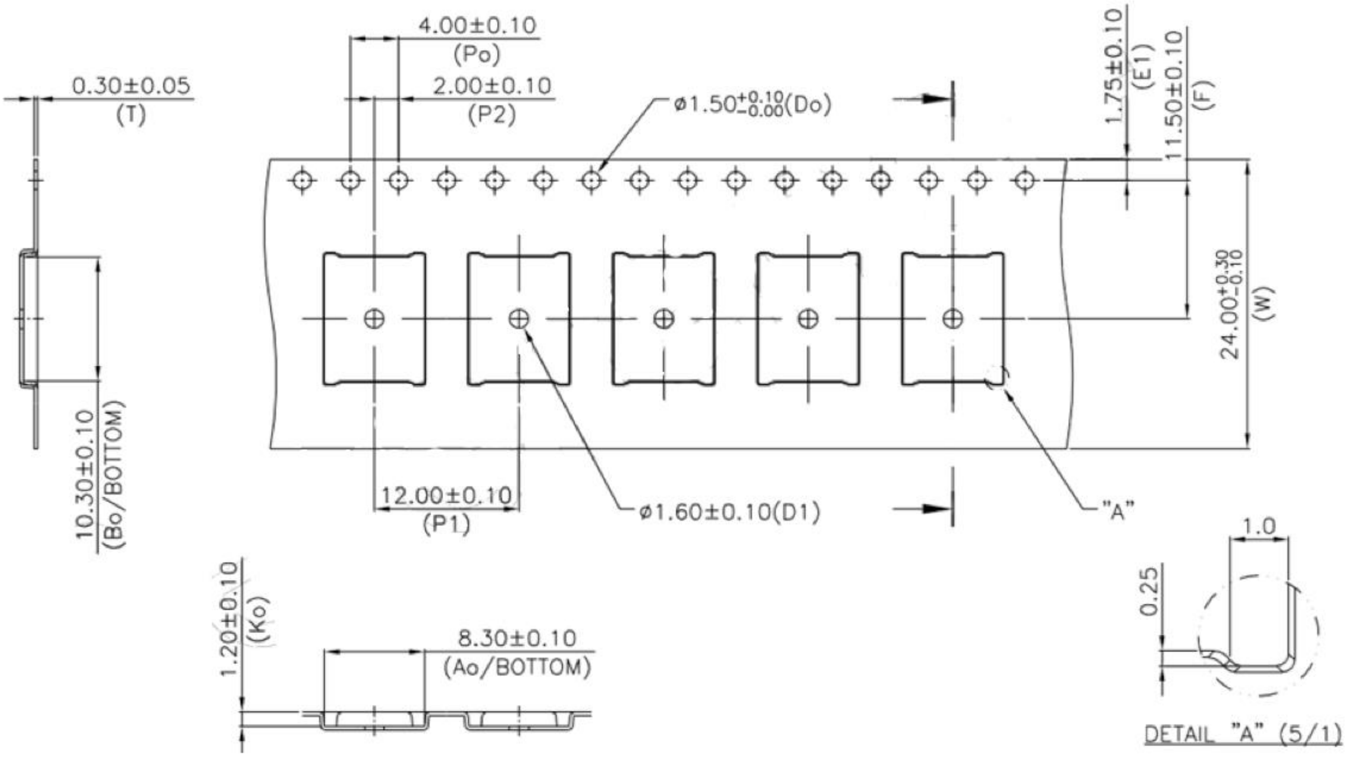


SYM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	–	0.05
A3	–	0.203 REF.	–
b	0.25	0.30	0.35
D	9.90	10.00	10.10
E	7.90	8.00	8.10
D2	3.425	3.475	3.525
E2	6.10	6.15	6.20
D3	2.925	2.975	3.025
E3	4.675	4.725	4.775
e		0.65 BSC	
e1		2.55 BSC	
e2		1.275 BSC	
K	–	0.30 REF.	–
K1	–	0.325 REF.	–
K2	–	1.75 REF.	–
L	0.55	0.60	0.65
R	–	0.15 REF.	–
S	0.20	0.25	0.30

NOTES:

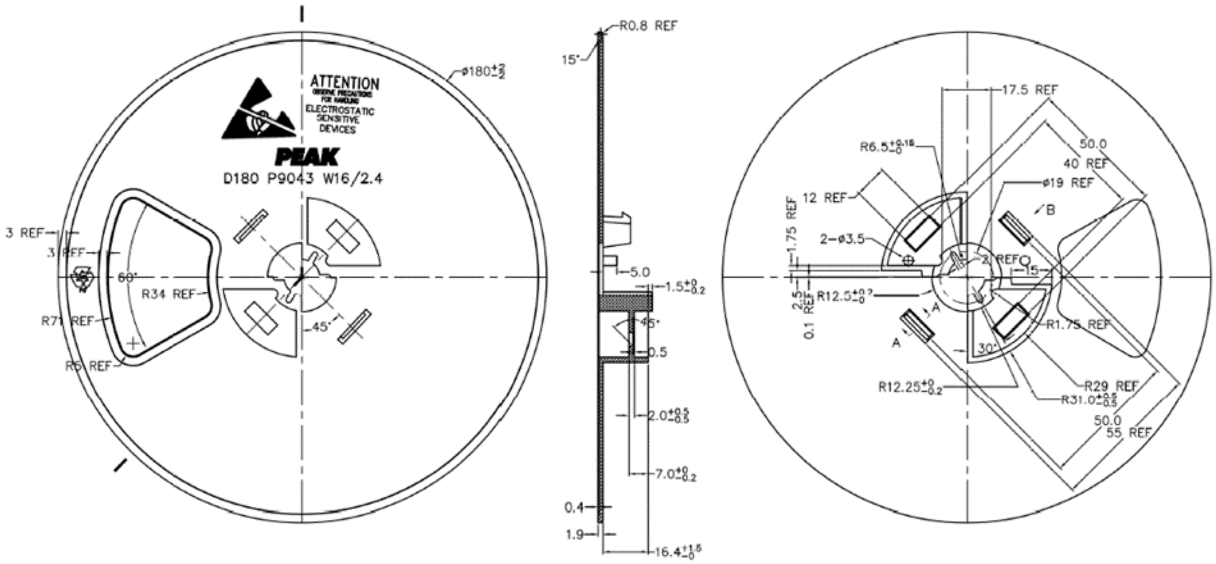
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. MAXIMUM ALLOWABLE BURRS IS 0.050 MM IN ALL DIRECTIONS.

12. Tape and Reel Dimensions

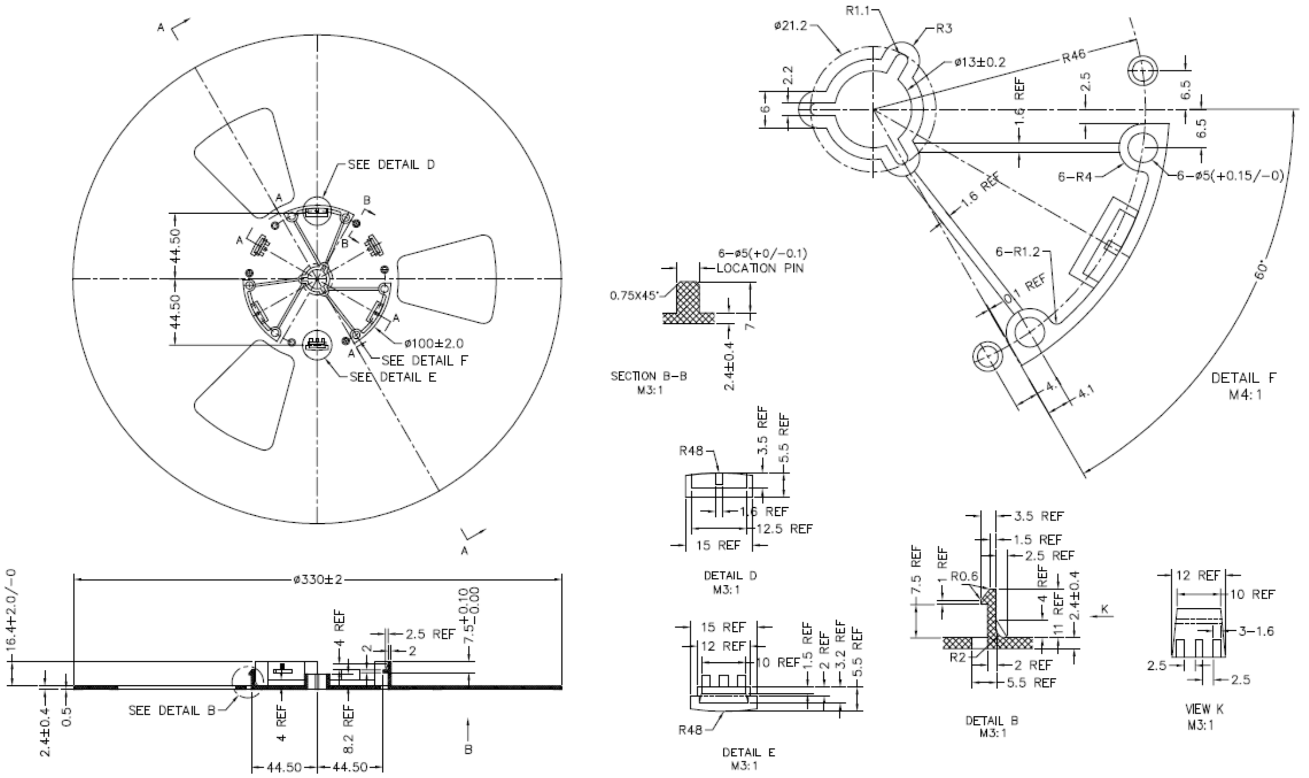


13. Tape and Reel Dimensions (Cont.)

7” Reel



13” Reel



14. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing (Tape & Reel)
NV6269M-RA	-55°C to +150°C T_{CASE}	-55°C to +150°C T_{CASE}	8 x 10 mm PQFN	3	1000: 7” Reel
NV6269M	-55°C to +150°C T_{CASE}	-55°C to +150°C T_{CASE}	8 x 10 mm PQFN	3	5000: 13” Reel

15. 20-Year Limited Warranty

The product(s) described in this data sheet **include a** warranty period of twenty (20) years under, and subject to the terms and conditions of, Navitas' express limited product warranty, available at https://navitassemi.com/terms-conditions. The warranted specifications include only the MIN and MAX values only listed in Absolute Maximum Ratings, ESD Ratings and Electrical Characteristics sections of this datasheet. Typical (TYP) values or other specifications are not warranted.

16. Revision History

Date	Status	Notes
Mar. 21, 2024	Preliminary Revision	Graphs need to be updated
May. 13, 2024	Prelim Update	All data and graphs added. Theta JA to be updated.
Sep. 24, 2024	Final	Change RDD from 100/1000 to 300/1500. Fix several typos.

Additional Information

Contact info@navitassemi.com