700V Advanced GaNSlim Power IC NV6144C

1. Feature

- Integrated gate drive
- 3.3V/5V/15V PWM logic input compatible
- Programmable accurate GaN current sensing
- Over-temperature protection
- Wide V_{CC} range (6.2V to 24V typical)
- Low standby current (50uA typical)
- Sleep mode current (10uA max)
- Built-in turn-on dV/dt optimization
- Built-in turn-off di/dt optimization
- Reliable hard and soft switching
- Zero reverse recovery charge

DPAK-4L package with grounded cooling pad

- Grounded cooling pad
- Minimized package inductance
- Low thermal resistance

Sustainability

- RoHS, Pb-free, REACH-compliant
- Up to 40% energy savings vs Si solutions
- System level 4kg CO_2 Carbon Footprint reduction

Product Reliability

- 20-year limited product warranty
  (see Section 15 for details)

2. Applications

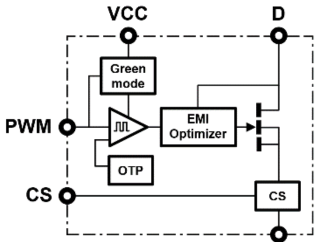
- AC-DC Charger & Adapter
- Wireless power
- LED lighting
- Solar Micro-inverters
- TV Power
- Server Power, Telecom Power

CERTIFIED CARBON NEUTRAL® company
CarbonNeutral.com

20-YEAR WARRANTY GaNFast™

GaNSlim™ Power IC
***with* GaNSense ™ Technology**

DPAK-4L



Simplified schematic

3. Description

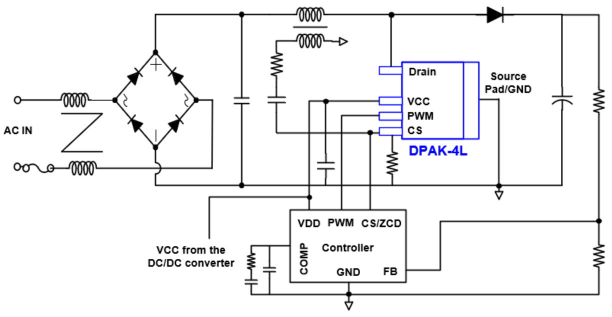
This feature-rich 700 V GaNSlim™ Power IC includes a high performance eMode GaN FET (260mΩ), integrated gate drive, and extended features to create the fastest, smallest, most efficient, and most robust integrated powertrain in the world.

Integrated lossless current sensing eliminates external current sensing resistors and increases system efficiency, over-temperature protection increases system robustness, auto standby and sleep mode increases light/tiny/no-load efficiency.

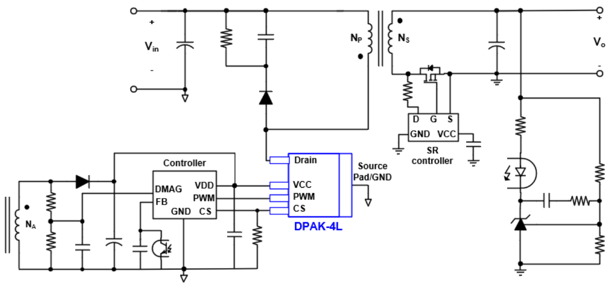
The highest dV/dt immunity, high-speed integrated drive and industry-standard low-profile, low-inductance, DPAK package combine to enable designers to exploit Navitas GaN technology with simple, quick, reliable solutions achieving breakthrough power density and efficiency.

Navitas' GaNSlim™ power ICs extend the capabilities of traditional topologies and enable the commercial introduction of breakthrough design.

4. Typical Application Circuits



Boost PFC



QR Flyback

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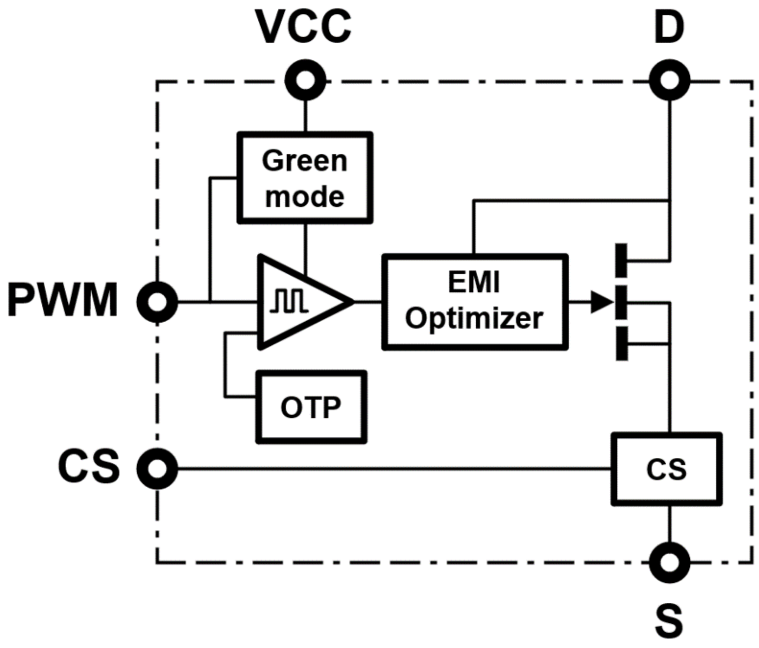
6. Block Diagram



Notes:

- GND connection for the IC is to the die pad.
- CS is the analog test output.

7. Specifications

7.1. Absolute Maximum Ratings (1) (with respect to Source (pad) unless noted)

SYMBOL	PARAMETER	MAX	UNITS
V_{DS}	Drain-to-Source Voltage	-7 to +700	V
V_{TDS}	Transient Drain-to-Source Voltage(2)	800	V
V_{CC}	Supply Voltage	30	V
V_{CS}	CS Pin Voltage	5.3	V
PWM	OUTH Output Pin Voltage	-0.6V~Vcc	V
I_D	260 mΩ Version Continuous Drain Current (@ $T_C = 25$ºC)	7.9	A
I_D	260 mΩ Version Continuous Drain Current (@ $T_C = 100$ºC)	5	A
I_D PULSE	260 mΩ Version Pulsed Drain Current (10 µs, $T_J = 125$ºC)	10	A
T_J	Operating Junction Temperature	-55 to 150	ºC
T_{STOR}	Storage Temperature	-55 to 150	ºC

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS\ (TRAN)}$ rating allows for surge ratings during non-repetitive events that are <100us (for example start-up, line interruption). $V_{DS\ (TRAN)}$ rating allows for repetitive events that are <400ns, with 80% derating required (for example repetitive leakage inductance spikes). Refer to Section 9.7 for detailed recommended design guidelines.

7.2. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	10.5		24	V
VPWM	PWM input pin voltage	0	5	Vcc	V

7.3. ESD Ratings

SYMBOL	PARAMETER	MAX	UNITS
HBM	Human Body Model (per JS-001)	1,500	V
CDM	Charged Device Model (per JS-002)	1,000	V

7.4. Thermal Resistance

SYMBOL	PARAMETER	TYP (260 mΩ)	UNITS
$R_{\theta JC}$ (1)	Junction-to-Case	8.50	ºC/W
$R_{\theta JA}$ (1)	Junction-to-Ambient	51.85	ºC/W

(1) R_θ measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

7.5. Electrical Characteristics

Typical conditions: V_{DS} = 400 V, V_{CC} = 15 V, T_{AMB} = 25 ºC, I_D = I_{TEST}(2) (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC} and V_{DD} Supply Characteristics						
V_{CCUV+}	V_{CC} UVLO Rising Turn-On Threshold		9		V	
V_{CCUV-}	V_{CC} UVLO Falling Turn-Off Threshold			6.2	V	
$I_{QCC-STBY}$	V_{CC} Standby Current		50		µA	Standby
I_{CCO}	V_{CC} Operating Current		500		µA	PWM high
$I_{STARTUP}$				10	µA	V_{CC} = 24V
t_{WAKE_UV} (1)	Wake Up Delay from UVLO Mode		35		µs	V_{CC} = 0 → 15V during 1µs PWM tie to V_{CC}
I_{CC-SW}	V_{CC} Switching Current, 260 mΩ		0.8		mA	F_{SW} = 500kHz, V_{DS} = Open
Input Characteristics (PWM pin)						
V_{PWM_H}	PWM Pin Logic High Threshold			2.7	V	
V_{PWM_L}	PWM Pin Logic Low Threshold	1.1			V	
$V_{PWM-HYS}$	PWM Pin Input Logic Hysteresis		0.6		V	
Sleep mode Characteristics						
t_{WAKE_Sleep}	Wake up delay time from Sleep mode			1.1	us	From PWM high
t_{TO_Sleep}	Time Out Delay Entering Sleep Mode		11		ms	From PWM low
Standby Mode Characteristics						
t_{TO_STBY}	Time Out Delay Entering Standby Mode		75		µs	
t_{WAKE_STBY}	Wake Up Delay Time from Standby Mode			350	ns	
Current Sense Characteristics (CS pin)						
I_{CS}	CS Pin Output Current	1.16	1.25	1.34	mA	V_{PWM} =5V, I_{DS} =.5* I_{DSMAX}
$t_{CSDLY10}$(1)	CS Pin Delay from I_{DS}=10% rated current to V_{CS}=10% of desired full-scale voltage		62		ns	0.25us from 0 to Idmax R_{CS}=400Ohm

Electrical Characteristics (cont.)

Typical conditions: V_{DS} = 400 V, V_{CC} = 15 V, T_{AMB} = 25 ºC, I_D = I_{TEST}(2) (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Over Temperature Protection						
T_{OTP+}(1)	OTP Shutdown Threshold		160		ºC	
T_{OTP_HYS}	OTP Restart Hysteresis		65		ºC	

Electrical Characteristics (cont.)

Typical conditions: V_{DS} = 400 V, V_{CC} = 15 V, T_{AMB} = 25 ºC, I_D = I_{TEST}(2) (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
NV6144C GaN FET Characteristics (260 mΩ version)						
I_{DSS}	Drain-Source Leakage Current		0.15	25	µA	V_{DS} = 650 V, V_{PWM} = 0 V
I_{DSS}	Drain-Source Leakage Current		11		µA	V_{DS} = 650 V, V_{PWM} = 0 V, T_C = 150 ºC
$R_{DS(ON)}$	Drain-Source Resistance		260	364	mΩ	$V_{PDC/PWM}$ = 0 V, I_D = 2.5 A
V_{SD}	Source-Drain Reverse Voltage		3.5	5	V	$V_{PDC/PWM}$ = 5 V, I_{SD} = 2.5 A
Q_{OSS}	Output Charge		8.8		nC	V_{DS} = 400 V, V_{PWM} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	
C_{OSS}	Output Capacitance		13		pF	V_{DS} = 400 V, V_{PWM} = 0 V
$C_{O(er)}$(3)	Effective Output Capacitance, Energy Related		16		pF	V_{DS} = 400 V, V_{PWM} = 0 V
$C_{O(tr)}$(4)	Effective Output Capacitance, Time Related		22		pF	V_{DS} = 400 V, V_{PWM} = 0 V

(1) Guarantee by design

(2) I_{TEST} = 2A

(3) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(4) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

7.6. Typical Waveforms

(T_C = 25 ºC unless otherwise specified)

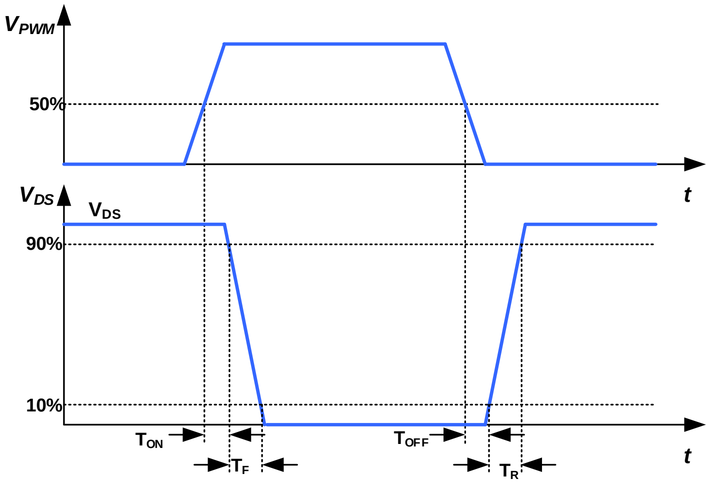


Figure 1. Inductive Switching Test Circuit

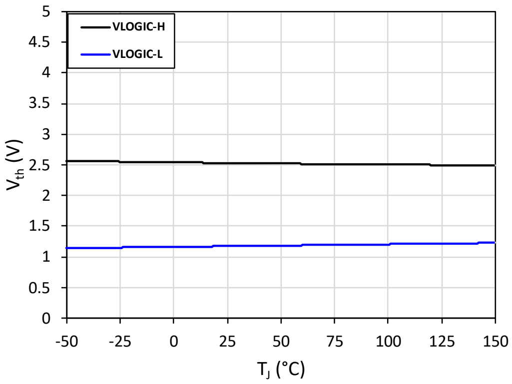


Figure 2. $V_{LOGIC-H}$ and $V_{LOGIC-L}$ vs. junction temperature(T_J)

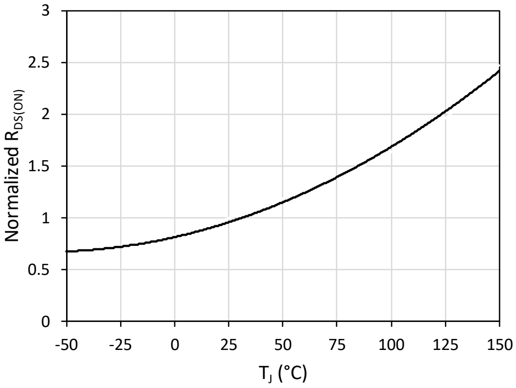


Figure 3. Normalized on-resistance ($R_{DS(ON)}$) vs. junction temperature (T_J)

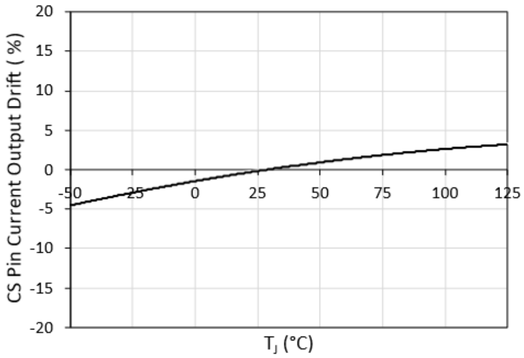


Figure 4. CS Pin Current Output Drift vs. case temperature (T_C)

Typical Waveform

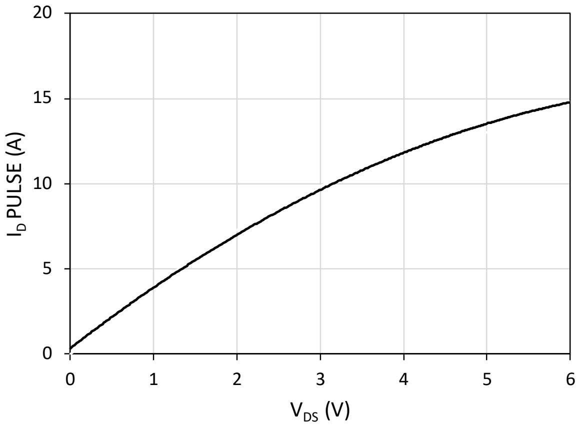


Figure 5. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 25 °C

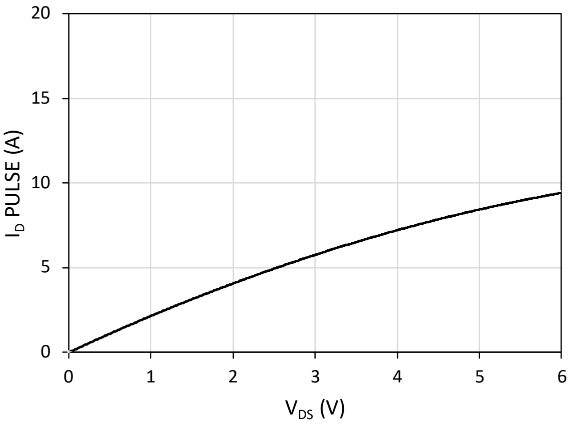


Figure 6. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 125 °C

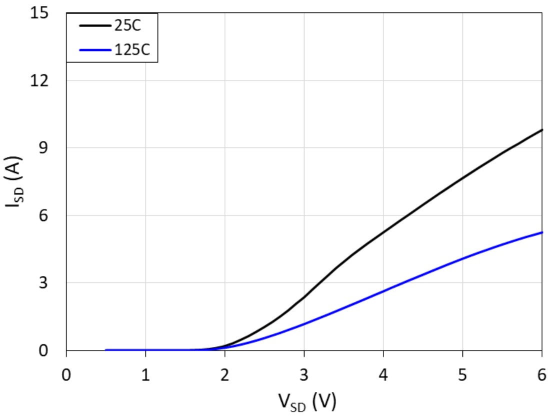


Figure 7. Source-to-drain reverse conduction voltage

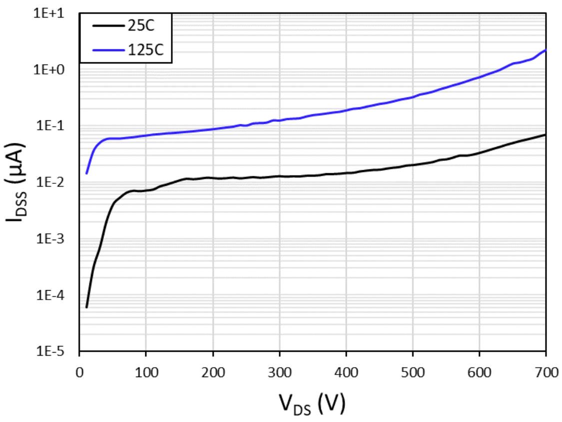


Figure 8. Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS})

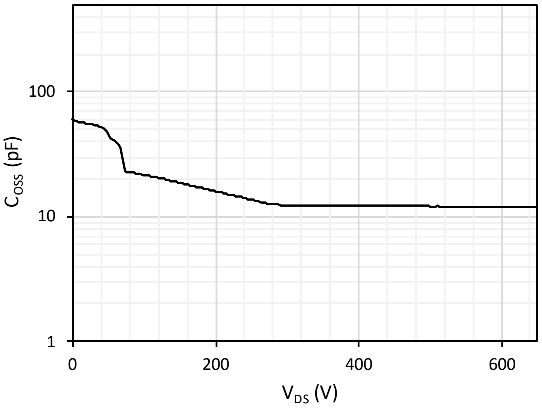


Figure 9. Output capacitance (C_{OSS}) vs. drain-to-source voltage (V_{DS})

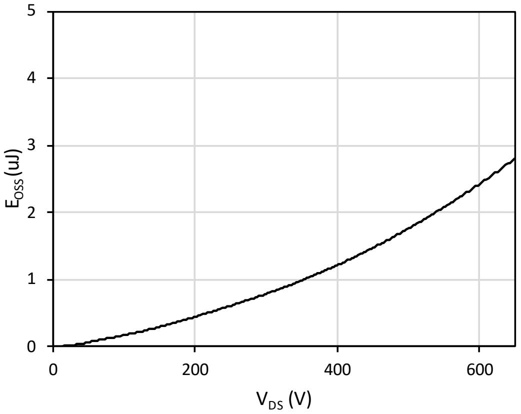


Figure 10. Energy stored in output capacitance (E_{OSS}) vs. drain-to-source voltage (V_{DS})

Typical Waveform(cont.)

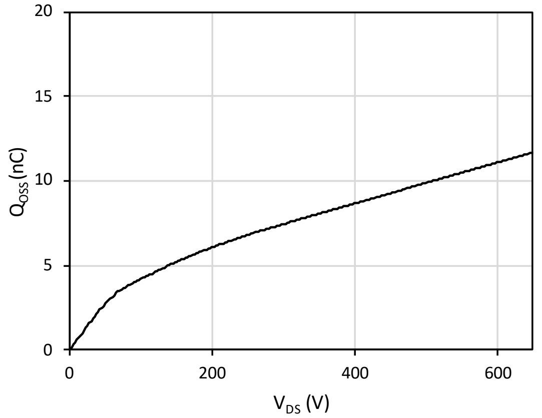


Figure 11. Charge stored in output capacitance (QOSS) vs. drain-to-source voltage (VDS)

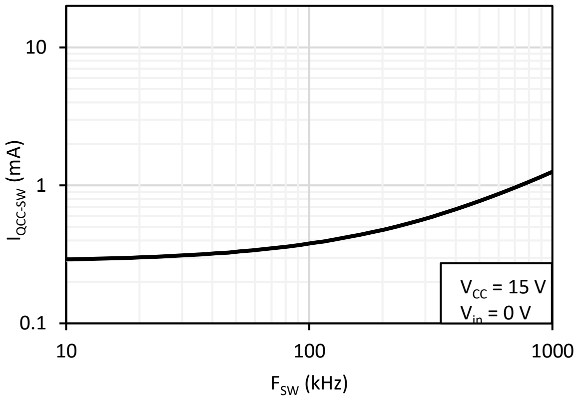


Figure 12. VCC operating current (IQCC-SW) vs. switching frequency

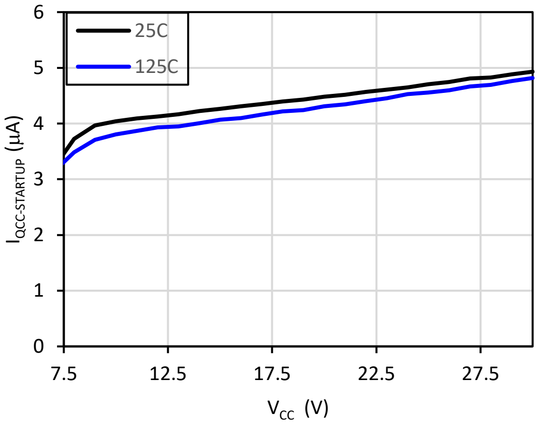


Figure 13. VCC STARTUP current (IQCC-STARTUP) vs. Supply Voltage (VCC)

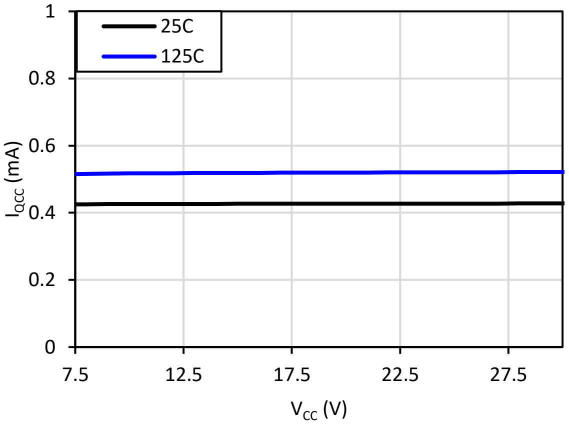


Figure 14. VCC quiescent current vs. Supply Voltage (VCC)

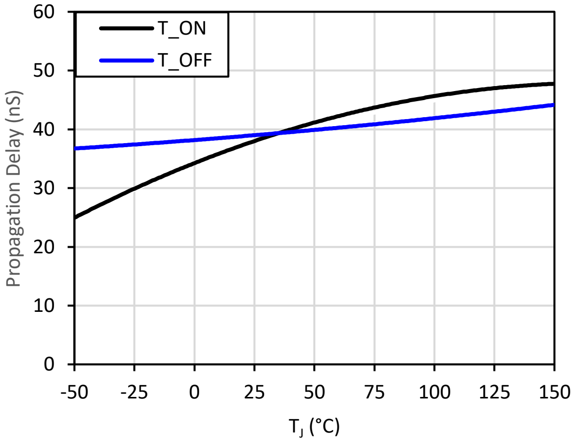


Figure 15. CP01 Propagation delay (TON and TOFF) vs. junction temperature(TJ)

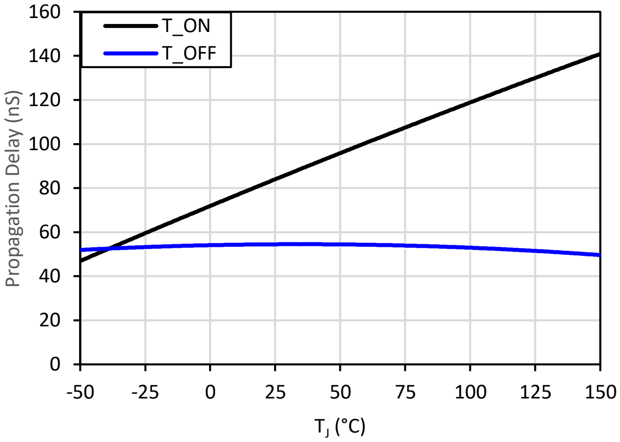


Figure 16. CQ01 Propagation delay (TON and TOFF) vs. junction temperature(TJ)

8. Pin Configurations and Functions

8.1. GaNSlim "Single" DPAK-4L

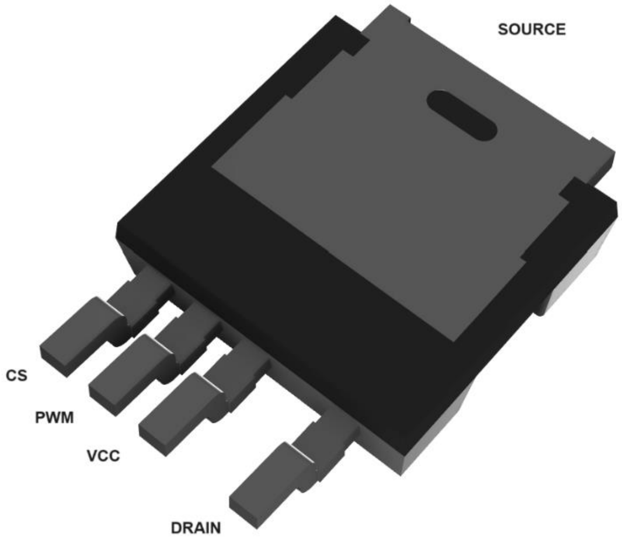


Figure 17. Package Bottom View

Pin		I/O[1]	Description
Number	Symbol		
1	Drain	P	Drain of power FET.
2	VCC	P	IC supply voltage.
3	PWM	I	PWM input.
4	CS	O	GaN FET I DS current sensing set pin. Internal current source and external resistor sets current measurement level. External resistor reference is SGND.
SOURCE	GND	G	Source of power FET & IC supply ground. Metal pad on bottom of package.

Note 1: I = Input, O = Output, P = Power, G = Ground, T = Test Mode

9. Functional Description

The following functional description contains additional information regarding the IC operating modes and pin functionality. Please refer to the State Diagram for additional details.

9.1. GaN Power IC Connections and Component Values

The typical connection diagram for this GaN Power IC is shown in Fig 18. The IC pins include drain of the GaN power FET (D), source of the GaN power FET (S), IC supply (V_{CC}), PWM input (PWM), and current sensing output (CS). The external components around the IC include V_{CC} filter capacitor (C_{VCC}) connected between V_{CC} pin and S pin, a current sense amplitude set resistor (R_{SET}) connected between CS pin and S.

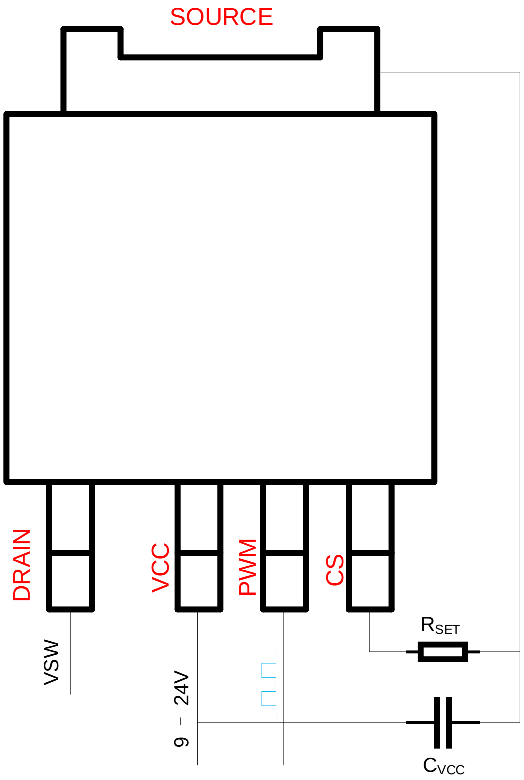


Figure 18. IC connection diagram

The following table (Table I) shows the recommended component values (typical only) for the external components connected to the pins of this GaN power IC. These components should be placed as close as possible to the IC. Please see PCB Layout Guidelines for more information.

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} supply capacitor	0.1	µF
R_{SET}	Current sense amplitude set resistor	Depends on system design (See Section 9.5 Equation 1)	Ω

Table I. Recommended component values (typical only).

9.2. UVLO Mode

This GaN Power IC includes under-voltage lockout (UVLO) circuits for properly disabling all the internal circuitry when VCC is below the VCCUV+ threshold (8.5V, typical). During UVLO Mode, the internal gate drive and power FET are disabled and VCC consumes a low quiescent current which is less than 10uA. As the VCC supply voltage increases (Figure 19) and exceeds VCCUV+, the IC enters Normal Operating Mode when PWM goes high. The gate drive is enabled and the control signal at the PWM input turns the internal GaN power FET on and off normally. During system power off, when VCC decreases below the VCCUV- threshold (5.5, typical), the gate drive is disabled and the IC enters UVLO Mode.

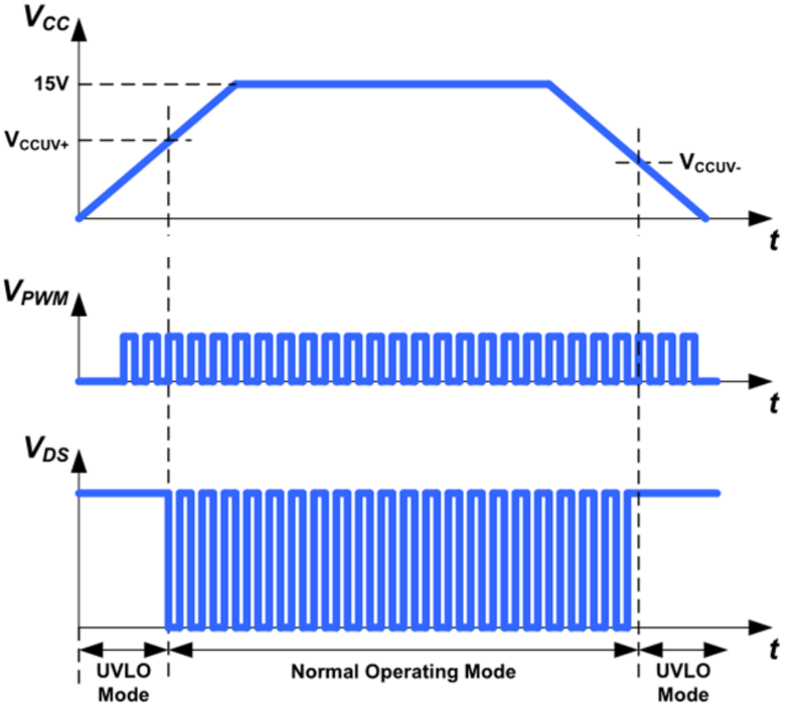


Figure 19. UVLO Mode and Normal Operating Mode Timing Diagram

9.3. Normal Operating Mode

During Normal Operating Mode, all the internal circuit blocks are active. V_{CC} is above 9.5V, the internal gate drive and power FET are both enabled. The external PWM signal at the PWM pin determines the frequency and duty-cycle of the internal gate of the power FET. As the PWM voltage toggles above and below the rising and falling input thresholds (2.7V and 1.1V), the internal power FET toggles on and off (Figure 20). The drain of the power FET then toggles between the source voltage (power ground) and a higher voltage level (700V, max), depending on the external power conversion circuit topology. During each on-time, the CS pin outputs a voltage signal from the internal loss-less current sensing circuit. This circuit measures the current flowing in the GaN power FET without the need for an external current sensing resistor (see section 9.5 GaNSense^{TM} Technology Loss-Less Current Sensing).

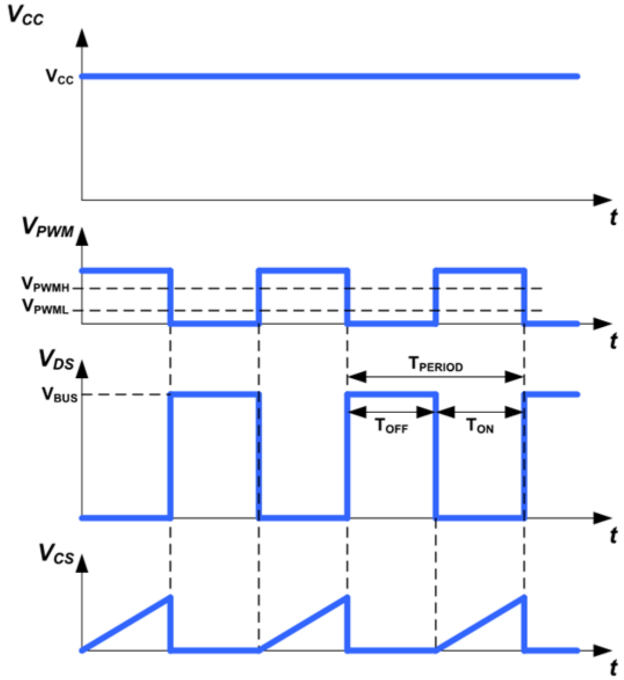


Figure 20. Normal Operating Mode Timing Diagram (PWM input)

9.4. Low Power Standby Mode and Sleep Mode

This GaN Power IC includes an autonomous Low Power Standby Mode for disabling the IC and reducing the VCC current consumption. During Normal Operating Mode, the PWM pin toggles high and low to turn the GaN power FET on and off. If the input pulses at the PWM pin stop and stay below the lower V_{PWML} turn-off threshold (1.1V, typical) for the duration of the internal timeout standby delay (t_{TO_STBY}, 75usec, typical), then the IC will automatically enter Low Power Standby Mode (Figure 21). This will disable the gate drive and internal current sense circuitry and reduce the V_{CC} supply current to a low level (50uA, typical). If PWM pin continue to stay below the lower VPWML turn-off threshold for the duration of the internal timeout sleep delay (t_{TO_SLEEP}, 10msec, typical), then the IC will automatically enter Low Power Sleep Mode (Figure 21). This will disable the gate drive and other internal circuitry and reduce the V_{CC} supply current to less than 10uA. When the PWM pulses restart, the IC will wake up with another wake-up delay (less than 200ns from standby mode or less than 1us from Sleep mode) at the first rising edge of the PWM input and enter Normal Operating Mode again.

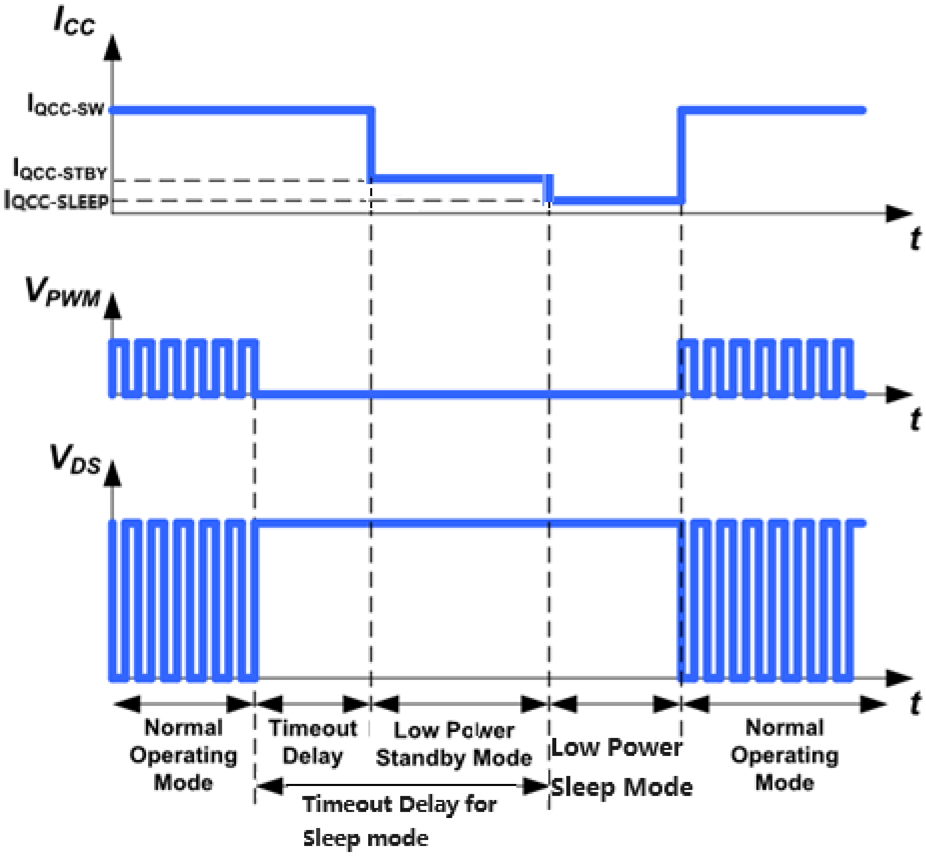


Figure 21. Sleep Mode Operating Timing Diagram

9.5. GaNSenseTM Technology Loss-Less Current Sensing

For many applications it is necessary to sense the cycle-by-cycle current flowing through the power FET. Existing current sensing solutions include placing a current sensing resistor in between the source of the power FET and PGND. This resistor method increases system conduction power losses, creates a hotspot on the PCB, and lowers overall system efficiency. To eliminate this external resistor and hotspot, and increase system efficiency, this IC includes GaNSenseTM Technology for integrated and accurate loss-less current sensing. The current flowing through the internal GaN power FET is sensed internally and then converted to a current at the current sensing output pin (CS). An external resistor (R_{SET}) is connected from the CS pin to the GND pin and is used to set the amplitude of the CS pin voltage signal (Figure 22). This allows for the CS pin signal to programmed to work with different controllers with different current sensing input thresholds.

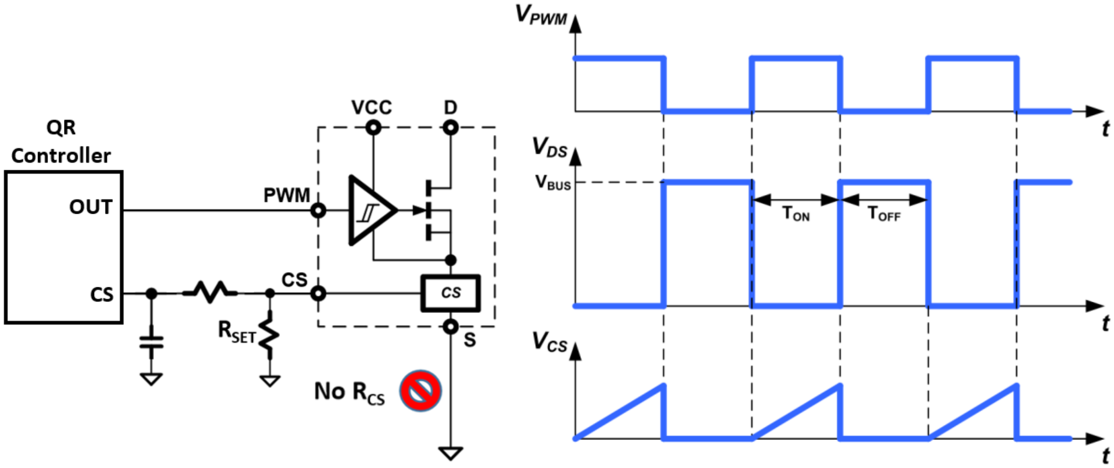


Figure 22. Current sensing circuit and timing diagram

When comparing GaNSenseTM Technology versus existing external resistor sensing method (Figure 23), the total ON resistance, $R_{ON(TOT)}$, can be substantially reduced. For a 65W high-frequency QR flyback circuit, for example, $R_{ON(TOT)}$ is reduced from 520m to 260m. The power loss savings by eliminating the external resistor results in a +0.5% efficiency benefit for the overall system.

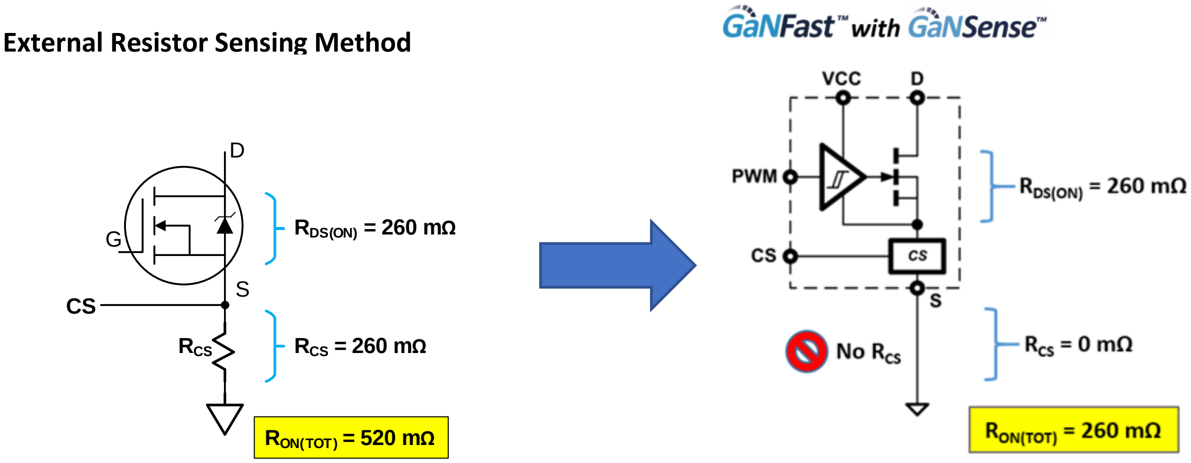


Figure 23. External resistor sensing vs. GaNSense^{TM} Technology

To select the correct R_{SET} resistor value, the following equation (Equation 1) can be used. This equation uses the equivalent desired external current sensing resistor value (R_{CS}), together with the gain of the internal sensing circuitry, to generate the equivalent R_{SET} resistor value. This R_{SET} value will then give the correct voltage level at the CS pin to be compatible with the internal current sensing threshold of the system controller.

$$R_{SET} * I_{CS} = R_{CS} * I_{DS}$$

$$I_{CS\_Ratio} = \frac{I_{DS}}{I_{CS}}$$

$$R_{SET} = I_{CS\_Ratio} * R_{CS}$$

Equation 1. R_{SET} resistor value equation

PartNumber	NV6144C
Ics_ratio	2240

9.6. Over Temperature Protection (OTP)

This GaN Power IC includes over-temperature detection and protection (OTP) circuitry to protect the IC against excessively high junction temperatures (T_J). High junction temperatures can occur due to overload, high ambient temperatures, and/or poor thermal management. Should T_J exceed the internal T_{OTP+} threshold (165℃, typical) then the IC will latch off safely. When T_J decreases again and falls below the internal T_{OTP-} threshold (95℃, typical), then the OTP latch will be reset. Until then, internal OTP latch guaranteed to remain in the correct state while V_{CC} is greater than 5V. During an OTP event, this GaN IC will latch off and the system V_{CC} supply voltage will decrease due to the loss of the aux winding supply. The system V_{CC} will fall below the lower UV- threshold of the controller and the high-voltage start-up circuit will turn-on and V_{CC} will increase again (Figure 24). V_{CC} will increase above the rising UV+ threshold and the controller turn on again and deliver PWM pulses again.

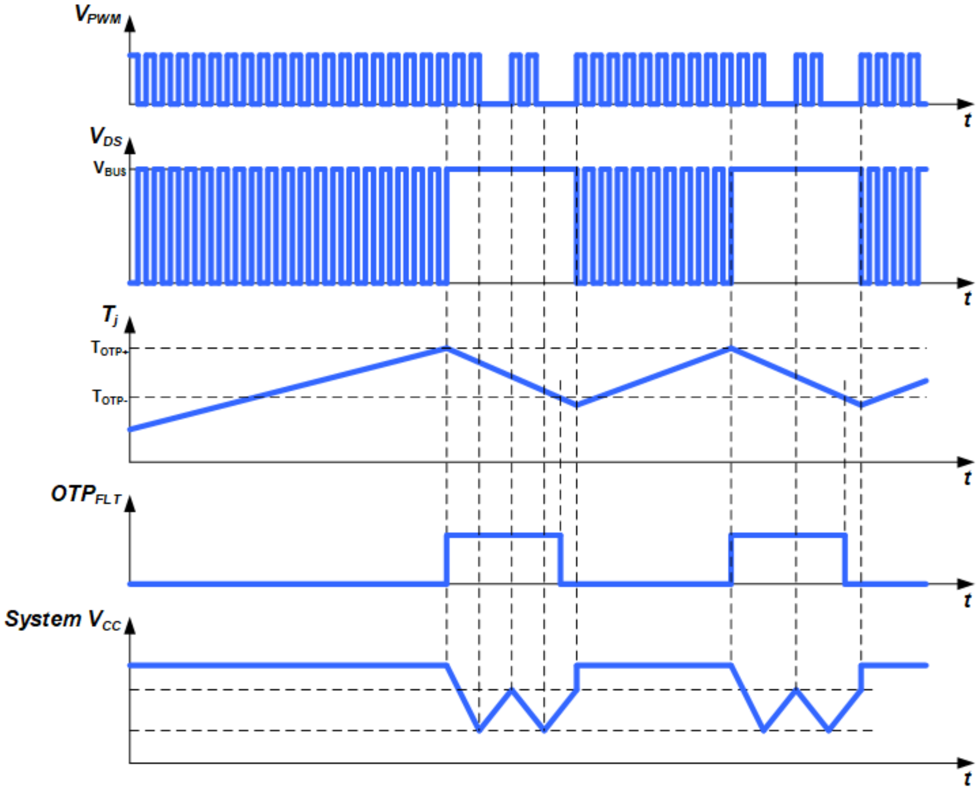


Figure 24. OTP threshold timing diagram

9.7. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Figure 25. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE}. The clamp circuit should be designed to control the magnitude of V_{SPIKE}. After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Figure 25 as $V_{DS\text{-}OFF}$.

- For repetitive events, 80% derating should be applied from $V_{DS\ (TRAN)}$ rating (800V) to 640V max under the worst-case operating conditions.

- It is recommended to design the system such that $V_{DS\text{-}OFF}$ is derated 80% from the $V_{DS(CONT)}$ (700V) max rating to 560V.
- For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the $V_{DS\text{-}OFF}$ derating guideline (560V).
- Non-repetitive events are infrequent, one-time conditions such as line surge, ESD, and lightning. No derating from the $V_{DS(TRAN)}$ rating (800V) is needed for non-repetitive V_{SPIKE} durations < 100 µs. The $V_{DS(TRAN)}$ rating (800V) allows for repetitive events that are <400ns, with 80% derating required (for example repetitive leakage inductance spikes).

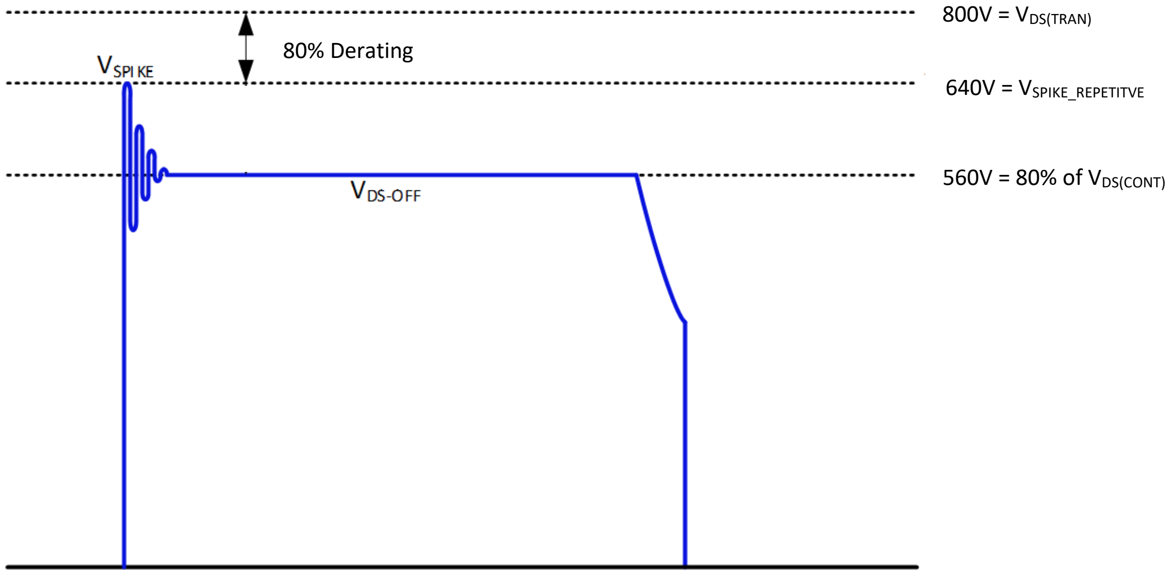


Figure 25. QR flyback drain-to-source voltage stress diagram

9.8. GaNSlim For High Side Application

The wake-up time from UVLO model of GaNSlim has 35us (typ) delay, so when GanSlim is designed for high side application, it requires the controller to accommodate. Navitas apps team has validated that GaNSlim works well with some controllers. It's highly recommended that the application note AN031 is referred to for system design if GaNSlim is used for high side.

10. PCB Layout Guidelines

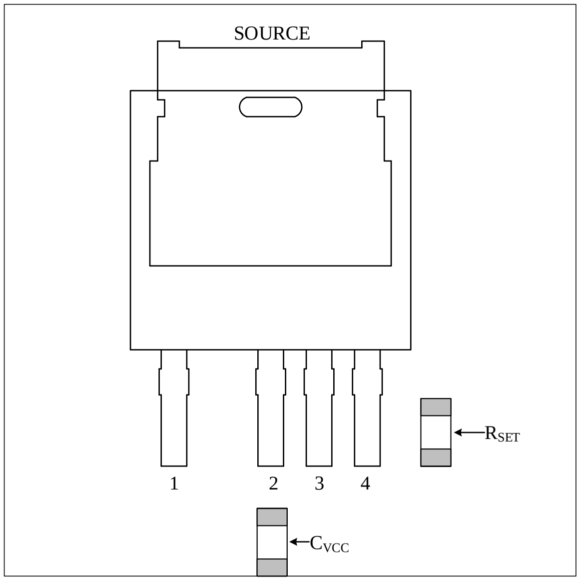
The design of the PCB layout is critical for good noise immunity, sufficient thermal management, and proper operation of the IC. A typical PCB layout example is shown as follow. The following rules should be followed carefully during the design of the PCB layout:

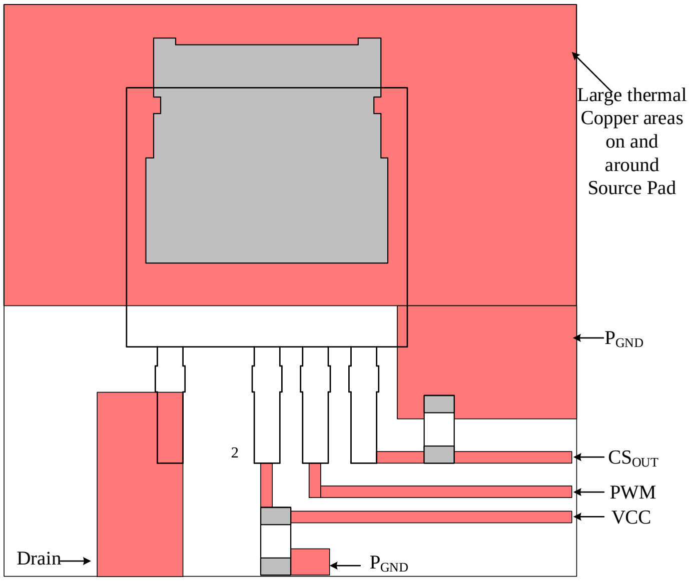
1) Place IC filter and programming components directly next to the IC. These components include (CVCC, RCS). Reference all these components to the GND pin.

2) Do not run power GND currents through signal GND!

3) For best thermal management, place thermal vias in the source pad area to conduct the heat out through the bottom of the package and through the PCB board to other layers.

4) Use large PCB thermal planes (connected with thermal vias to the source pad) and additional PCB layers to reduce IC temperatures as much as possible.



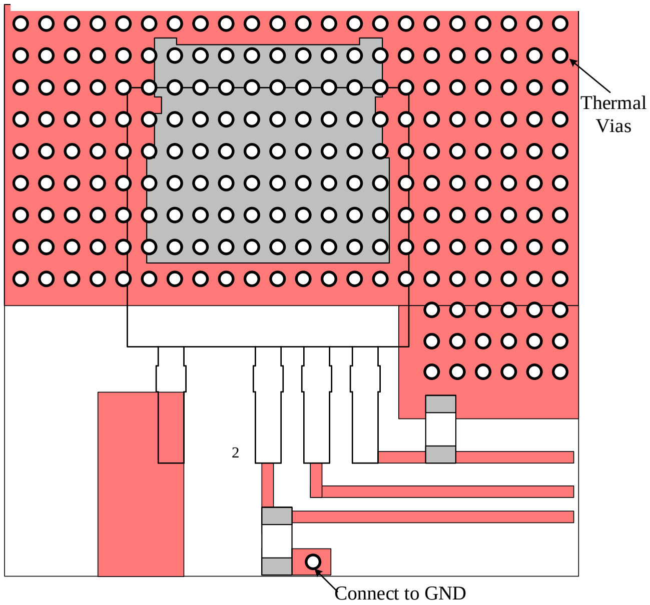


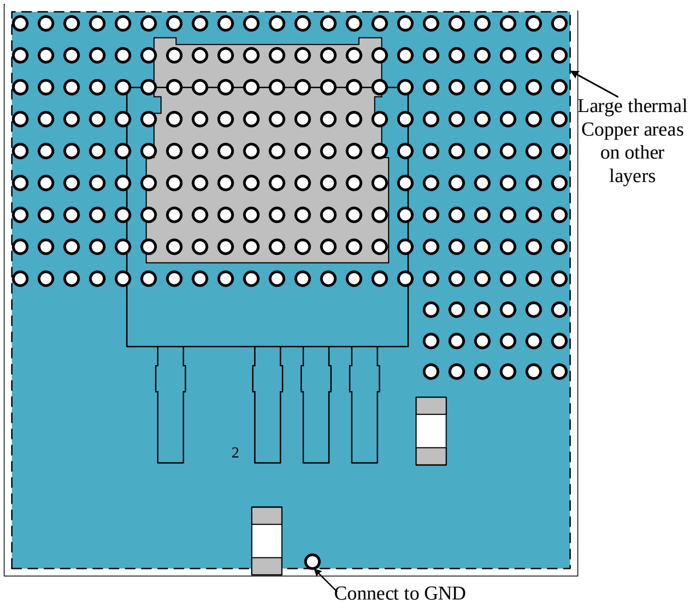
Step 1. Place GaN IC and components on PCB.

Place components as close as possible to IC!

Step 2. Route all connections on single layer.

Make large copper areas on and around Source pad!





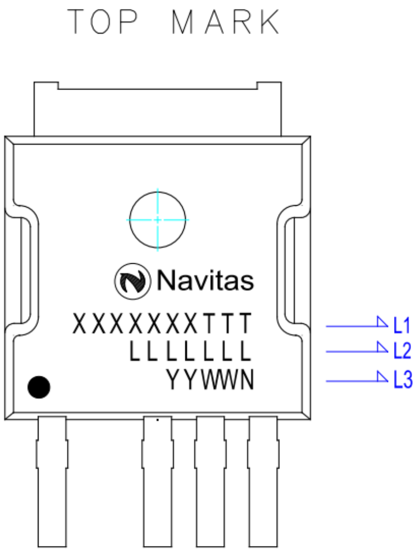
Step 3. Place many thermal vias inside source pad and inside source copper areas.

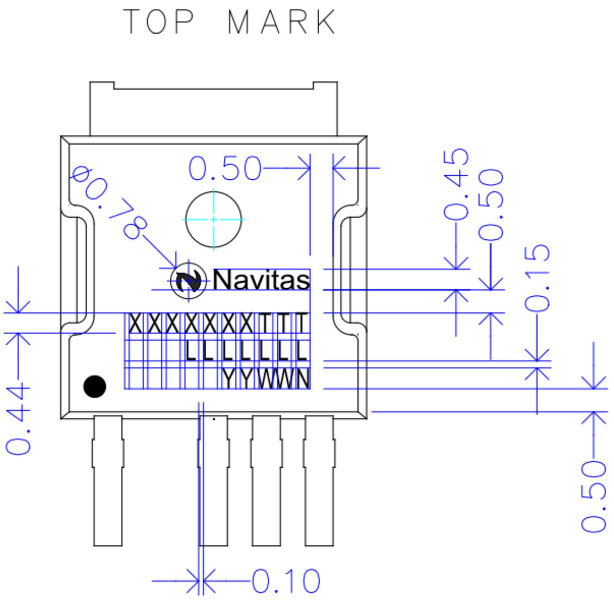
(dia=0.65mm, hole=0.33mm, pitch=0.925mm, via wall 1mil)

Step 4. Place large copper areas on other layers.

Make all thermal copper areas as large as possible!

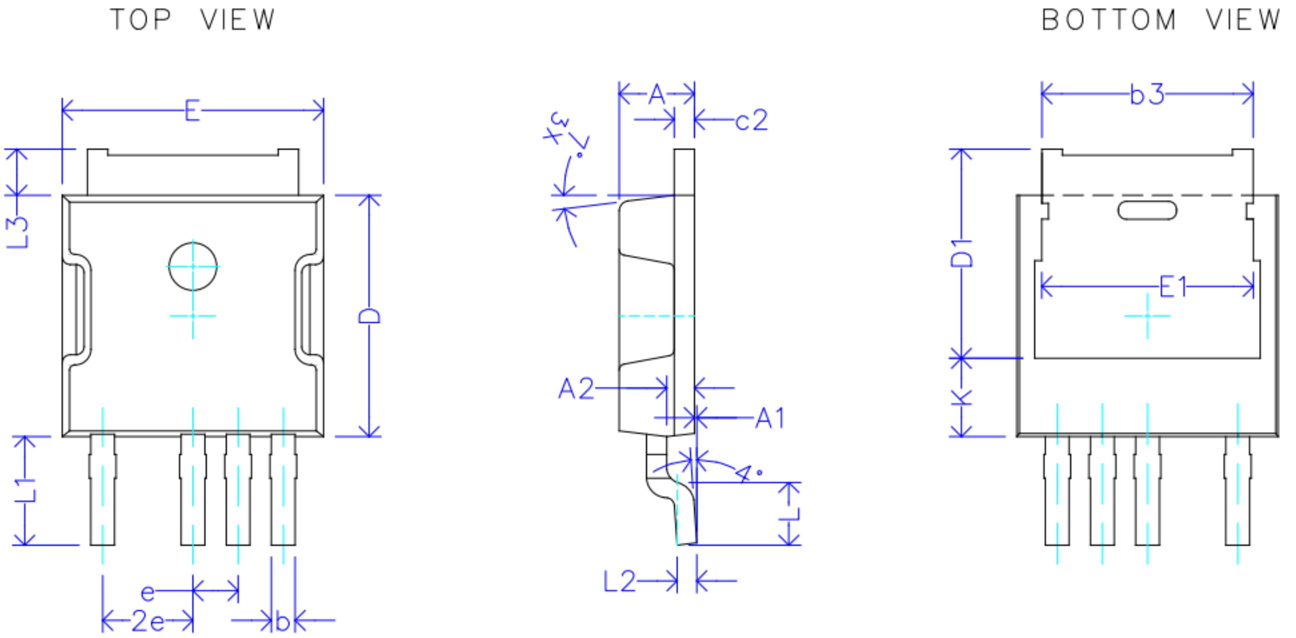
11. Package outline

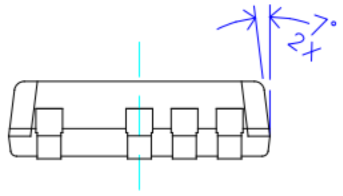




Marking Line	Marking Symbol	Content Description
L1	XXXXXXX	Part Number : First 7 characters of the Navitas Part Number Example : NV6143CP01, XXXXXXX = NV6143C
	TTT	Optional Trim Code : 8th, 9th, and 10th digit of the Navitas Part Number. Example : NV6143CP01, TTT = P01
L2	LLLLLLL	Lot Number : Max 7 digits assembly lot number for marking Example : NC31900
L3	YY	Year Code : Last 2 digits of the year Example : 2023, YY=23
	WW	Week Code : 01 - 53
	N	Supplier Site Code : Y = HYME

11. Package outline (cont.)





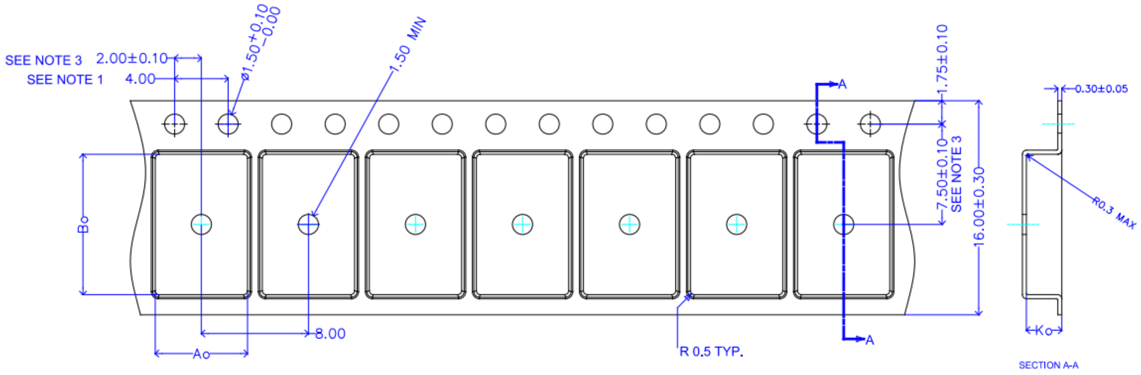
SYMBOL	MIN	NOM	MAX
A	1.80	1.90	2.00
A1	0.00	-	0.20
A2	0.60	0.70	0.80
b	0.508	0.60	0.711
b3	5.21	-	5.46
c2	0.41	0.508	0.61
D	6.00	6.10	6.22
D1	4.90	-	-
E	6.40	6.60	6.73

SYMBOL	MIN	NOM	MAX
E1	5.10	5.30	5.50
e		1.14 BSC	
L	1.34	1.585	1.77
L1		2.743 REF	
L2	0.41	0.508	0.61
L3	0.88	-	1.28
K	1.98	-	-
Package Draft Angles		5-9 degrees	
Foot Angle		0-8 degrees	
Gauge Plane for L		0.508	

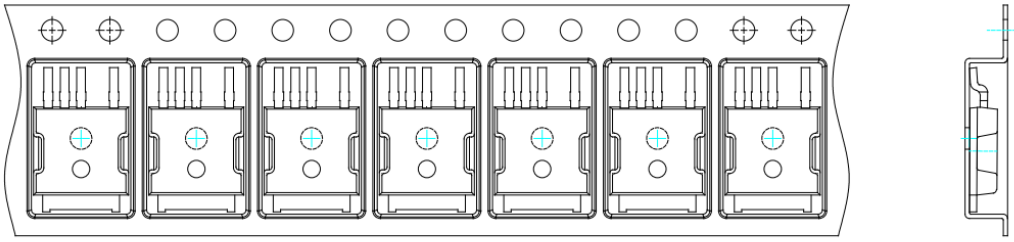
Notes :

1. All dimentions in mm.
2. Reference JEDEC TO-252F VAR AD
3. 100% Sn Plating

12. Tape and Reel Dimensions



Notes	
Ao	6.9
Bo	10.50
Ko	2.65
1. 10 sproket hole pitch cumulative tolerance ±0.2	
2. Camber in compliance with EIA 481	
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.	



Reel Quantity		Pin 1 Orientation
Reel Size	Unit qty in reel	2 1 3 4 Pin 1 on quadrant 1
7 "	500 units	
13 "	2500 units	
Leader and trailer pocket : 50 empty pockets		

13. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Note	Package	MSL Rating	Packing (Tape & Reel)
NV6144CQ01-RA	-55 °C to +150 °C T_J	-55 °C to +150 °C T_{STOR}	Isolated topology	DPAK-4L	3	500 : 7” Reel
NV6144CQ01	-55 °C to +150 °C T_J	-55 °C to +150 °C T_{STOR}	Isolated topology	DPAK-4L	3	2,500 : 13” Reel
NV6144CP01-RA	-55 °C to +150 °C T_J	-55 °C to +150 °C T_{STOR}	Non-isolated topology	DPAK-4L	3	500 : 7” Reel
NV6144CP01	-55 °C to +150 °C T_J	-55 °C to +150 °C T_{STOR}	Non-isolated topology	DPAK-4L	3	2,500 : 13” Reel

14. Revision History

Date	Status	Notes
07-25-2024	Final version	First publication

15. 20-Year Limited Product Warranty

The 20-year limited warranty applies to all packaged Navitas GaNFast Power ICs in mass production, subject to the terms and conditions of, Navitas' express limited product warranty, available at https://navitassemi.com/terms-conditions. The warranted specifications include only the MIN and MAX values only listed in Absolute Maximum Ratings, ESD Ratings and Electrical Characteristics sections of this datasheet. Typical (TYP) values or other specifications are not warranted.

Additional Information

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