Product Change Notification: SYST-03XJWE506

Date:

05-Dec-2024

Product Category:

Memory

Notification Subject:

Data Sheet - SST39SF010A/SST39SF020A/SST39SF040 - 1-Mbit/2-Mbit/4-Mbit (x8) Multi-Purpose Flash

Affected CPNs:

SYST-03XJWE506_Affected_CPN_12052024.pdf
SYST-03XJWE506_Affected_CPN_12052024.csv

Notification Text:

SYST-03XJWE506
Microchip has released a new Datasheet for the SST39SF010A/SST39SF020A/SST39SF040 - 1-Mbit/2-Mbit/4-Mbit (x8) Multi-Purpose Flash of devices. If you are using one of these devices please read the document located at **SST39SF010A/SST39SF020A/SST39SF040 - 1-Mbit/2-Mbit/4-Mbit (x8) Multi-Purpose Flash**. **Notification Status:** Final **Description of Change:**Updated Package Marking section. **Impacts to Data Sheet:** None **Reason for Change:** To improve productivity. **Change Implementation Status:** Complete **Date Document Changes Effective:** 05 Dec 2024

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SST39SF010A/SST39SF020A/SST39SF040 - 1-Mbit/2-Mbit/4-Mbit (x8) Multi-Purpose Flash

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Affected Catalog Part Numbers (CPN)

SST39SF010A-55-4C-NHE
SST39SF010A-55-4C-NHE-T
SST39SF010A-55-4C-WHE
SST39SF010A-55-4C-WHE-T
SST39SF010A-55-4I-NHE
SST39SF010A-55-4I-NHE-T
SST39SF010A-55-4I-WHE
SST39SF010A-55-4I-WHE-T
SST39SF010A-70-4C-NHE
SST39SF010A-70-4C-NHE-T
SST39SF010A-70-4C-PHE
SST39SF010A-70-4C-WHE
SST39SF010A-70-4C-WHE-T
SST39SF010A-70-4I-NHE
SST39SF010A-70-4I-NHE-T
SST39SF010A-70-4I-WHE
SST39SF010A-70-4I-WHE-T
SST39SF020A-55-4C-NHE
SST39SF020A-55-4C-NHE-T
SST39SF020A-55-4C-WHE
SST39SF020A-55-4C-WHE-T
SST39SF020A-55-4I-NHE
SST39SF020A-55-4I-NHE-T
SST39SF020A-55-4I-WHE
SST39SF020A-55-4I-WHE-T
SST39SF020A-70-4C-NHE
SST39SF020A-70-4C-NHE-T
SST39SF020A-70-4C-PHE
SST39SF020A-70-4C-WHE
SST39SF020A-70-4C-WHE-T
SST39SF020A-70-4I-NHE
SST39SF020A-70-4I-NHE-T
SST39SF020A-70-4I-WHE
SST39SF020A-70-4I-WHE-T
SST39SF040-55-4C-NHE
SST39SF040-55-4C-NHE-T
SST39SF040-55-4C-WHE
SST39SF040-55-4C-WHE-T
SST39SF040-55-4I-NHE
SST39SF040-55-4I-NHE-T
SST39SF040-55-4I-WHE
SST39SF040-55-4I-WHE-T
SST39SF040-70-4C-NHE
SST39SF040-70-4C-NHE-T
SST39SF040-70-4C-PHE
SST39SF040-70-4C-WHE

SST39SF040-70-4C-WHE-T

SST39SF040-70-4I-NHE

SST39SF040-70-4I-NHE-T

SST39SF040-70-4I-WHE

SST39SF040-70-4I-WHE-T

SST39SF010A/ SST39SF020A/SST39SF040

1-Mbit/2-Mbit/4-Mbit (x8) Multi-Purpose Flash

Features

- Organized as 128K x 8/256K x 8/512K x 8
- Single 4.5V-5.5V Read and Write Operations
- Superior Reliability:
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years data retention
- Low-Power Consumption (typical values at 14 MHz):
  - Active current: 10 mA (typical)
  - Standby current: 30 µA (typical)
- Sector Erase Capability:
  - Uniform 4-Kbyte sectors
- Fast Read Access Time:
  - 55 ns
  - 70 ns
- Latched Address and Data
- Automatic Write Timing:
  - Internal V_{PP} Generation
- Fast Erase and Byte Program:
  - Sector Erase time: 18 ms (typical)
  - Chip Erase time: 70 ms (typical)
  - Byte Program time: 14 µs (typical)
  - Chip Rewrite time:
    - 2 seconds (typical) for SST39SF010A
    - 4 seconds (typical) for SST39SF020A
    - 8 seconds (typical) for SST39SF040
- End-of-Write Detection:
  - Toggle Bit
  - Data# Polling
- TTL I/O Compatibility
- JEDEC® Standard:
  - Flash EEPROM pinouts and command sets
- All Devices are RoHS Compliant

Packages

- 32-Pin PDIP. 32-Lead PLCC and 32-Lead TSOP

Product Description

The SST39SF010A/020A/040 devices are CMOS Multi-Purpose Flash (MPF) manufactured with Microchip's proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF010A/020A/040 devices write (Program or Erase) with a 4.5V-5.5V power supply and conform to JEDEC® standard pin assignments for x8 memories.

Featuring a high-performance Byte Program, the SST39SF010A/020A/040 devices provide a maximum Byte Program time of 20 µsec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent writes, they have on-chip hardware and software data protection schemes.

The SST39SF010A/020A/040 devices provide superior reliability, being designed, manufactured and tested for a wide spectrum of applications.

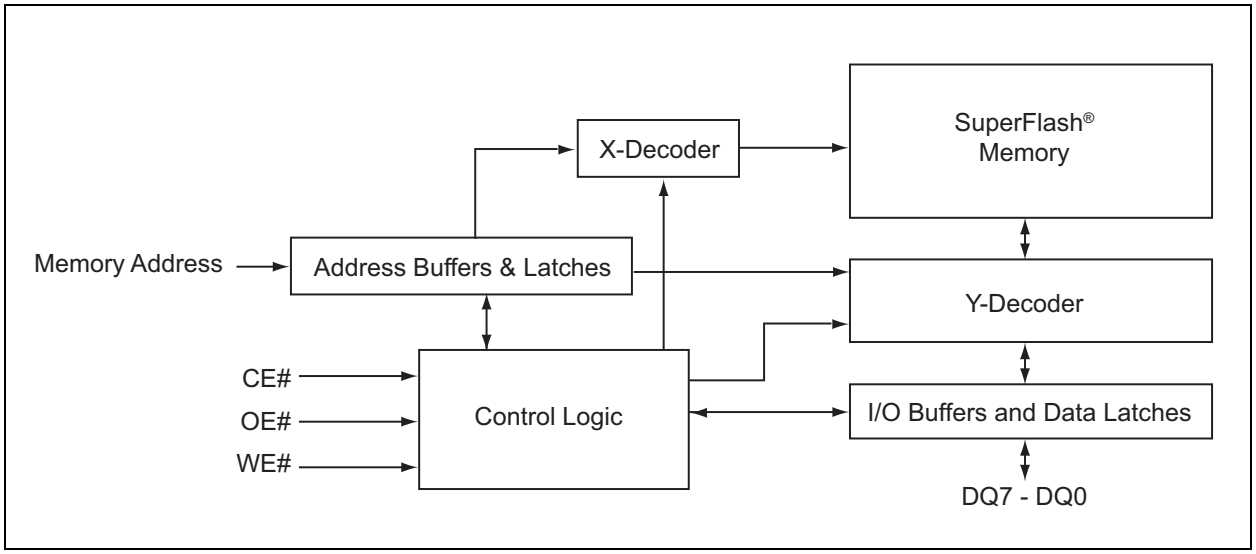
These devices are suited for applications that require convenient and economical updating of program, configuration or data memory. For all system applications, they significantly improve performance and reliability while lowering power consumption. They inherently use less energy during Erase and Program times than alternative Flash technologies. The total energy consumed is a function of the applied voltage, current and time of application. Since, for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative Flash technologies. These devices also improve flexibility while lowering the cost for program, data and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or derated as is necessary with alternative Flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

See Figure 2-1 for pin assignments and Table 2-1 for pin descriptions.

1.0 BLOCK DIAGRAM

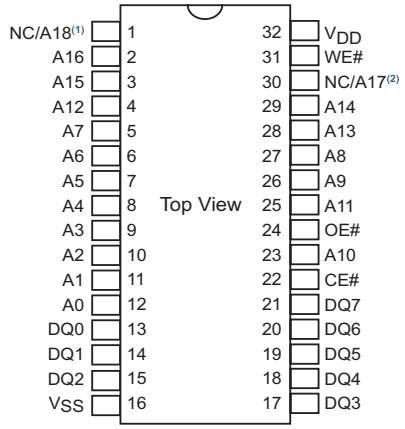
FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

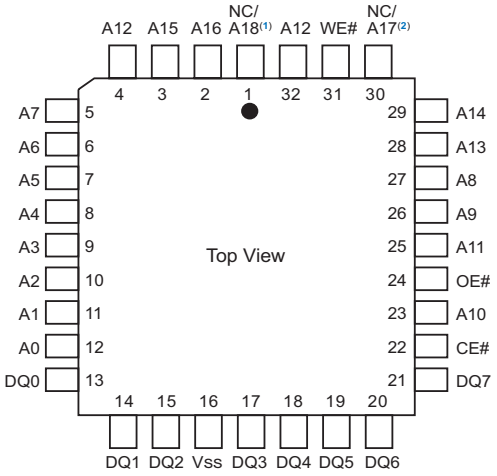
FIGURE 2-1: PIN ASSIGNMENTS

PIN ASSIGNMENT FOR 32-LEAD PDIP



Note 1: Pin 1 is NC for SST39SF010A and SST39SF020A and A18 for SST39SF040.
2: Pin 30 is NC for SST39SF010A and A17 for SST39SF020A and SST39SF040.

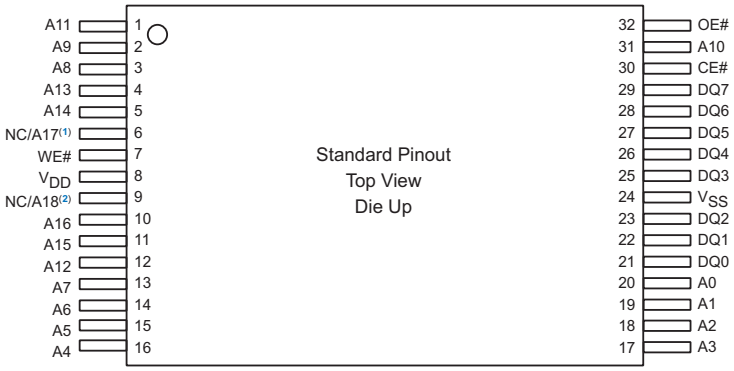
PIN ASSIGNMENT FOR 32-LEAD PLCC



Note 1: Pin 1 is NC for SST39SF010A and SST39SF020A and A18 for SST39SF040.

2: Pin 30 is NC for SST39SF010A and A17 for SST39SF020A and SST39SF040.

PIN ASSIGNMENT FOR 32-LEAD TSOP



Note 1: Pin 6 is NC for SST39SF010A and A17 for SST39SF020A and SST39SF040.

2: Pin 9 is NC for SST39SF010A and SST39SF020A and A18 for SST39SF040.

TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}[1]-A0	Address Inputs	Provide memory addresses. During Sector Erase A_{MS}-A12 address lines will select the sector.
DQ7-DQ0	Data Input/Output	Output data during Read cycles and receive input data during Write cycles. Data are internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	Activate the device when CE# is low.
OE#	Output Enable	Gate the data output buffers.
WE#	Write Enable	Control the Write operations.
V_{DD}	Power Supply	Provide power supply voltage: 4.5V-5.5V.
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

Note 1: A_{MS} = Most significant address
A_{MS} = A16 for SST39SF010A, A17 for SST39SF020A and A18 for SST39SF040

3.0 DEVICE OPERATION

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

3.1 Read

The Read operation of the SST39SF010A/020A/040 is controlled by CE# and OE#, and both must be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in a high-impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram (Figure 7-1) for further details.

3.2 Byte Program Operation

The SST39SF010A/020A/040 devices are programmed on a byte-by-byte basis. Before programming, the sector containing the byte must be completely erased. The Program operation is accomplished in three steps.

1. The first step is the three-byte load sequence for Software Data Protection.
2. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data are latched on the rising edge of either CE# or WE#, whichever occurs first.
3. The third step is the internal Program operation, which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first.

Once initiated, the Program operation will be completed within 20 µs. See Figure 7-2 and Figure 7-3 for WE# and CE# controlled Program operation timing diagrams and Figure 7-12 for a flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

3.3 Sector Erase Operation

The Sector Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 Kbytes. The Sector Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector Erase command (30H) and Sector Address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 7-6 for timing waveforms. Any commands written during the Sector Erase operation will be ignored.

3.4 Chip Erase Operation

The SST39SF010A/020A/040 devices provide Chip Erase operation, which allows the user to erase the entire memory array to the '1's state. This is useful when the entire device must be quickly erased.

The Chip Erase operation is initiated by executing a six- byte Software Data Protection command sequence with Chip Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4-2 for the command sequence, Figure 7-7 for the timing diagram and Figure 7-15 for the flowchart. Any commands written during the Chip Erase operation will be ignored.

3.5 Write Operation Status Detection

The SST39SF010A/020A/040 devices offer two software methods to detect the completion of a Write (Program or Erase) cycle, thereby optimizing the system's Write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system. Therefore, Data# Polling or Toggle Bit maybe be read concurrently with the completion of the write cycle. If this occurs, the system may receive incorrect results from the status detection process. For example, valid data may appear to conflict with either DQ7 or DQ6. To prevent false results upon detection of failures, the software routine should loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle; otherwise the failure is valid.

3.6 Data# Polling (DQ7)

When the SST39SF010A/020A/040 devices are undergoing an internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. Note that even though DQ7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid. Valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During an internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase operation is completed, DQ7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip Erase, Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7-4 for the Data# Polling timing diagram and Figure 7-13 for a flowchart.

3.7 Toggle Bit (DQ6)

During the internal Program or Erase operation, consecutive attempts to read DQ6 will produce alternating '0's and '1's, i.e., toggling between '0' and '1'. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7-5 for the Toggle Bit timing diagram and Figure 7-13 for a flowchart.

3.8 Data Protection

The SST39SF010A/020A/040 devices provide both hardware and software features to protect nonvolatile data from inadvertent writes.

3.9 Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power-Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high or WE# high will inhibit the Write operation, preventing inadvertent writes during power-up or power-down.

3.10 Software Data Protection (SDP)

The SST39SF010A/020A/040 devices provide the JEDEC®-approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence.

The SST39SF010A/020A/040 devices are shipped with the Software Data Protection permanently enabled. See Table 4-2 for the specific software command codes. During the SDP command sequence, invalid commands will abort the device to Read mode, within T_{RC}.

3.11 Product Identification

The Product Identification mode identifies the device as the SST39SF010A, SST39SF020A or SST39SF040 and the manufacturer as Microchip. This mode may be accessed through software operations. Users may wish to utilize the software Product Identification operation to identify the part (i.e., using the device ID) when multiple manufacturers are used in the same socket. For further details, see Table 4-2 for software operation, Figure 7-8 for the software ID Entry and Read timing diagram and Figure 7-14 for the ID Entry command sequence flowchart.

TABLE 3-1: PRODUCT IDENTIFICATION

		Address	Data
Manufacturer's ID		0000H	BFH
Device ID:	SST39SF010A	0001H	B5H
	SST39SF020A	0001H	B6H
	SST39SF040	0001H	B7H

3.12 Product Identification Mode Exit/Reset

To return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4-2 for the software command codes, Figure 7-9 for the timing waveform and Figure 7-14 for a flowchart.

4.0 OPERATIONS

TABLE 4-1: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X(1)	Sector or block address, XXH for Chip Erase
Standby	V_{IH}	X	X	High-Z	X
Write Inhibit	X	V_{IL}	X	High-Z/D_{OUT}	X
	X	X	V_{IH}	High-Z/D_{OUT}	X
Product Identification					
Software Mode	V_{IL}	V_{IH}	V_{IL}		see Table 4-2

Note 1: X can be V_{IL} or V_{IH}, but no other value.

TABLE 4-2: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr(1)	Data(2)	Addr(1)	Data(2)	Addr(1)	Data(2)	Addr(1)	Data(2)	Addr(1)	Data(2)	Addr(1)	Data(2)
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA(2)					
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_X(3)	30H
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry(4,5)	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit(6)	XXH	F0H										
Software ID Exit(6)	555H	AAH	2AAAH	55H	5555H	F0H						

Note 1: Address format A14-A0 (Hex), Addresses A_{MS}- A15 can be V_{IL} or V_{IH}, but no other value, for the command sequence.
A_{MS} = Most significant address
A_{MS} = A16 for SST39SF010A, A17 for SST39SF020A and A18 for SST39SF040

2: BA = Program Byte address.

3: SAx for Sector Erase; uses A_{MS} = A12 address lines.

4: The device does not remain in Software Product ID Mode if powered down.

5: With A_{MS}-A1 = 0; SST Manufacturer's ID = BFH, is read with A0 = 0,
SST39SF010A Device ID = B5H, is read with A0 = 1.
SST39SF020A Device ID = B6H, is read with A0 = 1.
SST39SF040 Device ID = B7H, is read with A0 = 1.

6: Both Software ID Exit operations are equivalent.

5.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
DC voltage on any pin to ground potential ..... -0.5V to V_{DD}+0.5V
Transient voltage (<20 ns) on any pin to ground potential ..... -2.0V to V_{DD}+2.0V
Voltage on A9 pin to ground potential ..... -0.5V to 13.2V
Package power dissipation capability (T_A = +25°C) 1W
Through hold lead soldering temperature (10 seconds) ..... +300°C
Surface mount lead soldering temperature (3 seconds) ..... +240°C
Output short circuit current[1] ..... 100 mA

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 5-1: OPERATING RANGE

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	4.5V-5.5V
Industrial	-40°C to +85°C	4.5V-5.5V

TABLE 5-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
5 ns	C_L = 30 pF for 55 ns
	C_L = 100 pF for 70 ns

Note 1: See Figure 7-10 and Figure 7-11.

6.0 DC CHARACTERISTICS

TABLE 6-1: DC OPERATING CHARACTERISTICS (V_{DD} = 4.5V-4.5V)[1]

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{DD}	Power Supply Current	—	—		Address Input = V_{ILT}/V_{ILT}, @ f = 1/T_{RC} minimum V_{DD} = V_{DD} maximum
	Read[2]	—	25	mA	CE# = V_{IL}, OE# = WE# = V_{IH} all I/Os open
	Program and Erase	—	35	mA	CE# = WE# = V_{IL}, OE# = V_{IH}
I_{SB1}	Standby Current V_{DD} (TTL input)	—	3	mA	CE# = V_{IH}, V_{DD} = V_{DD} maximum
I_{SB2}	Standby Current V_{DD} (CMOS input)	—	100	µA	CE# = V_{IHC}, V_{DD} = V_{DD} maximum
I_{LI}	Input Leakage Current	—	1	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} maximum
I_{LO}	Output Leakage Current	—	10	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} maximum
V_{IL}	Input Low Voltage	—	0.8	V	V_{DD} = V_{DD} minimum
V_{IH}	Input High Voltage	2.0	—	V	V_{DD} = V_{DD} maximum
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3	—	V	V_{DD} = V_{DD} maximum
V_{OL}	Output Low Voltage	—	0.4	V	I_{OL} = 2.1 mA, V_{DD} = V_{DD} minimum
V_{OH}	Output High Voltage	2.4	—	V	I_{OH} = 400 µA, V_{DD} = V_{DD} minimum

Note 1: Typical conditions for the Active Current shown on the front page of the data sheet are average values at +25°C (room temperature) and V_{DD} = 5V for SF devices. Not 100% tested.

2: Values are for 70 ns conditions. See the *Multi-Purpose Flash Power Rating* application note for further information.

TABLE 6-2: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-Up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-Up to Erase/Program Operation	100	µs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-3: CAPACITANCE (T_A = +25°C, F = 1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-4: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Unit	Test Method
N_{END}[1,2]	Endurance	10,000	Cycles	JEDEC® Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC® Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC® Standard A78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

2: N_{END} endurance rating is qualified as 10,000 cycles minimum for the whole device. A sector or block level rating would result in a higher minimum specification.

7.0 AC CHARACTERISTICS

TABLE 7-1: READ CYCLE TIMING PARAMETERS (V_{DD} = 4.5V-5.5V)

Symbol	Parameter	SST39SF010A/020A/040–55		SST39SF010A/020A/040–70		Unit
		Minimum	Maximum	Minimum	Maximum	
T_{RC}	Read Cycle Time	55	—	70	—	ns
T_{CE}	Chip Enable Access Time	—	55	—	70	ns
T_{AA}	Address Access Time	—	55	—	70	ns
T_{OE}	Output Enable Access Time	—	35	—	35	ns
T_{CLZ}(1)	CE# Low to Active Output	0	—	0	—	ns
T_{OLZ}(1)	OE# Low to Active Output	0	—	0	—	ns
T_{CHZ}(1)	CE# High to High-Z Output	—	20	—	25	ns
T_{OHZ}(1)	OE# High to High-Z Output	—	20	—	25	ns
T_{OH}(1)	Output Hold from Address Change	0	—	0	—	ns

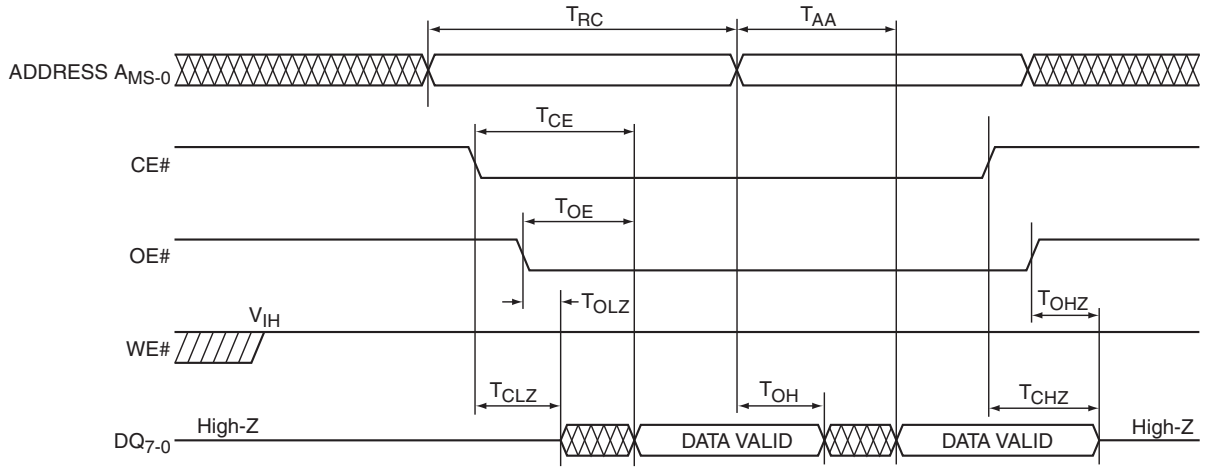
Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7-2: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Minimum	Maximum	Unit
T_{BP}	Byte Program Time	—	10	µs
T_{AS}	Address Setup Time	0	—	ns
T_{AH}	Address Hold Time	30	—	ns
T_{CS}	WE# and CE# Setup Time	0	—	ns
T_{CH}	WE# and CE# Hold Time	0	—	ns
T_{OES}	OE# High Setup Time	0	—	ns
T_{OEH}	OE# High Hold Time	10	—	ns
T_{CP}	CE# Pulse Width	40	—	ns
T_{WP}	WE# Pulse Width	40	—	ns
T_{WPH}(1)	WE# Pulse Width High	30	—	ns
T_{CPH}(1)	CE# Pulse Width High	30	—	ns
T_{DS}	Data Setup Time	40	—	ns
T_{DH}(1)	Data Hold Time	0	—	ns
T_{IDA}(1)	Software ID, Bypass Entry and Exit Times	—	150	ns
T_{SE}	Sector Erase	—	25	ms
T_{SCE}	Chip Erase	—	100	ms

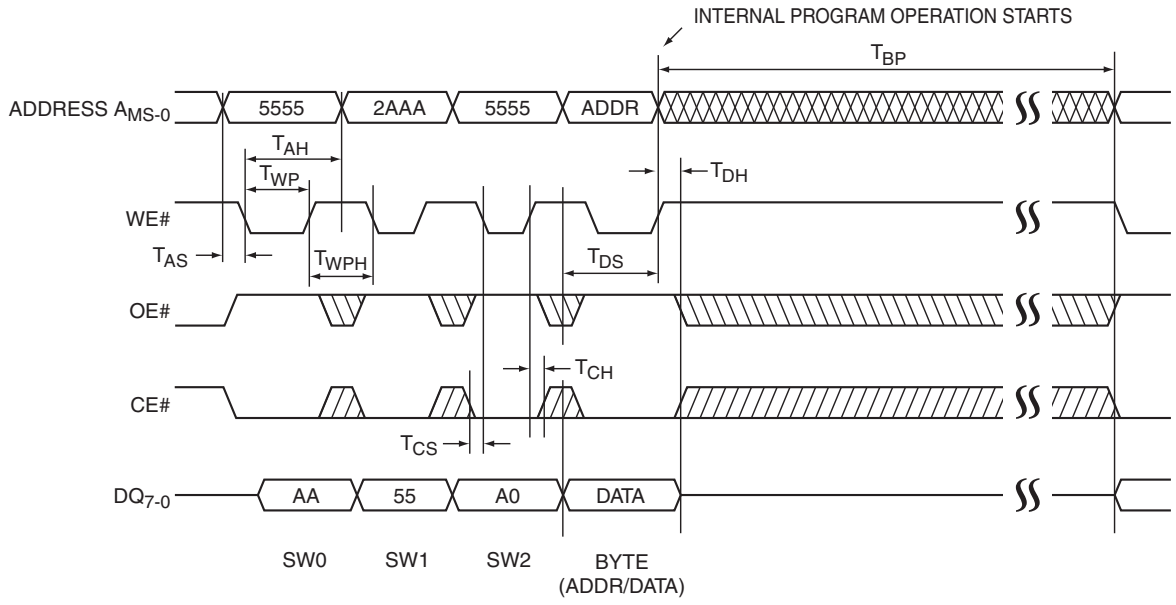
Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 7-1: READ CYCLE TIMING DIAGRAM



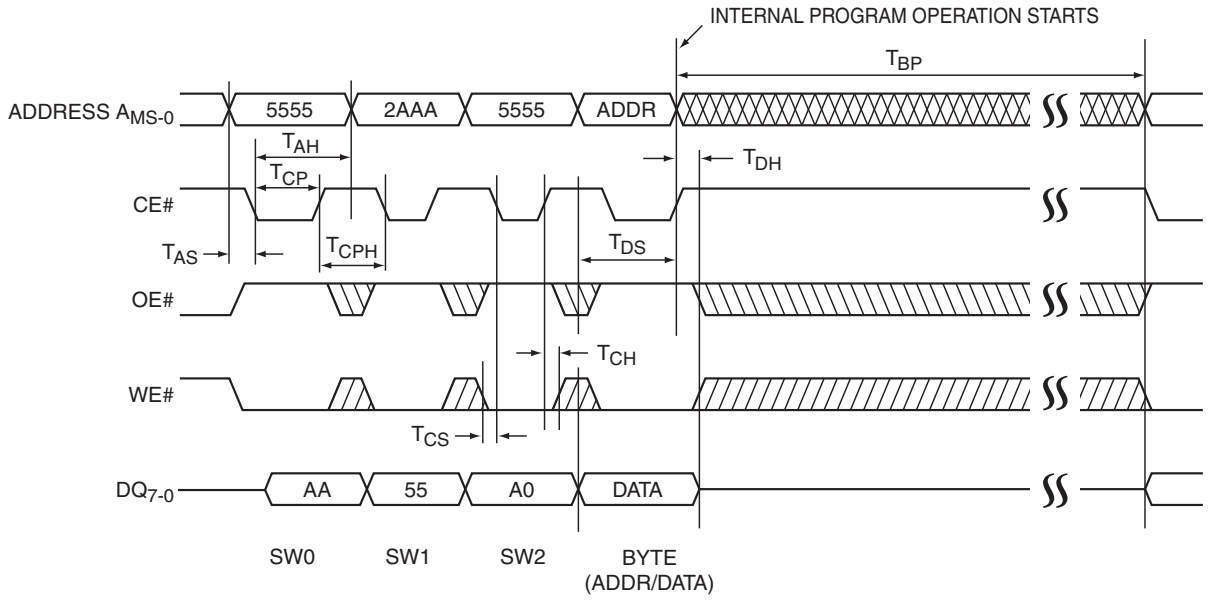
Note 1: AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A and A18 for SST39SF040

FIGURE 7-2: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



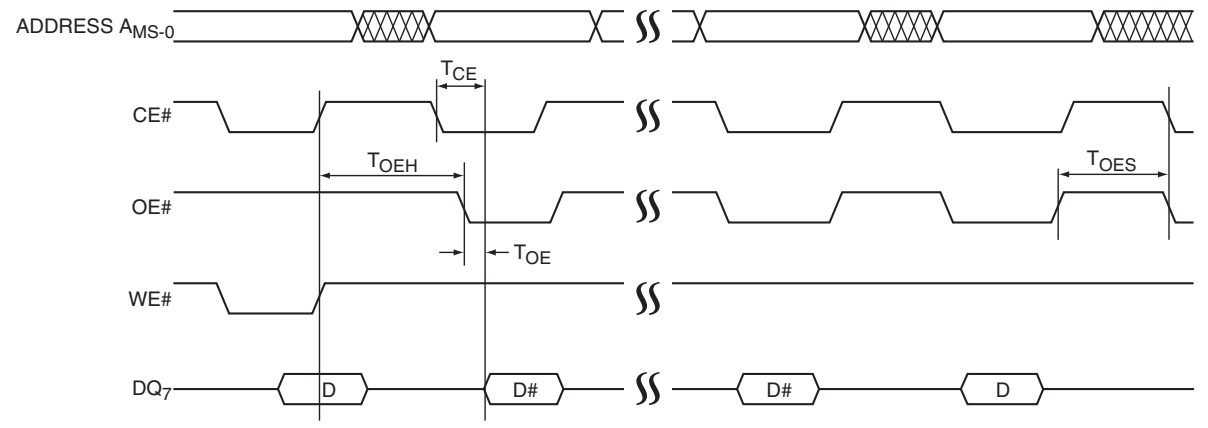
Note 1: AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A and A18 for SST39SF040

FIGURE 7-3: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



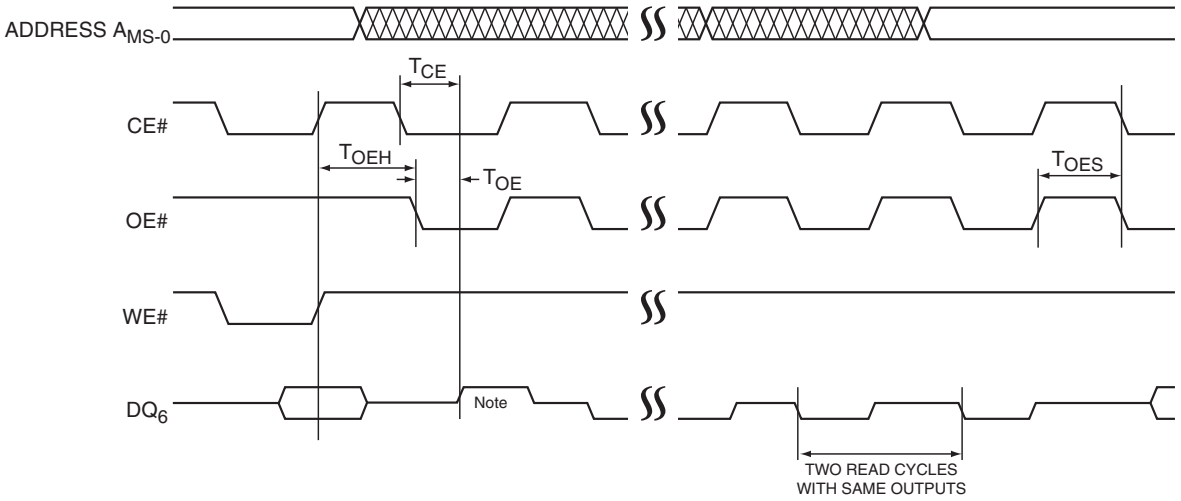
Note 1: AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A and A18 for SST39SF040

FIGURE 7-4: DATA# POLLING TIMING DIAGRAM



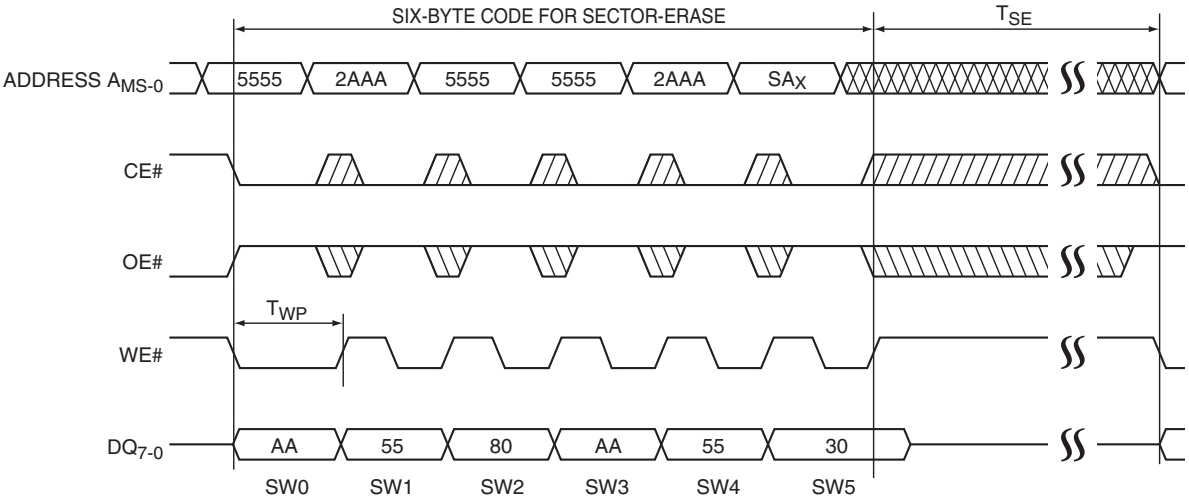
Note 1: AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A and A18 for SST39SF040

FIGURE 7-5: TOGGLE BIT TIMING DIAGRAM



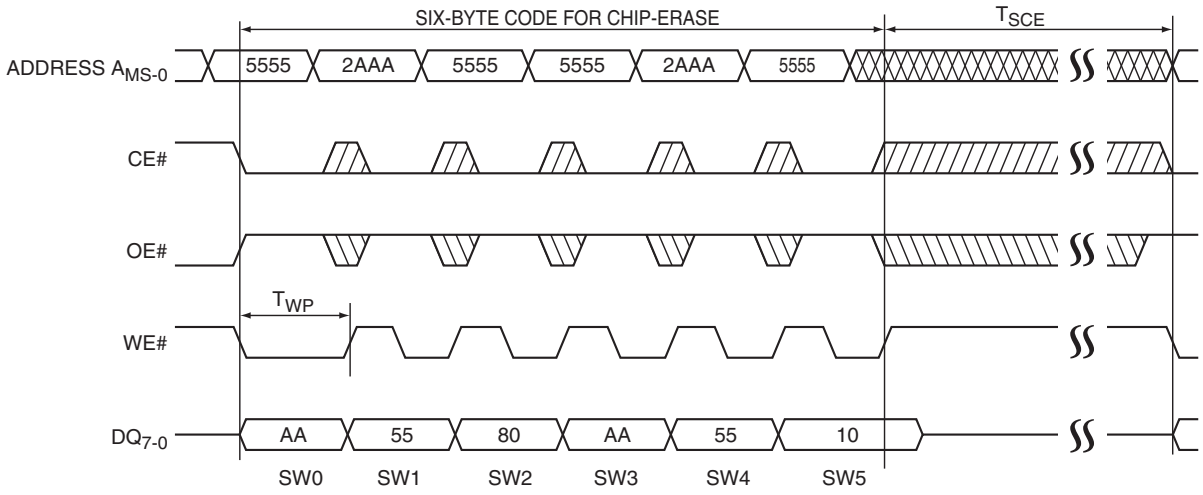
Note 1: Toggle bit output is always high first.
AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A and A18 for SST39SF040

FIGURE 7-6: WE# CONTROLLED SECTOR ERASE TIMING DIAGRAM



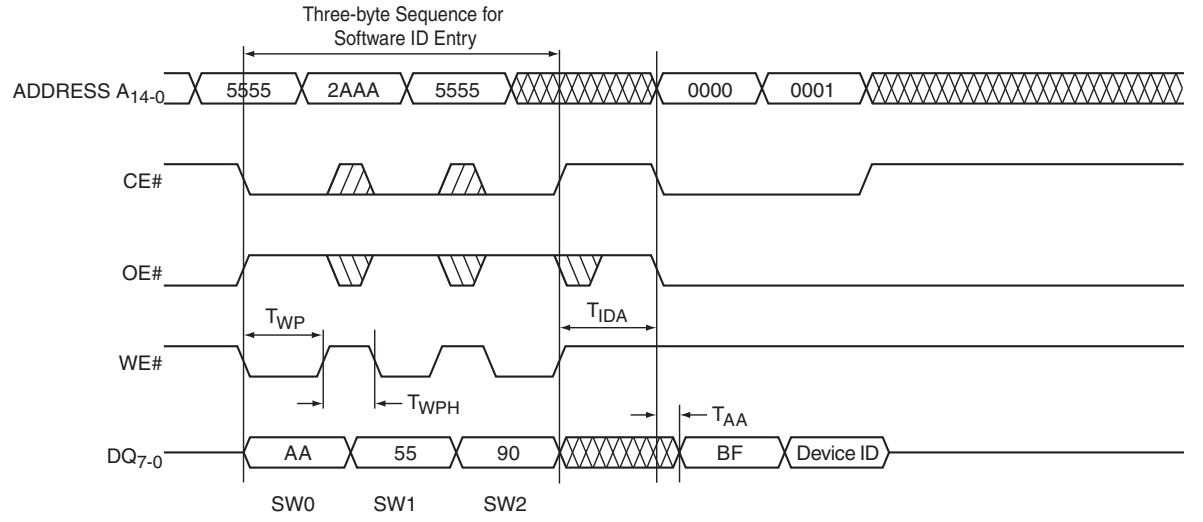
Note 1: This device also supports CE# controlled Sector Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met (see Table 6-4).
SAXX = Sector Address
Toggle bit output is always high first.
AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A and A18 for SST39SF040

FIGURE 7-7: WE# CONTROLLED CHIP ERASE TIMING DIAGRAM



Note 1: This device also supports CE# controlled Chip Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met (see Table 6-4).
SAXX = Sector Address
Toggle bit output is always high first.
AMS = Most significant address

FIGURE 7-8: SOFTWARE ID ENTRY AND READ



Note 1: Device ID = B5H for SST39SF010A, B6H for SST39SF020A and B7H for SST39SF040

FIGURE 7-9: SOFTWARE ID EXIT AND RESET

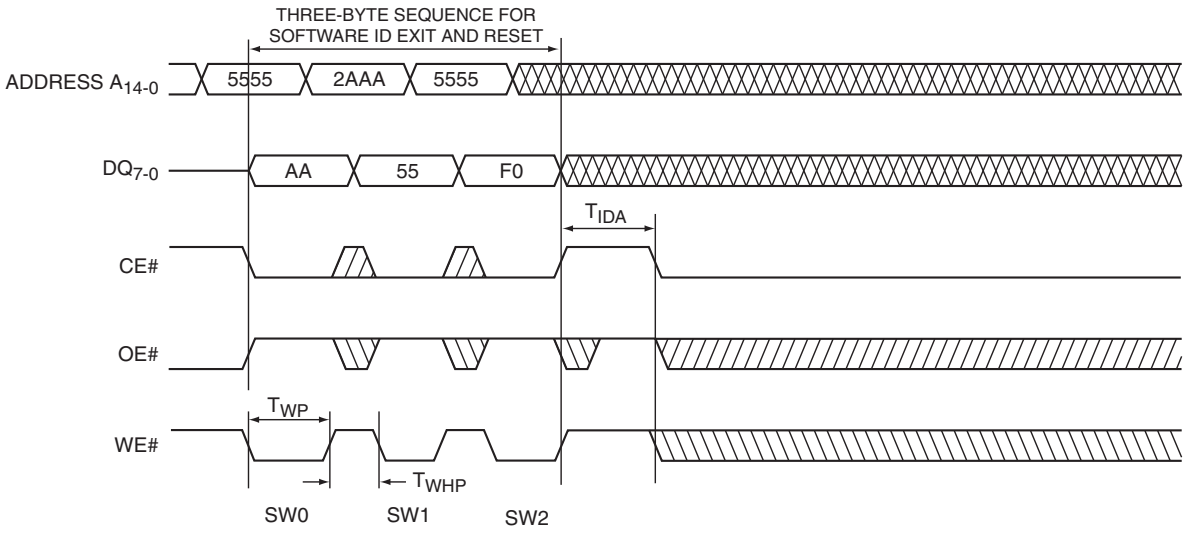
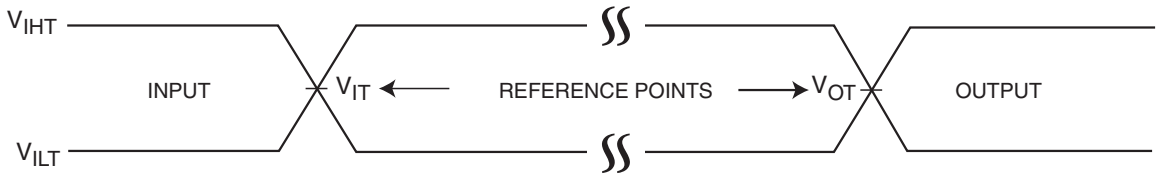


FIGURE 7-10: AC INPUT/OUTPUT REFERENCE WAVEFORMS



Note 1: AC test inputs are driven at VIHT (3.0V) for a logic '1' and VILT (0V) for a logic '0'. Measurement reference points for inputs and outputs are VIT (1.5V) and VOT (1.5 V). Input rise and fall times (10% ↔ 90%) are <5 ns.

2: VIT = VINPUT Test
VOT = VOUTPUT Test
VIHT = VINPUT HIGH Test
VILT = VINPUT LOW Test

FIGURE 7-11: A TEST LOAD EXAMPLE

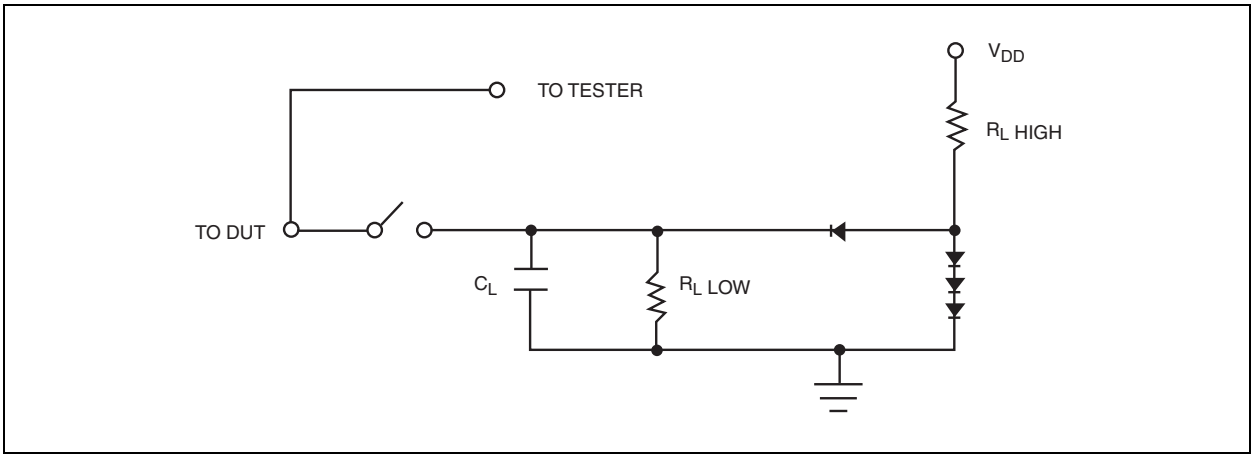


FIGURE 7-12: BYTE PROGRAM ALGORITHM

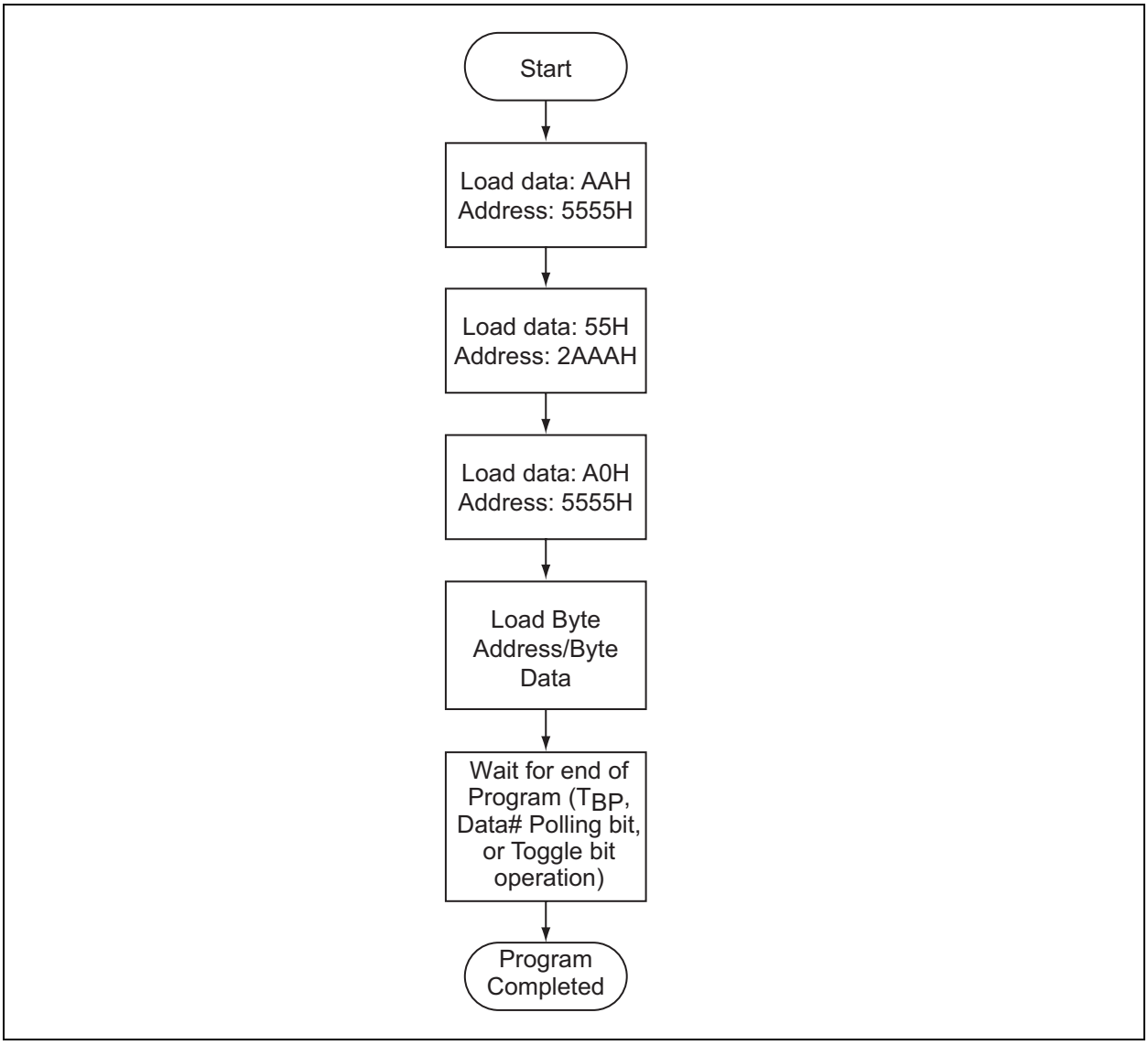


FIGURE 7-13: WAIT OPTIONS

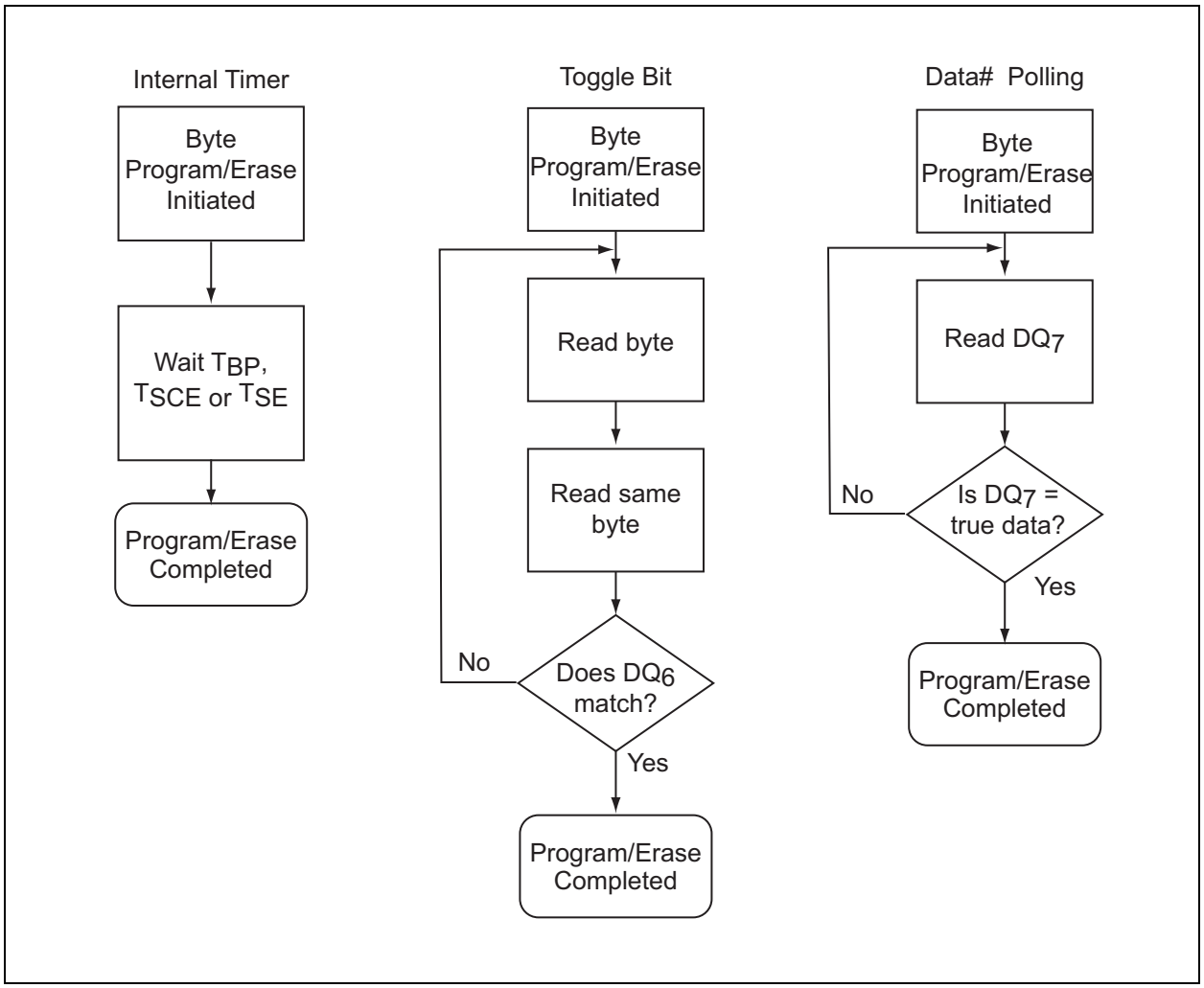


FIGURE 7-14: SOFTWARE PRODUCT COMMAND FLOWCHARTS

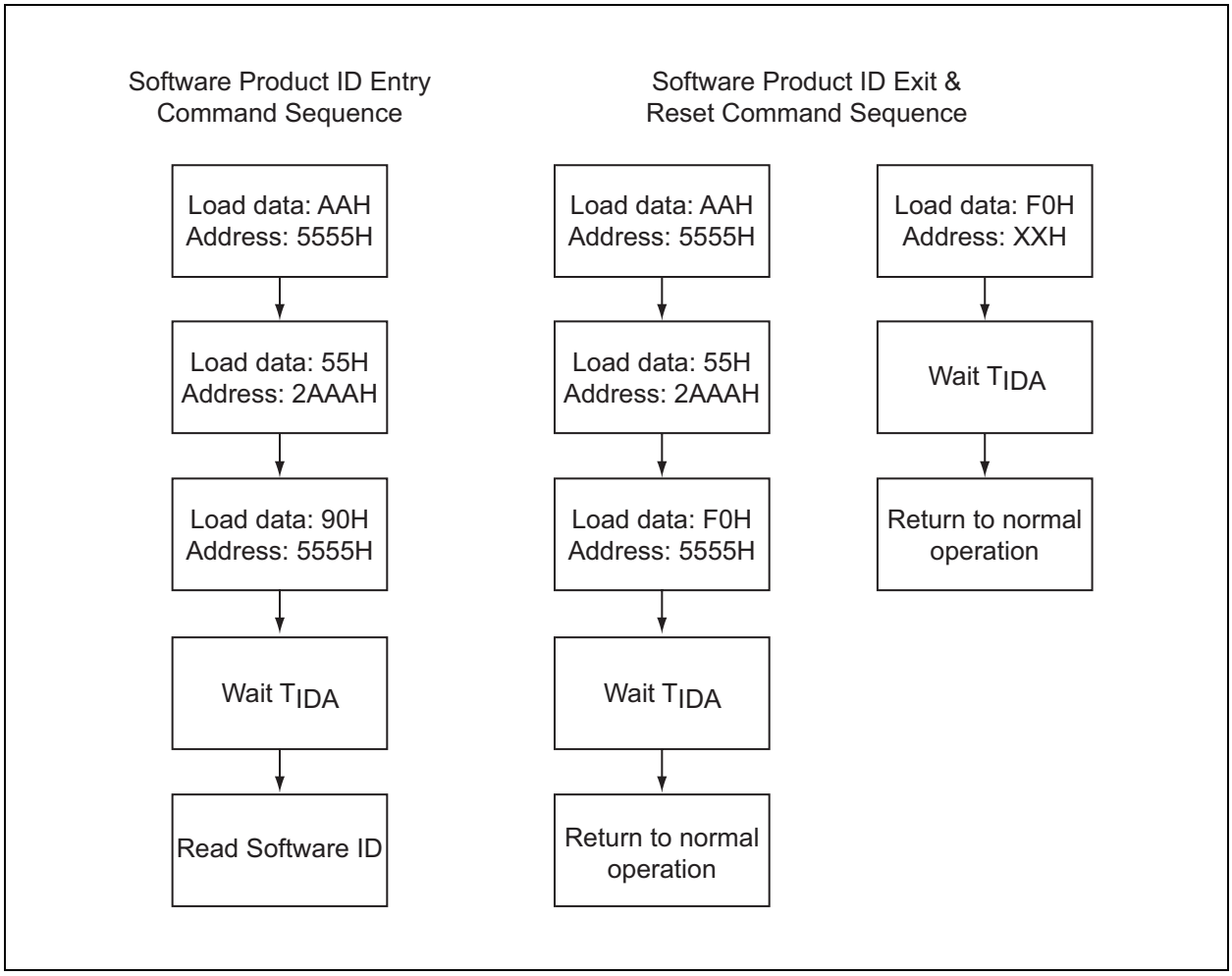
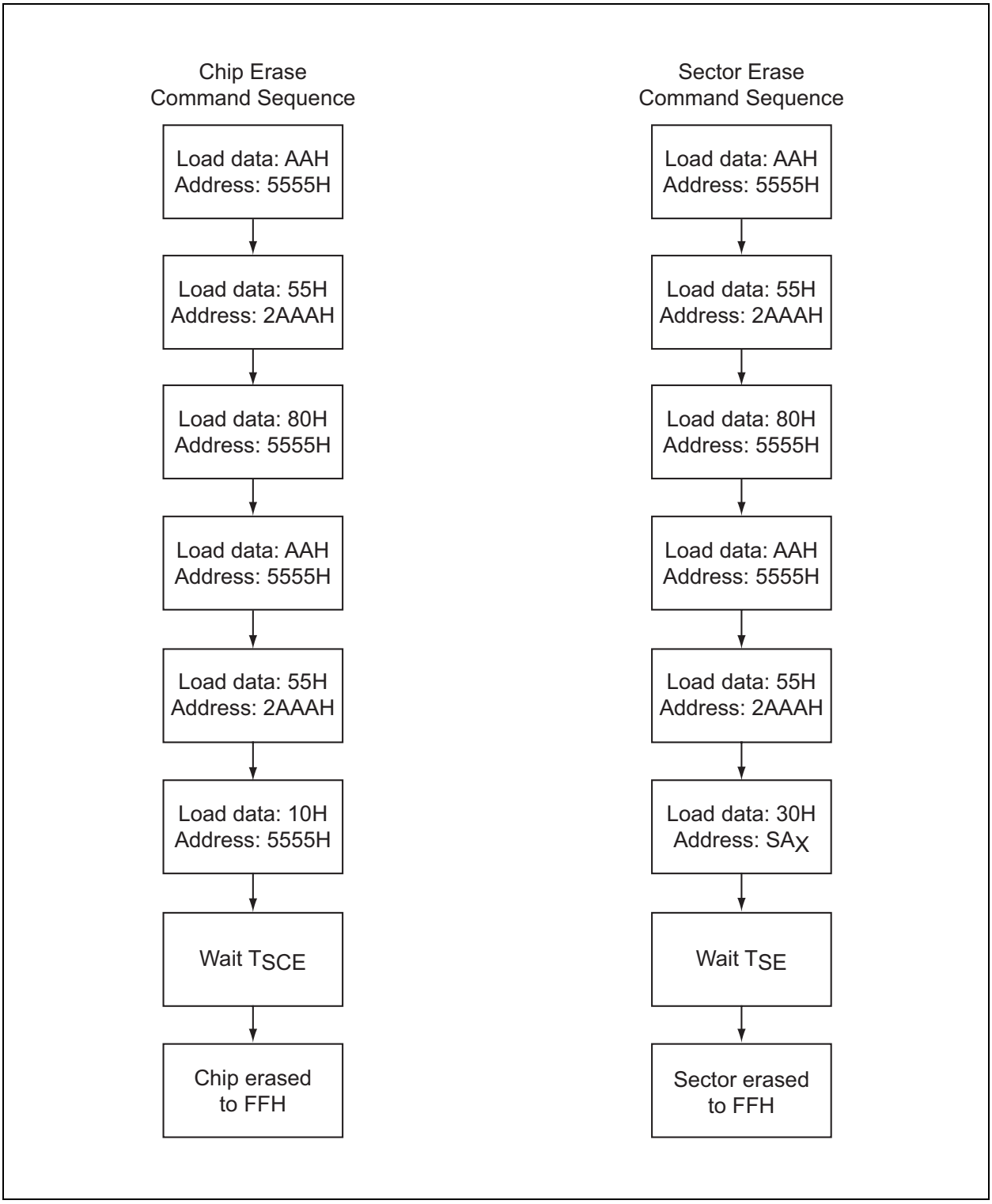


FIGURE 7-15: ERASE COMMAND SEQUENCE



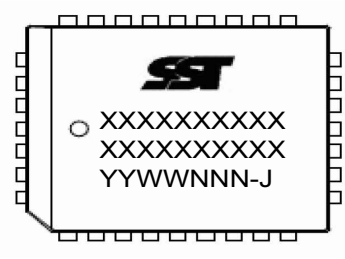
8.0 PACKAGING INFORMATION

8.1 Package Marking

32-Lead PDIP

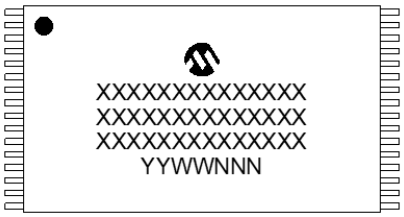
Example

32-Lead PLCC



Example

32-Lead TSOP



Example

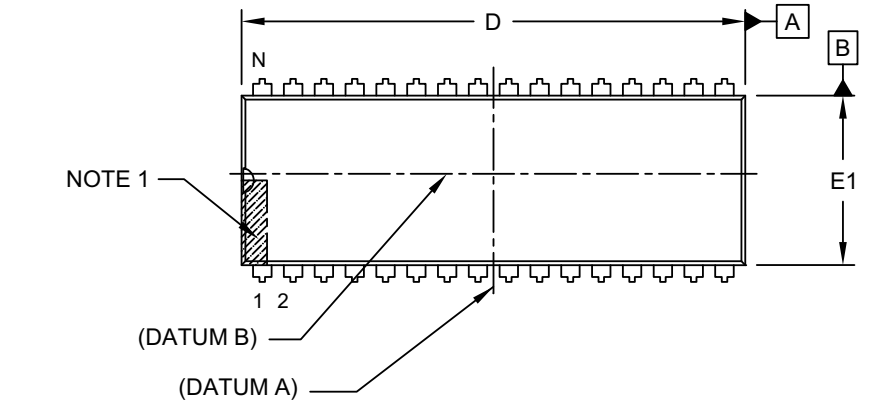
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

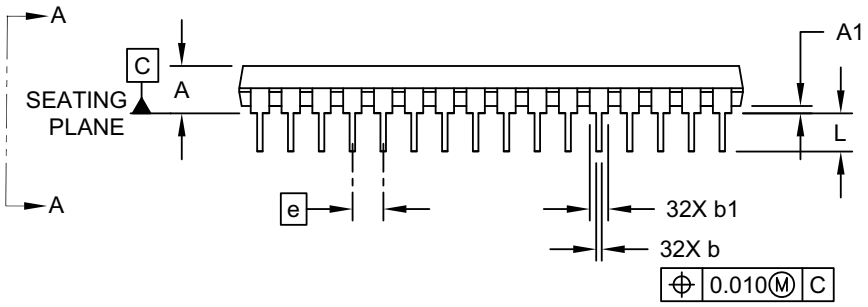
9.0 PACKAGING DIAGRAMS

32-Lead Plastic Dual In-Line (P2X) - 600 mil Body [PDIP]

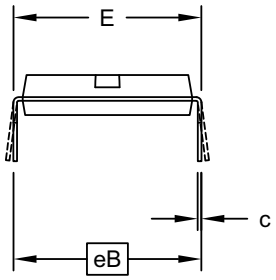
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

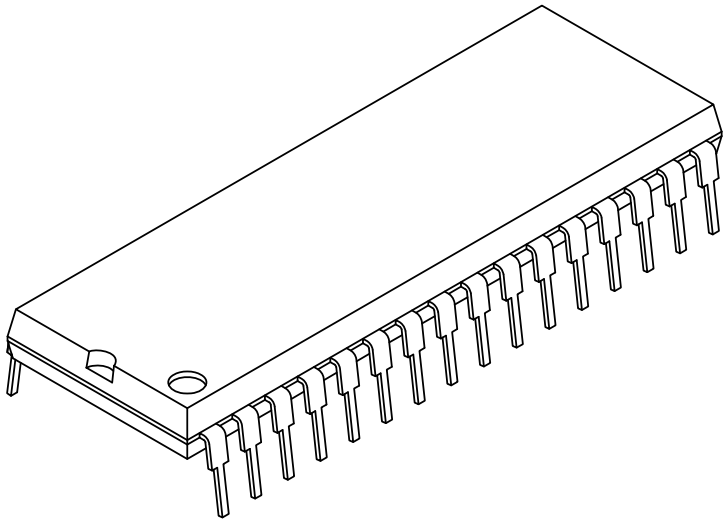


VIEW A-A

Microchip Technology Drawing C04-106-P2X Rev A Sheet 1 of 2

32-Lead Plastic Dual In-Line (P2X) - 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		32	
Pitch	e		.100 BSC	
Top to Seating Plane	A	.170	-	.200
Base to Seating Plane	A1	.015	-	.050
Shoulder to Shoulder Width	E	.600	-	.625
Molded Package Width	E1	.530	-	.550
Overall Length	D	1.645	-	1.655
Tip to Seating Plane	L	.120	-	.150
Lead Thickness	c	.008	-	.012
Upper Lead Width	b1	.045	-	.065
Lower Lead Width	b	.016	-	.022
Overall Row Spacing §	eB		.600 BSC	

Notes:

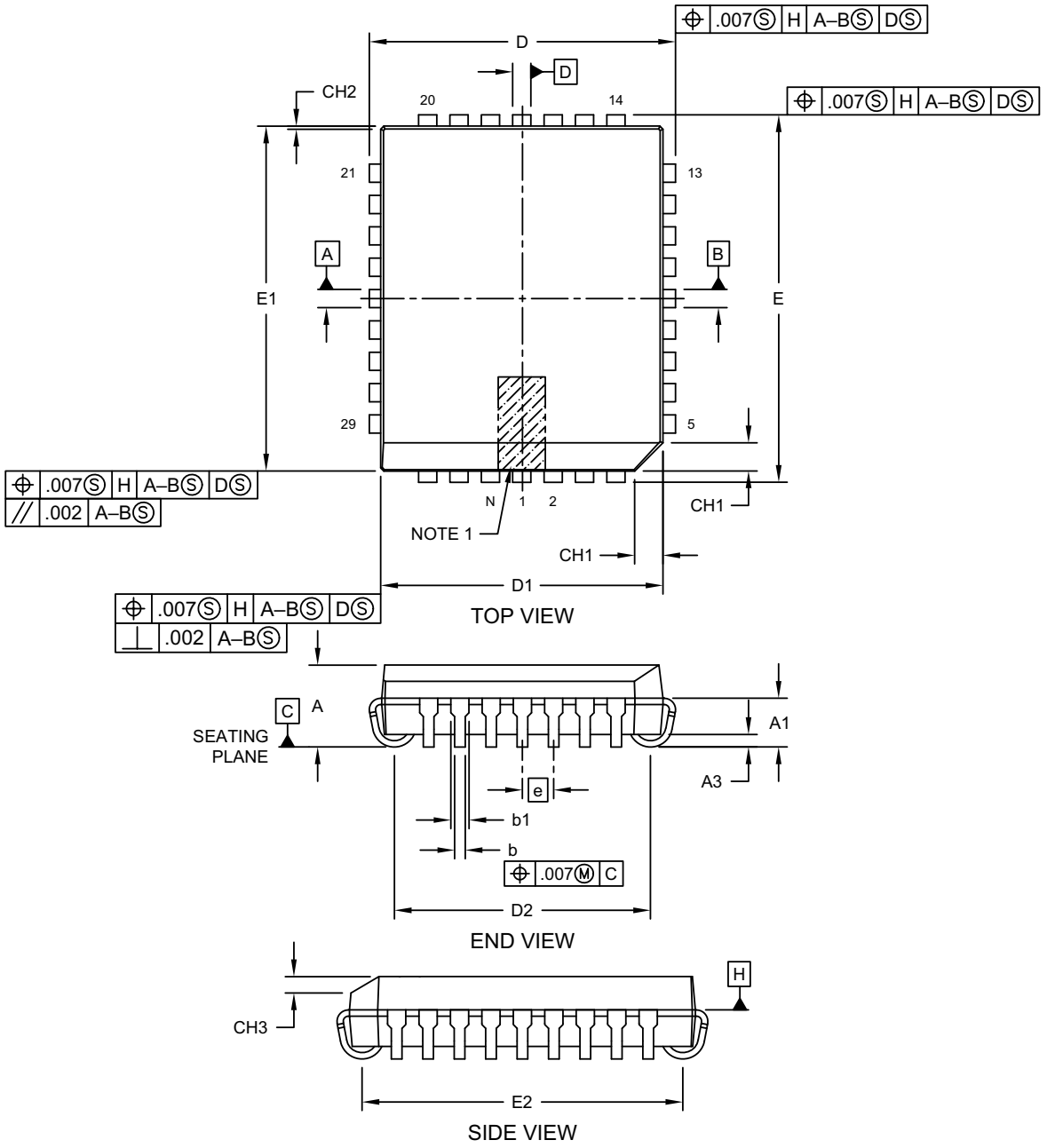
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-106-P2X Rev A Sheet 2 of 2

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

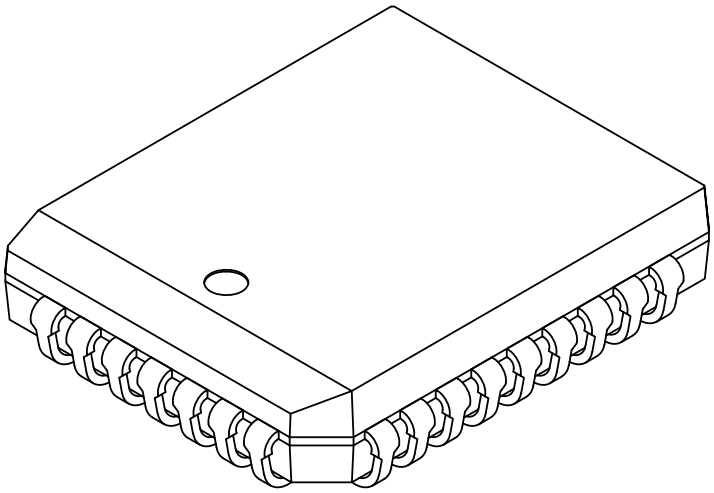
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-023 Rev C Sheet 1 of 2

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		32	
Pitch	e		.050 BSC	
Pins along Length	ND		7	
Pins along Width	NE		9	
Overall Height	A	.125	.132	.140
Contact Height	A1	.060	.0775	.095
Standoff §	A3	.015	-	-
Corner Chamfer	CH1	.042	.045	.048
Chamfers	CH2	-	-	.020
Side Chamfer Height	CH3	.023	.026	.029
Overall Length	D	.485	.490	.495
Overall Width	E	.585	.590	.595
Molded Package Length	D1	.447	.450	.453
Molded Package Width	E1	.547	.550	.553
Footprint Length	D2	.376	.411	.446
Footprint Width	E2	.476	.511	.546
Lead Thickness	c	.008	.010	.013
Upper Lead Width	b1	.026	.029	.032
Lower Lead Width	b	.013	.017	.021

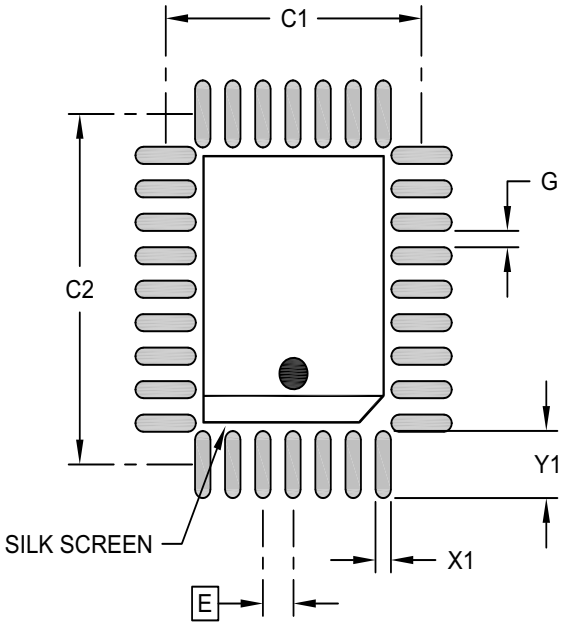
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-023 Rev C Sheet 2 of 2

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		.050 BSC	
Contact Pad Spacing	C1		.425	
Contact Pad Spacing	C2		.524	
Contact Pad Width (X32)	X1			.026
Contact Pad Length (X32)	Y1			.100
Contact Pad to Center Pad (X28)	G	.008		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

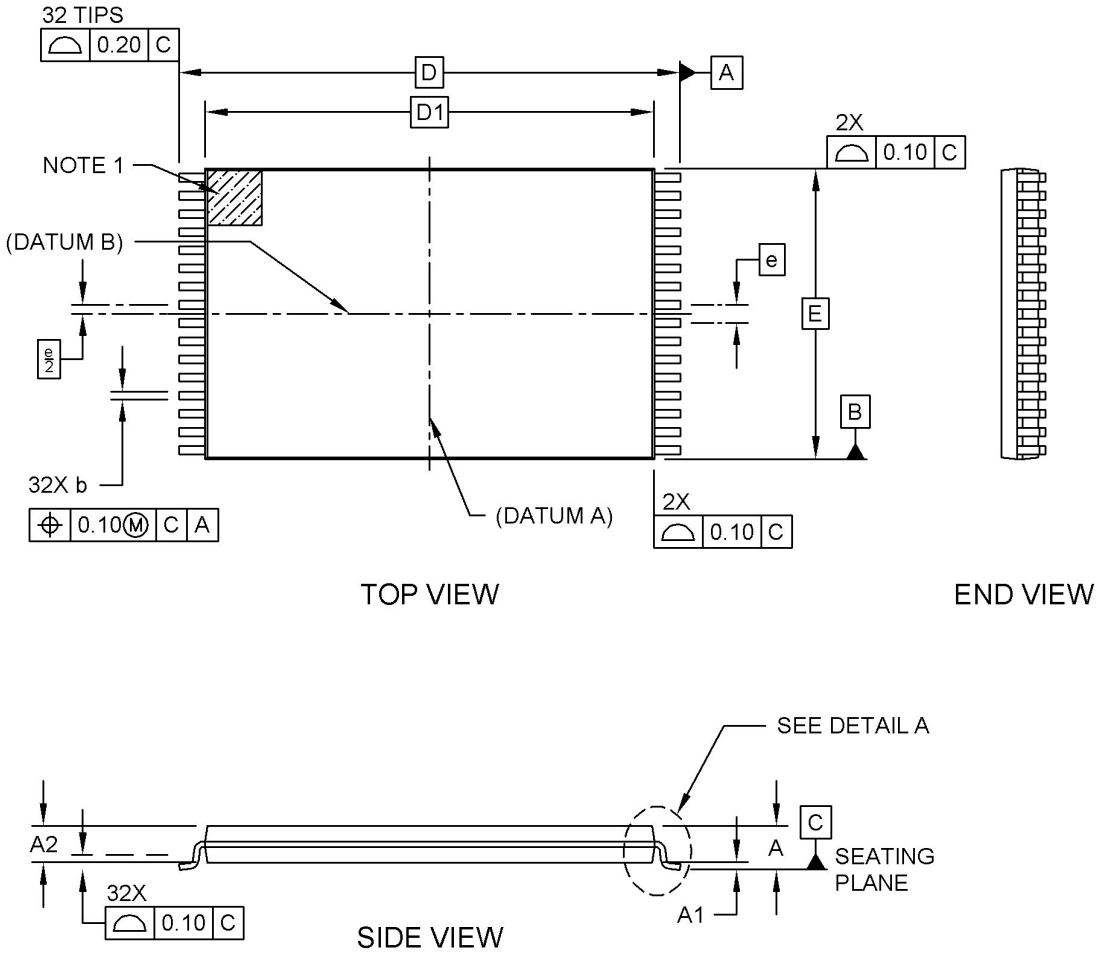
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2023 Rev C

32-Lead Plastic Thin Small Outline Package (6JW) - 8x13.4 mm Body [TSOP]

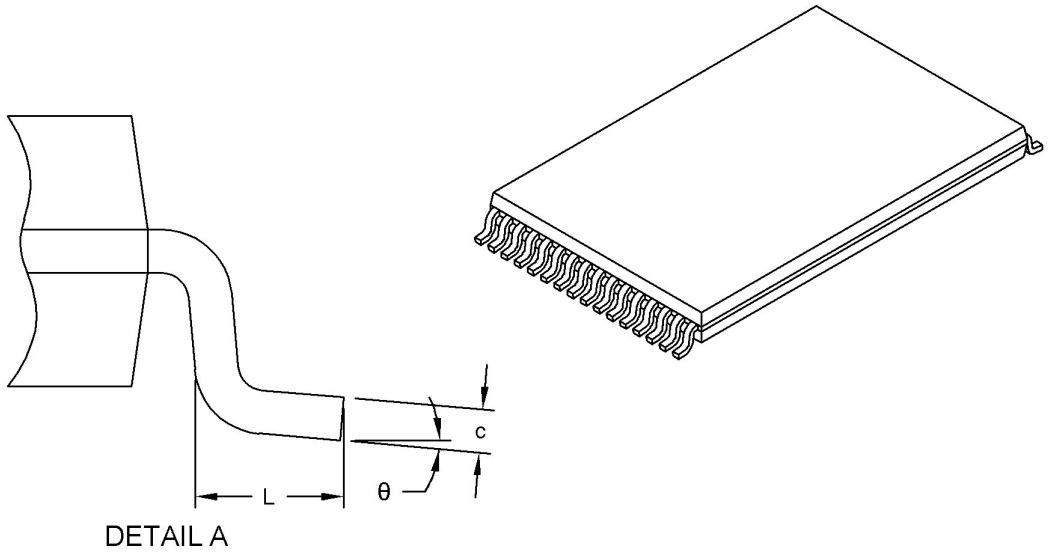
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-628 Rev A Sheet 1 of 2

32-Lead Plastic Thin Small Outline Package (6JW) - 8x13.4 mm Body [TSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		13.40 BSC	
Molded Package Length	D1		11.80 BSC	
Overall Width	E		8.00 BSC	
Terminal Thickness	c	–	-	0.21
Terminal Width	b	0.17	–	0.23
Terminal Length	L	0.30	–	0.70
Foot Angle	θ	0°	–	5°

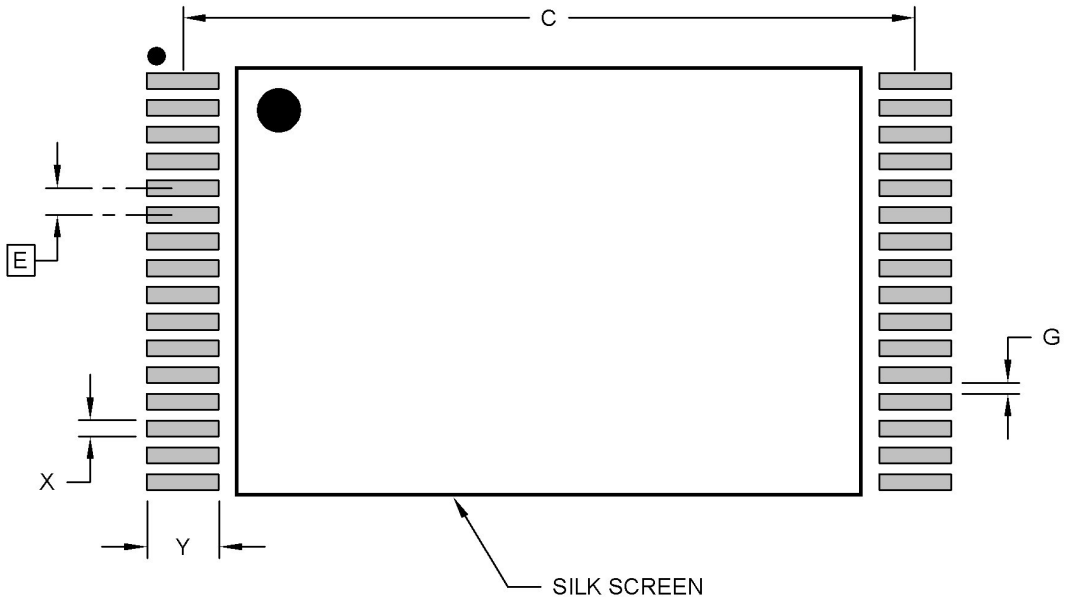
Notes:

1. Pin 1 visual index feature may vary but must be located within the hatched area.
2. Dimensions D1 and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-628 Rev A Sheet 2 of 2

32-Lead Plastic Thin Small Outline Package (6JW) - 8x13.4 mm Body [TSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C		12.90	
Contact Pad Width (X32)	X			0.30
Contact Pad Length (X32)	Y			1.30
Contact Pad to Contact Pad (X30)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2628 Rev A

APPENDIX A: REVISION HISTORY

Revision E (November 2024)

Updated Package Marking section.

Revision D (September 2024)

Replaced WHE package type with TU package type.

Revision C (April 2016)

Corrected typo in “Product Ordering Information” section.

Revision B (April 2013)

End of Life for all 45 ns valid combinations; Updated Table 6 and Table 11.

Revision A (July 2011)

All 45 ns parts reinstated; Applied new document format; Released document under letter revision system; Updated spec number from S71147 to DS25022.

Revision 09 (January 2010)

End of Life for all 45 ns valid combinations. See S71147(02); Added replacement 55 ns valid combinations.

Revision 08 (September 2009)

Changed endurance from 10,000 to 100,000 in “Product Description” section.

Revision 07 (March 2009)

Removed leaded parts from valid combinations. See PSN-D0PB0001.

Revision 06 (August 2004)

Corrected Revision History for Version 04: I_{DD} maximum value was incorrectly stated as 30 mA instead of 35 mA.

Revision 05 (November 2003)

2004 Data Book; Added non-Pb MPNs and removed footnote.

Revision 04 (October 2003)

Document status changed from “Preliminary Specification” to “Data Sheet”; Changed I_{DD} Program and Erase maximum values from 25 to 35 in Table 7 on page 12.

Revision 03 (March 2003)

Changes to Table 7 on page 12; Added footnote for MPF power usage and Typical conditions; Clarified the Test Conditions for Power Supply Current and Read parameters; Clarified I_{DD} Write to be Program and Erase.

Revision 02 (May 2002)

2002 Data Book

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups and a Microchip design partner program member listing
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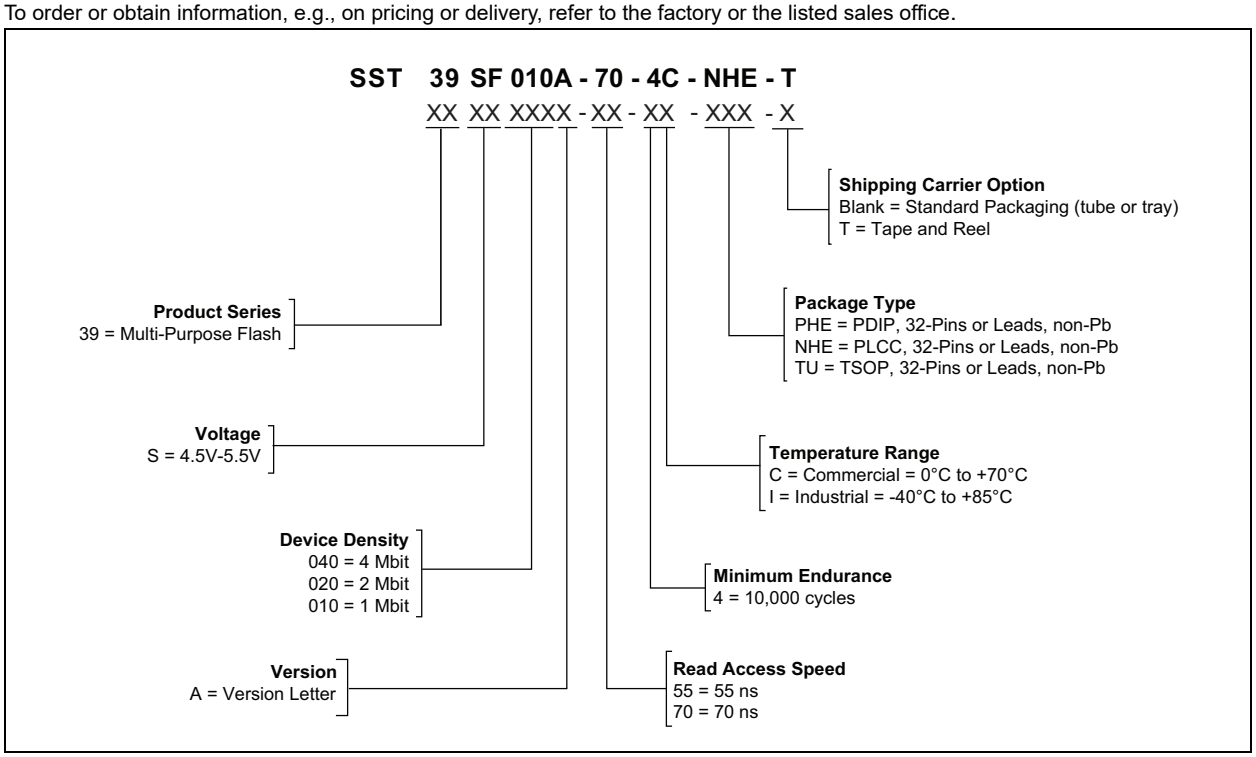
To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Valid Combinations for SST39SF010A[1]		
SST39SF010A–55–4C–NHE	SST39SF010A–55–4C–TU	SST39SF010A–70–4C–PHE
SST39SF010A–70–4C–NHE	SST39SF010A–70–4C–TU	
SST39SF010A–55–4I–NHE	SST39SF010A–55–4I–TU	
SST39SF010A–70–4I–NHE	SST39SF010A–70–4I–TU	
Valid Combinations for SST39SF020A[1]		
SST39SF020A–55–4C–NHE	SST39SF020A–55–4C–TU	SST39SF020A–70–4C–PHE
SST39SF020A–70–4C–NHE	SST39SF020A–70–4C–TU	
SST39SF020A–55–4I–NHE	SST39SF020A–55–4I–TU	
SST39SF020A–70–4I–NHE	SST39SF020A–70–4I–TU	
Valid Combinations for SST39SF040[1]		
SST39SF040–55–4C–NHE	SST39SF040–55–4C–TU	SST39SF040–70–4C–PHE
SST39SF040–70–4C–NHE	SST39SF040–70–4C–TU	
SST39SF040–55–4I–NHE	SST39SF040–55–4I–TU	
SST39SF040–70–4I–NHE	SST39SF040–70–4I–TU	

Note 1: For Tape and Reel, add “-T”.

Note the following details of the code protection feature on Microchip products:

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