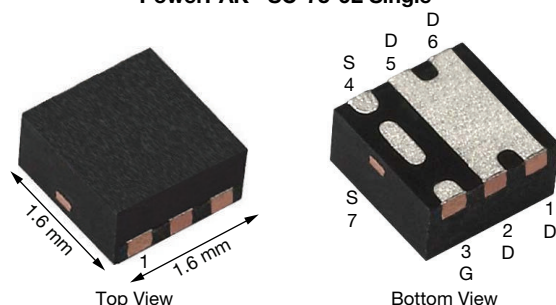


P-Channel 20 V (D-S) MOSFET

PowerPAK® SC-75-6L Single

Marking code: BP

PRODUCT SUMMARY	
V_{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.026
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.034
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.5$ V	0.051
Q_g typ. (nC)	7.0
I_D (A) ^a	-9
Configuration	Single

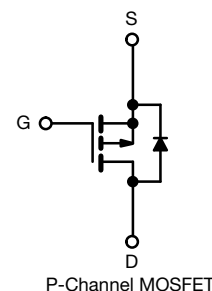
FEATURES

- TrenchFET® Gen V p-channel MOSFET
- Thermally enhanced PowerPAK® SC-75 package
 - Small footprint area
 - Low on-resistance
 - Thin 0.75 mm profile
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Portable devices such as smart phones, tablet PCs, and mobile computing
 - Battery charger switch
 - Buck converter
 - Power management
 - Load switch



P-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SC-75
Lead (Pb)-free and halogen-free	SiB5215DK-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	-20	V	
Gate-source voltage	V_{GS}	± 12		
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	-9 ^a	A	
	$T_C = 70$ °C	-9 ^a		
	$T_A = 25$ °C	-7.9 ^{b, c}		
	$T_A = 70$ °C	-6.3 ^{b, c}		
Pulsed drain current ($V_{GS} = -10$ V, $t = 100$ μ s)	I_{DM}	-35		
Continuous source-drain diode current (MOSFET diode conduction)	$T_C = 25$ °C	-9 ^a		
	$T_A = 25$ °C	-2.2 ^{b, c}		
Maximum power dissipation	$T_C = 25$ °C	13	W	
	$T_C = 70$ °C	8.4		
	$T_A = 25$ °C	2.45 ^{b, c}		
	$T_A = 70$ °C	1.6 ^{b, c}		
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^{d, e}		260		

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

**THERMAL RESISTANCE RATINGS**

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, b}	$t \leq 5$ s	R_{thJA}	41	51	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	7.5	9.5	

Notes

a. Surface mounted on 1" x 1" FR4 board

b. Maximum under steady state conditions is 105 °C/W

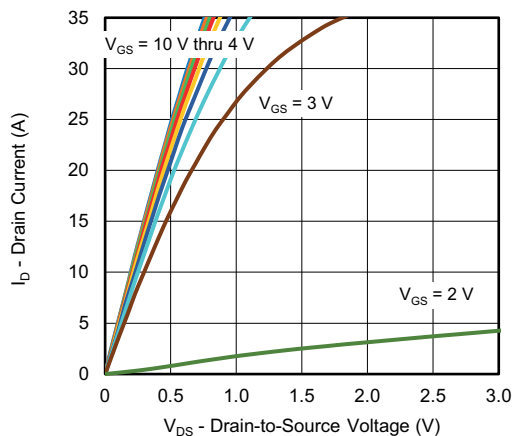
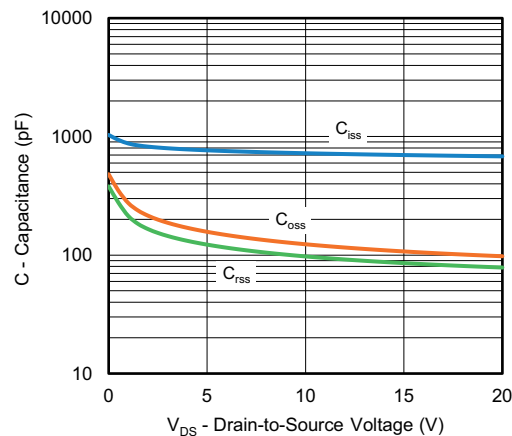
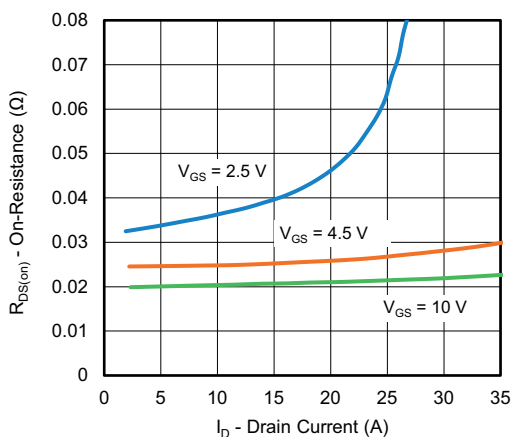
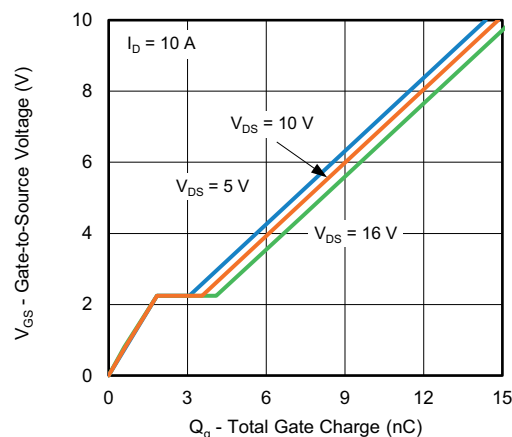
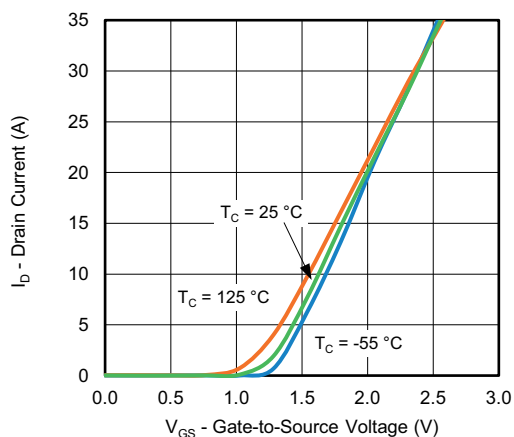
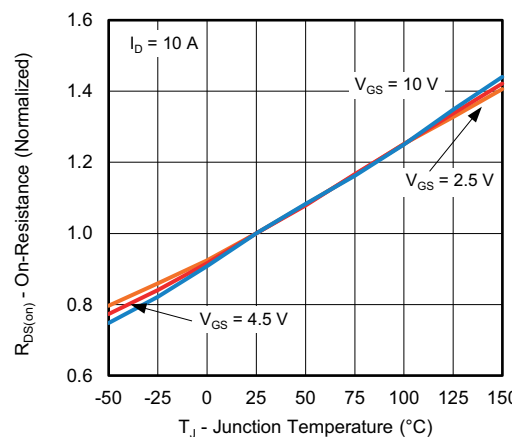
SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-20	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -10 mA	-	-14.2	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = -250 μA	-	3.2	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.6	-	-1.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -5 A	-	0.020	0.026	Ω
		V _{GS} = -4.5 V, I _D = -3 A	-	0.024	0.034	
		V _{GS} = -2.5 V, I _D = -2 A	-	0.034	0.051	
Forward transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -15 A	-	27	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	-	730	-	pF
Output capacitance	C _{oss}		-	125	-	
Reverse transfer capacitance	C _{rss}		-	100	-	
Total gate charge	Q _g	V _{DS} = -10 V, V _{GS} = -10 V, I _D = -10 A	-	15	23	nC
Gate-source charge	Q _{gs}	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -10 A	-	7.0	11	
Gate-drain charge	Q _{gd}		-	1.8	-	
Gate resistance	R _g		f = 1 MHz	1.3	6.5	
Turn-on delay time	t _{d(on)}	V _{DD} = -10 V, R _L = 1 Ω I _D ≅ -10 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	12	25	ns
Rise time	t _r		-	32	65	
Turn-off delay time	t _{d(off)}		-	22	45	
Fall time	t _f		-	10	20	
Turn-on delay time	t _{d(on)}	V _{DD} = -10 V, R _L = 1 Ω I _D ≅ -10 A, V _{GEN} = -10 V, R _g = 1 Ω	-	7	15	
Rise time	t _r		-	5	10	
Turn-off delay time	t _{d(off)}		-	19	40	
Fall time	t _f		-	7	15	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-9	A
Pulse diode forward current	I _{SM}		-	-	-35	
Body diode voltage	V _{SD}	I _S = -10 A, V _{GS} = 0 V	-	-0.81	-1.1	V
Body diode reverse recovery time	t _{rr}	I _F = -10 A, di/dt = 100 A/μs, T _J = 25 °C	-	8	20	ns
Body diode reverse recovery charge	Q _{rr}		-	2.5	5	nC
Reverse recovery fall time	t _a		-	5	-	ns
Reverse recovery rise time	t _b		-	3	-	

Notesa. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %

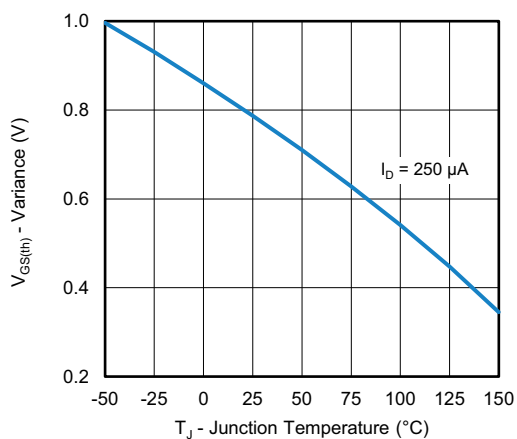
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

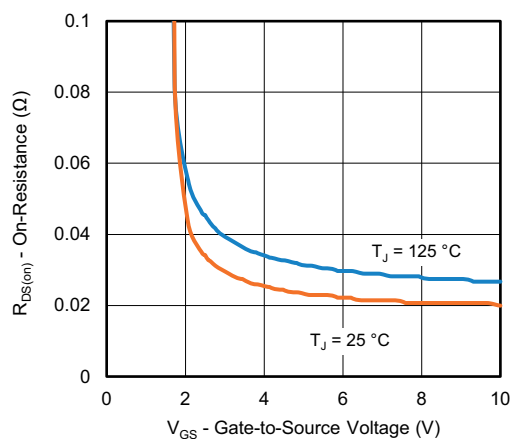
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Gate-Source Voltage vs. Gate Current

Capacitance

On-Resistance vs. Drain Current and Gate Voltage

Gate Charge

Transfer Characteristics

On-Resistance vs. Junction Temperature



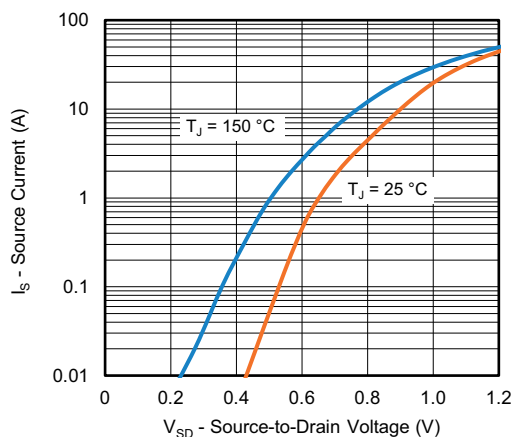
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



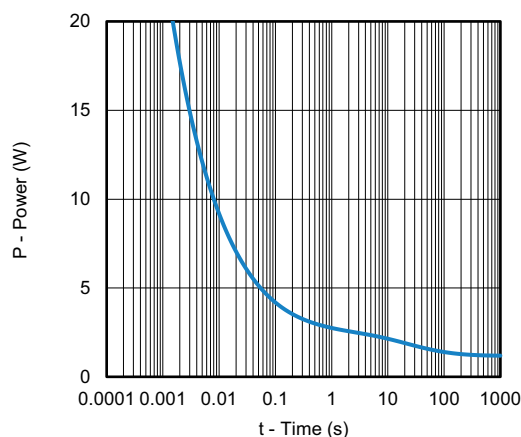
Threshold Voltage



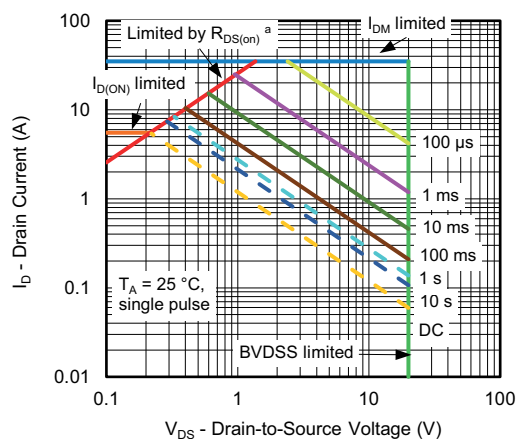
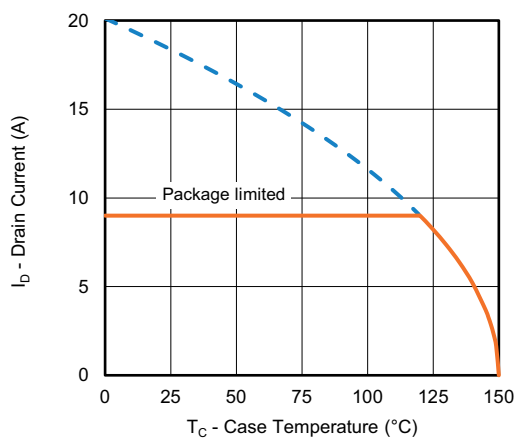
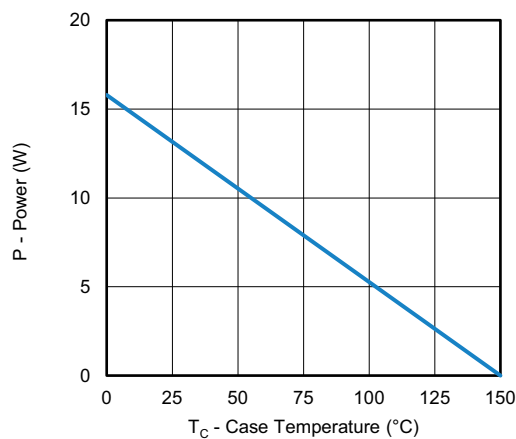
On-Resistance vs. Gate-to-Source Voltage



Source-Drain Diode Forward Voltage



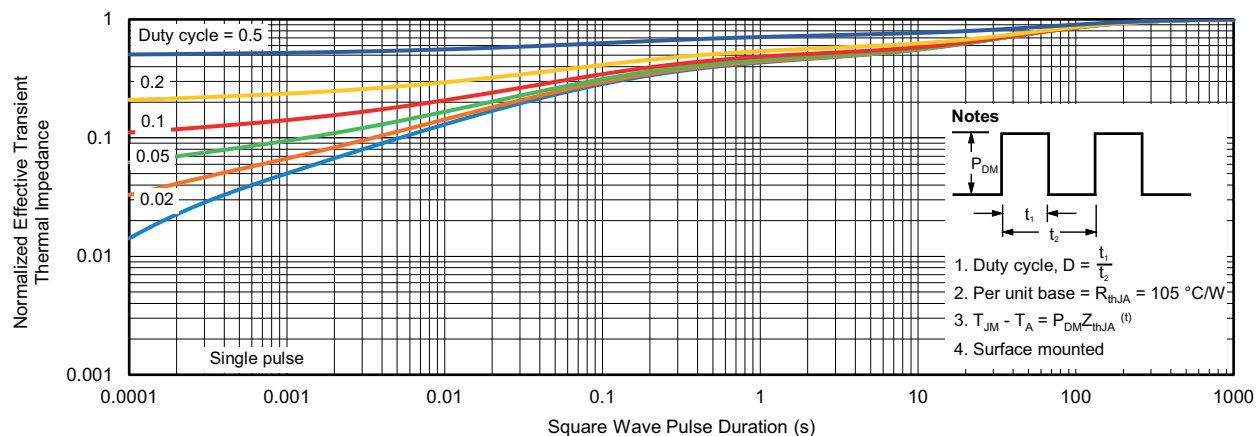
Single Pulse Power, Junction-to-Ambient

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Safe Operating Area, Junction-to-Case

Current Derating ^a

Power Derating
Note

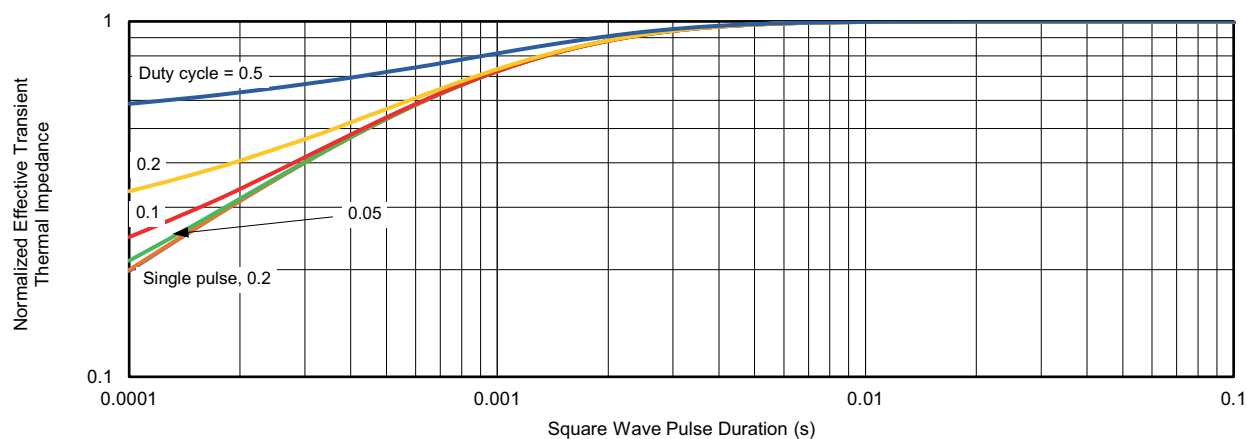
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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