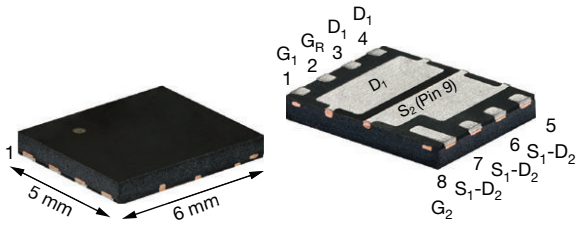
Symmetric Dual N-Channel 40 V (D-S) MOSFET

PowerPAIR® 6 x 5FSW



Top View Bottom View

FEATURES

- TrenchFET® Gen IV power MOSFET
- 100 % R_g and UIS tested
- Integrated half-bridge MOSFET power stage
- Wettable flank terminals
- Internally connected switch node
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

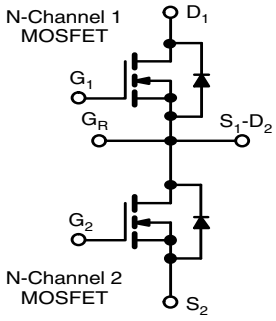
AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Buck-boost
- Half-bridge synchronous rectification
- Synchronous buck
- Motor drive control



PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.0015
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.0024
I_D (A) [e]	162
Configuration	Dual

ORDERING INFORMATION	
Package	PowerPAIR 6 x 5FSW
Lead (Pb)-free and halogen-free	SQZF140ELPW-T1_GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current [e]	T_C = 25 °C	I_D	162	A
	T_C = 125 °C		93	
Pulsed drain current [e]		I_{DM}	543	
Continuous source-drain diode current [e]	T_C = 25 °C	I_S	68	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	37	
Single pulse avalanche energy		E_{AS}	68	mJ
Maximum power dissipation [a, e]	T_C = 25 °C	P_D	75	W
	T_C = 125 °C		25	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [b]	R_{thJA}	30	°C/W
Junction-to-case (exposed pad) [d]		R_{thJC}	2.0	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. When mounted on 1" square PCB (FR4 material)

c. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

d. As per JESD51-14

e. Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.2	1.7	2.2	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 40 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	-	-	100	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	-	-	500	
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V	I_D = 15 A	-	0.00185	0.00240	Ω
		V_{GS} = 10 V	I_D = 15 A	-	0.00125	0.0015	
		V_{GS} = 10 V	I_D = 15 A, T_J = 125 °C	-	-	0.0024	
		V_{GS} = 10 V	I_D = 15 A, T_J = 175 °C	-	-	0.0030	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 70 A		-	200	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	-	5042	7059	pF
Output capacitance	C_{oss}			-	1096	1535	
Reverse transfer capacitance	C_{rss}			-	32	45	
Total gate charge	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 15 A	-	72	-	nC
Gate-source charge	Q_{gs}			-	15	-	
Gate-drain charge	Q_{gd}			-	12	-	
Gate resistance	R_g	f = 1 MHz		0.3	0.9	2.4	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 1.33 Ω $I_D \cong$ 15 A, V_{GEN} = 10 V, R_g = 1 Ω		-	17	26	ns
Rise time	t_r			-	53	80	
Turn-off delay time	$t_{d(off)}$			-	40	60	
Fall time	t_f			-	8	12	
Source-Drain Diode Ratings and Characteristics [b]							
Body diode reverse recovery time	t_{rr}	I_F = 15 A, di/dt = 100 A/µs, T_J = 25 °C		-	42	84	ns
Body diode reverse recovery charge	Q_{rr}			-	38	76	nC
Reverse recovery fall time	t_a			-	22		A
Reverse recovery rise time	t_b			-	22		A
Pulsed current	I_{SM}			-	-	300	A
Forward voltage	V_{SD}	I_S = 10 A, V_{GS} = 0 V		-	0.75	1.1	V

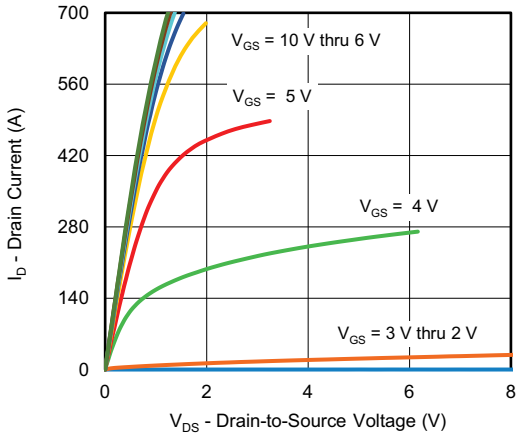
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

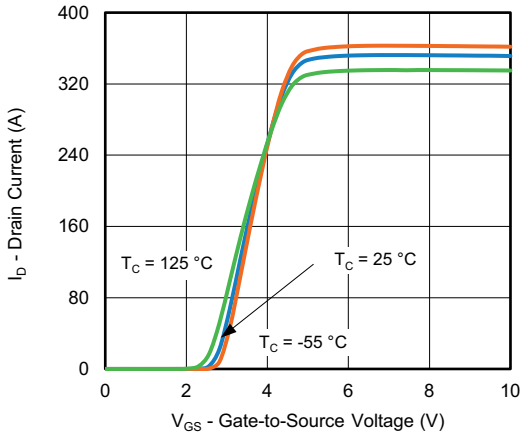
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

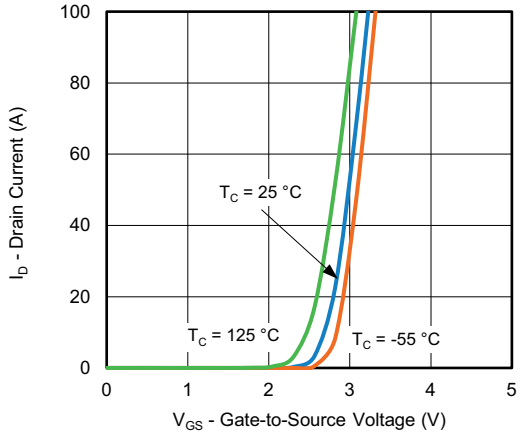
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



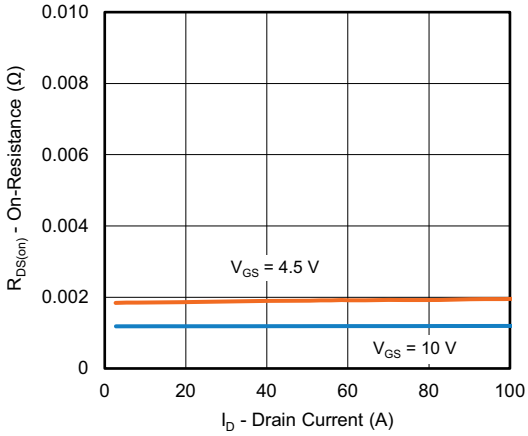
Output Characteristics



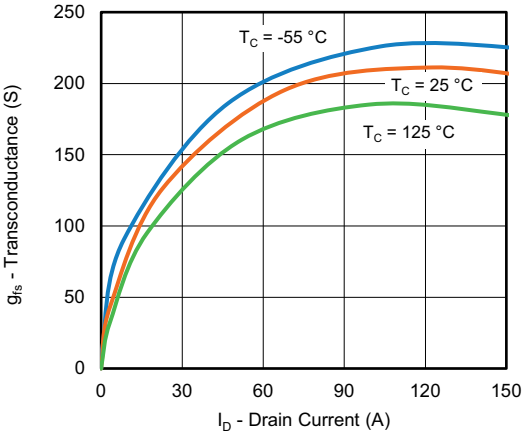
Transfer Characteristics



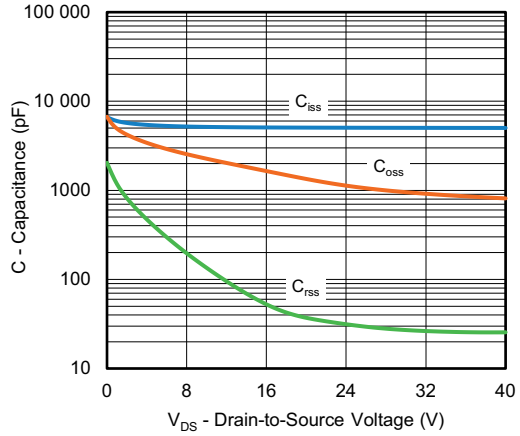
Transfer Characteristics



On-Resistance vs. Drain Current

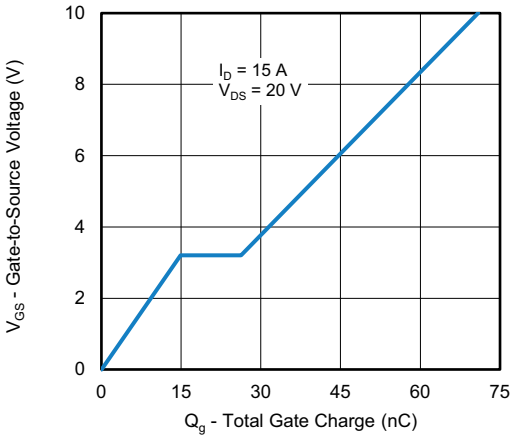


Transconductance

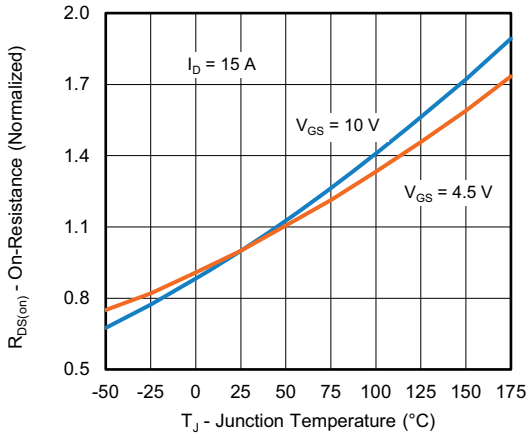


Capacitance

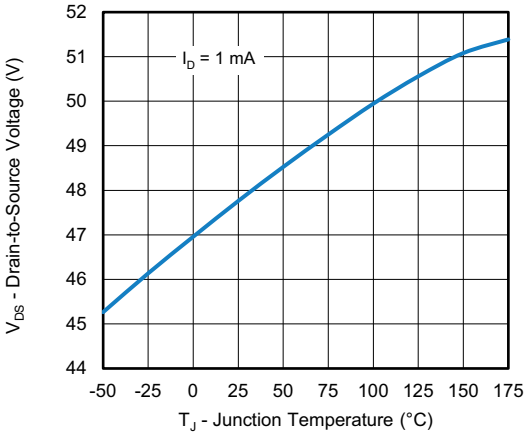
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



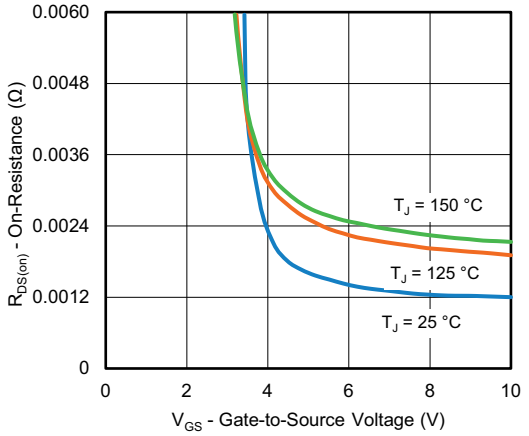
Gate Charge



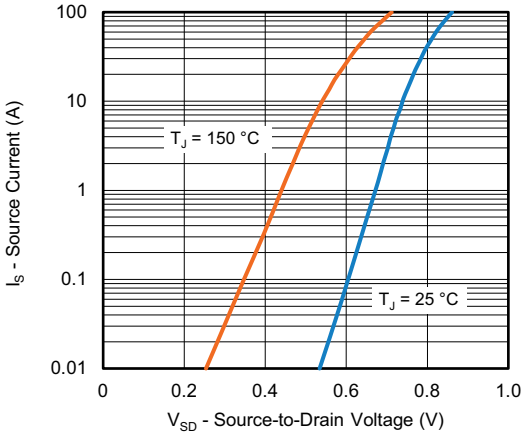
On-Resistance vs. Junction Temperature



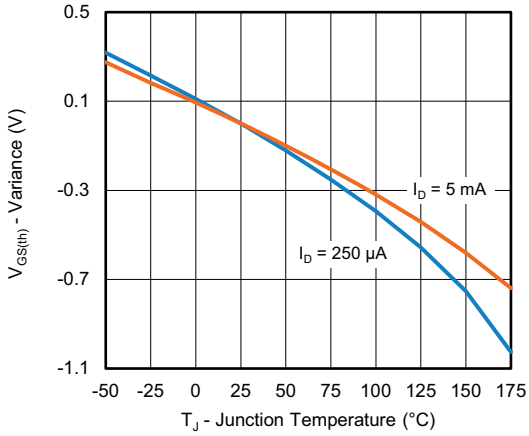
Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



Source-Drain Diode Forward Voltage

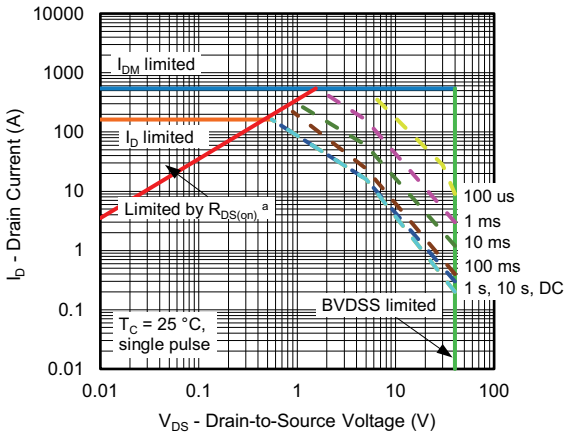


Threshold Voltage

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area

Note

b. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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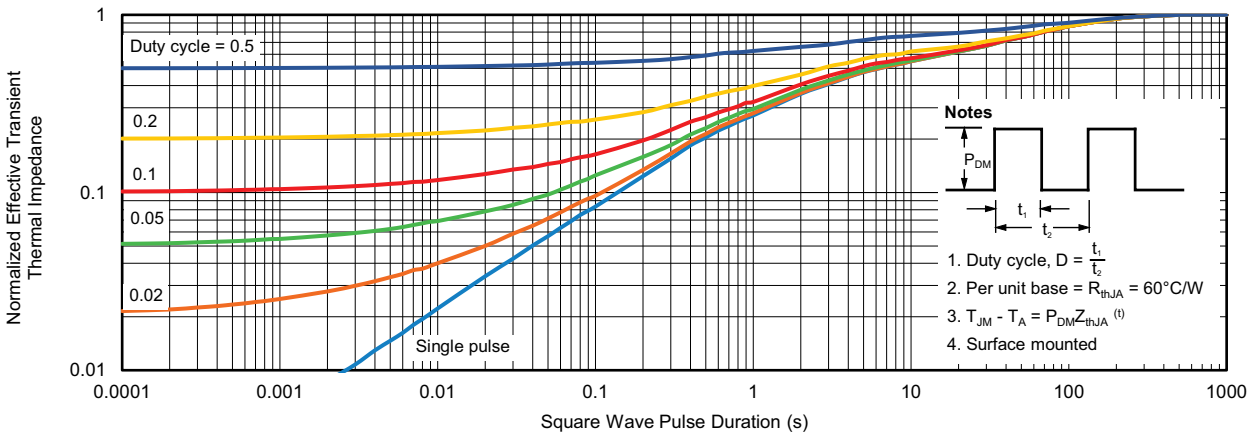
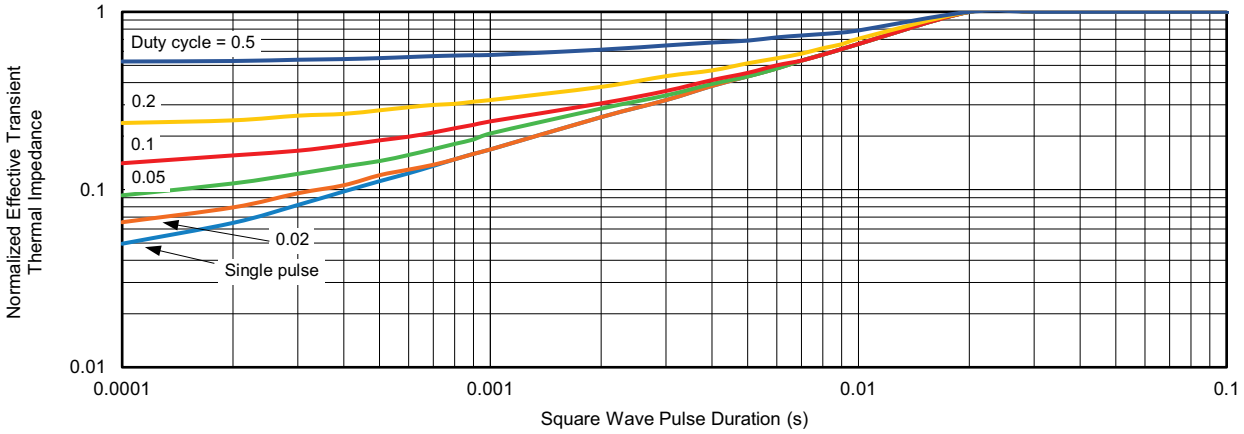


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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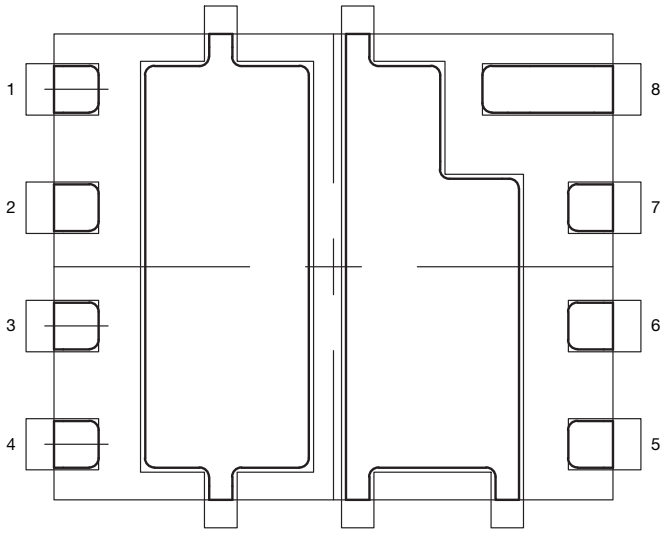
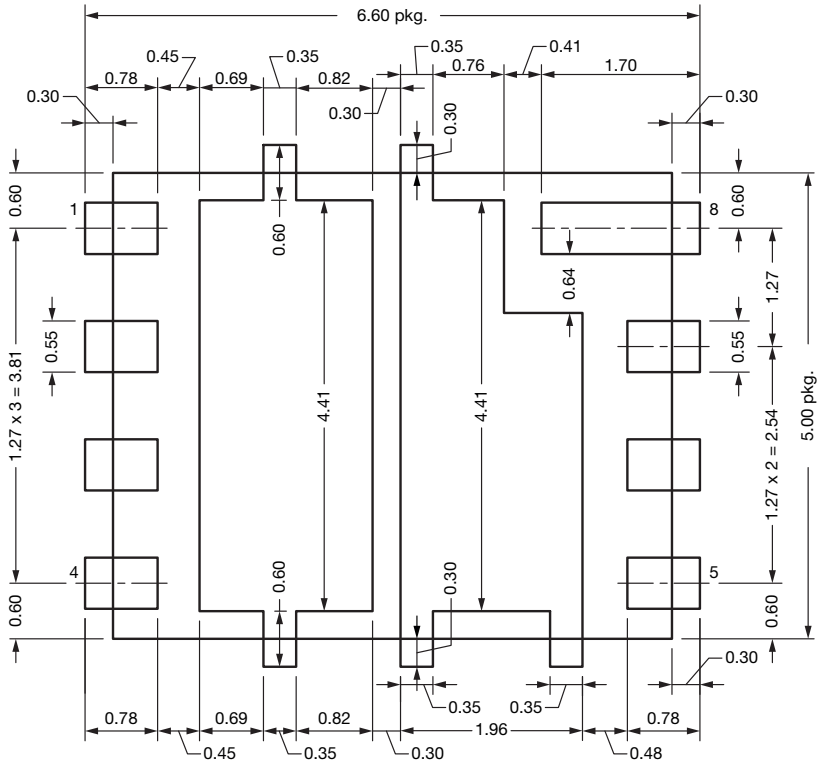
Recommended Land Pattern PowerPAIR® 6 x 5 FS and PowerPAIR® 6 x 5 FSW





Note

- Dimensions in mm

T24-0311-Rev. A, 09-Sep-2024 DWG: 3030

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