# Low $I_Q$, Dual, 2-Phase Synchronous Boost Controller for GaN FETs

## FEATURES

- GaN Drive Technology fully Optimized for GaN FETs
- Output Voltage up to 100V
- Wide $V_{IN}$ Range: 4V to 60V and Operates Down to 1V After Start-Up
- No Catch, Clamp, or Bootstrap Diodes Needed
- Internal Smart Bootstrap Switches Prevent Overcharging of High-Side Driver Supplies
- Resistor Adjustable Dead Times
- Split Output Gate Drivers for Adjustable Turn-On and Turn-Off Driver Strengths
- Accurate Adjustable Driver Voltage and UVLO
- Low Operating $I_Q$: 15µA
- Programmable Frequency (100kHz to 3MHz)
- Synchronizable Frequency (100kHz to 3MHz)
- Spread Spectrum Frequency Modulation
- 40-Lead (6mm × 6mm), Side Wettable, QFN Package
- AEC-Q100 Qualified for Automotive Applications

## APPLICATIONS

- Automotive and Industrial Power Systems
- Military Avionics and Medical Systems
- Telecommunications Power Systems

## GENERAL DESCRIPTION

The **LTC®7892** is a high-performance dual boost DC-to-DC switching regulator controller that drives all N-channel synchronous gallium nitride (GaN) field effect transistor (FET) power stages with output voltages up to 100V. The LTC7892 solves many of the challenges traditionally faced when using GaN FETs. The LTC7892 simplifies the application design while requiring no protection diodes and no other additional external components compared to a silicon metal-oxide-semiconductor field effect transistor (MOSFET) solution.

The Internal smart bootstrap switches prevent overcharging of the BOOSTx pin to the SWx pin the high-side driver supplies during dead times, protecting the gate of the top GaN FET. The dead times of the LTC7892 can optionally be optimized with external resistors for margin or to tailor the application for higher efficiency and allowing for high-frequency operation.

The gate drive voltage of the LTC7892 can be precisely adjusted from 4V to 5.5V to optimize performance and allow the use of different GaN FETs or even logic-level MOSFETs. When biased from the boost converter regulator output, the LTC7892 can operate from an input supply as low as 1V after start-up.

## TYPICAL APPLICATION

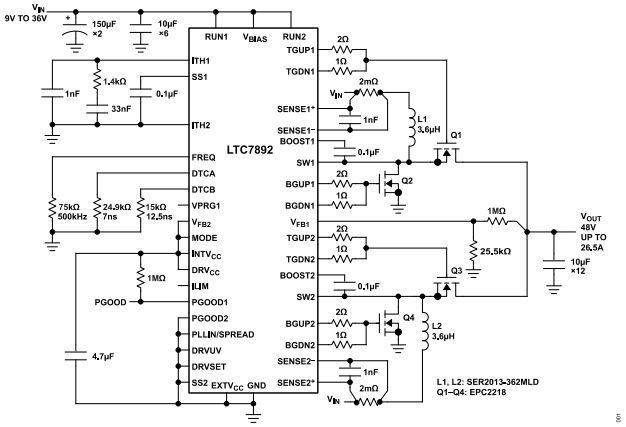


*Figure 1. High Power, 48V Output Boost Converter*

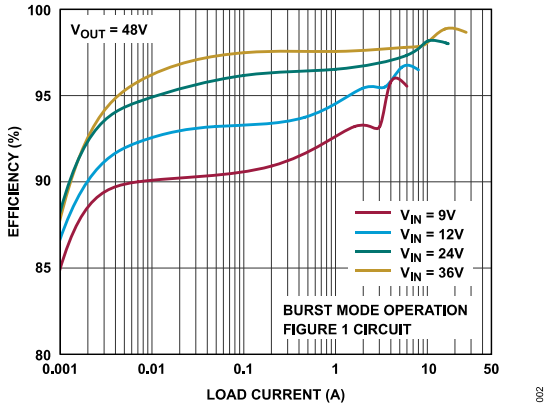


*Figure 2. Efficiency and Power Loss*


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## REVISION HISTORY

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 12/24 | Initial release | — |

# SPECIFICATIONS

**Table 1. Electrical Characteristics**

(Specifications are at $T_J$ = -40°C to +125°C for the minimum and maximum values, $T_A$ = 25°C for the typical values, $V_{BIAS}$ = 12V, RUN1 and RUN2 = 5V, VPRG1 = Float, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, DTCA and DTCB = 0V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Input Supply** | | | | | | |
| Bias Input Supply Operating Range | $V_{BIAS}$ | | 4 | | 100 | V |
| Boost Converter Input Supply Operating Range | $V_{IN}$ | $V_{BIAS} \geq 4V$ | 1 | | 60 | V |
| Output Voltage Operating Range | $V_{OUT1,OUT2}$ | | 1.2 | | 100 | V |
| **Controller Operation** | | | | | | |
| Channel 1 Regulated Feedback Voltage | $V_{FB1}$ | $V_{BIAS}$ = 4V to 100V,<br>ITH1 Voltage = 0.6V to 1.2V<br>VPRG1 = floating, $T_A$ = 25°C<br>VPRG1 = floating<br>VPRG1 = 0V<br>VPRG1 = $INTV_{CC}$ | <br><br>1.188<br>1.182<br>23.45<br>27.38 | <br><br>1.2<br>1.2<br>24<br>28 | <br><br>1.212<br>1.218<br>24.55<br>28.62 | <br><br>V<br>V<br>V<br>V |
| Channel 2 Regulated Feedback Voltage[1] | $V_{FB2}$ | $V_{BIAS}$ = 4V to 100V,<br>ITH2 Voltage = 0.6V to 1.2V<br>$T_A$ = 25°C | <br>1.188<br>1.182 | <br>1.2<br>1.2 | <br>1.212<br>1.218 | <br>V<br>V |
| Channel 1 Feedback Current[1] | | VPRG1 = floating, $T_A$ = 25°C<br>VPRG1 = 0V or $INTV_{CC}$ | -50 | 0<br>2 | +50 | nA<br>µA |
| Channel 2 Feedback Current[1] | | $T_A$ = 25°C | -50 | 0 | +50 | nA |
| Feedback Overvoltage Threshold | | Relative to $V_{FBx}$, $T_A$ = 25°C | 7 | 10 | 13 | % |
| Transconductance Amplifier[1] | $g_{m1}$, $g_{m2}$ | ITH1 and ITH2 = 1.2V,<br>Sink and Source = 5µA | | 1.8 | | mmho |
| Maximum Current Sense Threshold | $V_{SENSE(MAX)}$ | $V_{FBx}$ = 1.1V, $SENSEx^+$ = 12V<br>ILIM = 0V<br>ILIM = floating<br>ILIM = $INTV_{CC}$ | <br>21<br>45<br>67 | <br>25<br>50<br>75 | <br>31<br>55<br>83 | <br>mV<br>mV<br>mV |

(Specifications are at $T_J$ = -40°C to +125°C for the minimum and maximum values, $T_A$ = 25°C for the typical values, $V_{BIAS}$ = 12V, RUN1 and RUN2 = 5V, VPRG1 = Float, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, DTCA and DTCB = 0V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Current Sense Threshold Matching between Channels | | $V_{FBx}$ = 1.1V, $SENSEx^+$ = 12V, ILIM = floating, $T_A$ = 25°C | -3.5 | 0 | 3.5 | mV |
| $SENSE1^-$ and $SENSE2^-$ Pin Current | $I_{SENSE1^-}$, $I_{SENSE2^-}$ | $SENSE1^-$ and $SENSE2^-$ = 12V, $T_A$ = 25°C | -1 | | +1 | µA |
| $SENSE1^+$ Pin Current | $I_{SENSE1^+}$ | $SENSE1^+$ < 3V<br>3.3V ≤ $SENSE1^+$ < $INTV_{CC}$ – 0.5V<br>$SENSE1^+$ > $INTV_{CC}$ + 0.5V | | 1<br>75<br>725 | | µA<br>µA<br>µA |
| $SENSE2^+$ Pin Current | $I_{SENSE2^+}$ | $SENSE2^+$ < $INTV_{CC}$ – 0.5V, $T_A$ = 25°C<br>$SENSE2^+$ > $INTV_{CC}$ + 0.5V | -2 | <br>650 | +2 | µA<br>µA |
| Soft-Start Charge Current | | SS1 and SS2 = 0V | 9.5 | 12 | 14.5 | µA |
| RUN Pin ON Threshold | | RUNx rising | 1.15 | 1.20 | 1.25 | V |
| RUN Pin Hysteresis | | | | 120 | | mV |
| **DC Supply Current** | | | | | | |
| $V_{BIAS}$ Shutdown Current | | RUN1 and RUN2 = 0V | | 1 | | µA |
| $V_{BIAS}$ Sleep Mode Current | | $SENSE1^+$ < 3.2V, $EXTV_{CC}$ = 0V<br>One Channel On<br>Both Channels On | | <br>15<br>19 | | <br>µA<br>µA |
| Sleep Mode Current[2], Only Channel 1 On<br>$V_{BIAS}$ Current<br>$V_{BIAS}$ Current<br>$EXTV_{CC}$ Current<br>$SENSE1^+$ Current | | <br>$SENSE1^+$ ≥ 3.2V, $EXTV_{CC}$ = 0V<br>$SENSE1^+$ ≥ 3.2V, $EXTV_{CC}$ ≥ 4.8V<br>$SENSE1^+$ ≥ 3.2V, $EXTV_{CC}$ ≥ 4.8V<br>$SENSE1^+$ ≥ 3.2V | | <br>5<br>1<br>6<br>10 | | <br>µA<br>µA<br>µA<br>µA |
| Sleep Mode Current[2] Both Channels On<br>$V_{BIAS}$ Current<br>$EXTV_{CC}$ Current<br>$SENSE1^+$ Current | | $SENSE1^+$ ≥ 3.2V, $EXTV_{CC}$ ≥ 4.8V | | <br>1<br>7<br>12 | | <br>µA<br>µA<br>µA |

(Specifications are at $T_J$ = -40°C to +125°C for the minimum and maximum values, $T_A$ = 25°C for the typical values, $V_{BIAS}$ = 12V, RUN1 and RUN2 = 5V, VPRG1 = Float, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, DTCA and DTCB = 0V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Pulse-Skipping (PS) Mode or Forced Continuous Mode (FCM), $V_{BIAS}$ or $EXTV_{CC}$ Current[2] | | One Channel On<br>Both Channels On | | 2<br>3 | | mA<br>mA |
| **Gate Drivers** | | | | | | |
| TGxxx or BGxxx On Resistance | | DRVSET = $INTV_{CC}$<br>Pull-Up<br>Pull-Down | | <br>1.0<br>1.0 | | <br>Ω<br>Ω |
| BOOSTx to $DRV_{CC}$ Switch on Resistance | | DRVSET = $INTV_{CC}$ | | 6 | | Ω |
| TGxxx or BGxxx Transition Time[3] | | Rise Time<br>Fall Time | | 25<br>15 | | ns<br>ns |
| BGxxx Off to TGxxx on Adaptive Delay Time[4] | | DTCA = 0V | | 15 | | ns |
| TGxxx Off to BGxxx on Adaptive Delay Time[4] | | DTCB = 0V | | 15 | | ns |
| BGxxx Off to TGxxx on Open-Loop Delay[4] | | DTCA = 10kΩ<br>DTCA = 50kΩ<br>DTCA = 100kΩ | | 7<br>25<br>40 | | ns<br>ns<br>ns |
| TGxxx Off to BGxxx on Open-Loop Delay[4] | | DTCB = 10kΩ<br>DTCB = 50kΩ<br>DTCB = 100kΩ | | 7<br>25<br>40 | | ns<br>ns<br>ns |
| BGxxx Minimum On-Time[5] | $t_{ON(MIN)}$ | | | 100 | | ns |
| Maximum Duty Factor for BGxxx | | $V_{FREQ}$ = 0V | | 93 | | % |
| **$INTV_{CC}$ Low Dropout (LDO) Linear Regulators** | | | | | | |
| $INTV_{CC}$ Voltage for $V_{BIAS}$ and $EXTV_{CC}$ LDOs | | $EXTV_{CC}$ = 0V for $V_{BIAS}$ LDO,<br>$EXTV_{CC}$ = 12V for $EXTV_{CC}$ LDO | | | | |

(Specifications are at $T_J$ = -40°C to +125°C for the minimum and maximum values, $T_A$ = 25°C for the typical values, $V_{BIAS}$ = 12V, RUN1 and RUN2 = 5V, VPRG1 = Float, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, DTCA and DTCB = 0V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| | | DRVSET = $INTV_{CC}$ | 5.2 | 5.5 | 5.7 | V |
| | | DRVSET = 0V | 4.8 | 5.0 | 5.2 | V |
| | | DRVSET = 64.9kΩ | 4.5 | 4.75 | 5.0 | V |
| $DRV_{CC}$ Load Regulation | | $DRV_{CC}$ load current = 0mA to 100mA, $T_A$ = 25°C | | 1 | 3 | % |
| Undervoltage Lockout | UVLO | $DRV_{CC}$ Rising | | | | |
| | | DRVUV = $INTV_{CC}$ | 4.8 | 5.0 | 5.2 | V |
| | | DRVUV = 0V | 3.6 | 3.8 | 4.0 | V |
| | | DRVUV = floating | 4.2 | 4.4 | 4.6 | V |
| | | $DRV_{CC}$ Falling | | | | |
| | | DRVUV = $INTV_{CC}$ | 4.55 | 4.75 | 4.95 | V |
| | | DRVUV = 0V | 3.4 | 3.6 | 3.8 | V |
| | | DRVUV = floating | 4.0 | 4.18 | 4.4 | V |
| $EXTV_{CC}$ LDO Switchover Voltage $EXTV_{CC}$ Rising | | DRVUV = $INTV_{CC}$ or floating, $T_A$ = 25°C | 5.75 | 5.95 | 6.15 | V |
| | | DRVUV = 0V, $T_A$ = 25°c | 4.6 | 4.76 | 4.9 | V |
| $EXTV_{CC}$ LDO Switchover Hysteresis $EXTV_{CC}$ Falling | | DRVUV = $INTV_{CC}$ or floating | | 390 | | mV |
| | | DRVUV = 0V | | 220 | | mV |
| **Spread Spectrum Oscillator and Phase-Locked Loop (PLL)** | | | | | | |
| Fixed Frequencies | $f_{OSC}$ | PLLIN/SPREAD = 0V | | | | |
| | | FREQ = 0V, $T_A$ = 25°C | 320 | 370 | 420 | kHz |
| | | FREQ = $INTV_{CC}$ | 2.0 | 2.25 | 2.5 | MHz |
| | | FREQ = 374kΩ | | 100 | | kHz |
| | | FREQ = 75kΩ, $T_A$ = 25°C | 450 | 500 | 550 | kHz |
| | | FREQ = 12.4kΩ | | 3 | | MHz |
| Synchronizable Frequency Range | $f_{SYNC}$ | PLLIN/SPREAD = External Clock | 0.1 | | 3 | MHz |
| PLLIN Input High-Level | | | 2.2 | | | V |
| PLLIN Input Low-Level | | | | | 0.5 | V |
| Spread Spectrum Frequency Range (Relative to $f_{OSC}$) | | PLLIN/SPREAD = $INTV_{CC}$ | | | | |
| | | Minimum Frequency | | 0 | | % |
| | | Maximum Frequency | | 20 | | % |

(Specifications are at $T_J$ = -40°C to +125°C for the minimum and maximum values, $T_A$ = 25°C for the typical values, $V_{BIAS}$ = 12V, RUN1 and RUN2 = 5V, VPRG1 = Float, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, DTCA and DTCB = 0V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PGOODx Outputs** | | | | | | |
| PGOODx Voltage Low | | PGOODx = 2mA, $T_A$ = 25°C | | 0.2 | 0.4 | V |
| PGOODx Leakage Current | | PGOODx = 5V, $T_A$ = 25°C | -1 | 0 | +1 | µA |
| PGOODx Trip Level ($V_{FBx}$ with respect to Set Regulated Voltage) | | $T_A$ = 25°C<br>$V_{FBx}$ Rising<br>Hysteresis<br>$V_{FBx}$ Falling<br>Hysteresis | <br>7<br><br>-13<br> | <br>10<br>1.6<br>-10<br>1.6 | <br>13<br><br>-7<br> | <br>%<br>%<br>%<br>% |
| PGOODx Delay for Reporting a Fault | | | | 25 | | µs |

1 The LTC7892 is tested in a feedback loop that servos ITHx voltage ($V_{ITHx}$) to a specified voltage and measures the resultant feedback voltage ($V_{FBx}$).

2 SENSE1+ bias current is reflected in the bias supply by the formula $I_{VBIAS} = I_{SENSE1^+} \times V_{BIAS}/(V_{OUT1} \times \eta)$, where η is the efficiency.

3 Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels unless otherwise noted.

4 TGxxx falling to BGxxx rising and BGxxx falling to TGxxx rising delay times are measured at the rising and falling thresholds on TGxxx and BGxxx of approximately 1V. See *Figure 40* and *Figure 41* for more details.

5 The minimum on-time condition specified for inductor peak-to-peak ripple current is >40% of the maximum load current ($I_{MAX}$). See the *Minimum On-Time Considerations* for more details.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C unless otherwise specified.

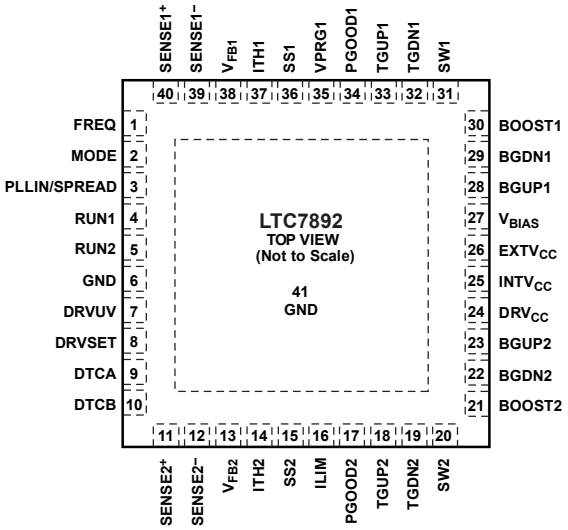
**Table 2. Absolute Maximum Ratings**

| PARAMETER | RATING |
|---|---|
| Bias Input Supply ($V_{BIAS}$) | –0.3V to 100V |
| RUN1 and RUN2 | –0.3V to 100V |
| BOOST1 and BOOST2 | –0.3V to 106V |
| SW1 and SW2 | –5V to 100V |
| BOOST1 to SW1 and BOOST2 to SW2 | –0.3V to 6V |
| TGUP1, TGUP2, TGDN1, TGDN2[1] | Not applicable |
| BGUP1, BGUP2, BGDN1, BGDN2[1] | Not applicable |
| $EXTV_{CC}$ | –0.3V to 30V |
| $DRV_{CC}$ and $INTV_{CC}$ | –0.3V to 6V |
| $V_{FB1}$ | –0.3V to 65V |
| PLLIN/SPREAD FREQ and $V_{FB2}$ | –0.3V to 6V |
| SS1, SS2, ITH1, and ITH2 | –0.3V to 6V |
| DRVSET and DRVUV | –0.3V to 6V |
| MODE, ILIM, and VPRG1 | –0.3V to 6V |
| PGOOD1 and PGOOD2 | –0.3V to 6V |
| DTCA and DTCB | -0.3V to 6V |
| $SENSE1^+$, $SENSE2^+$, $SENSE1^-$, and $SENSE2^-$ | –0.3V to 65V |
| $SENSE1^+$ to $SENSE1^-$ and $SENSE2^+$ to $SENSE2^-$ Continuous | –0.3V to +0.3V |
| $SENSE1^+$ to $SENSE1^-$ and $SENSE2^+$ to $SENSE2^-$ < 1ms | -100mA to +100mA |
| Operating Junction Temperature Range[2] | –40°C to 125°C |
| Storage Temperature Range | –65°C to 150°C |

[1] Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only. Otherwise, permanent damage can occur.

[2] The LTC7892 is specified over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in Watts) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$, where $\theta_{JA}$ is the package thermal impedance and equals 33°C/W for the 40-lead (6 mm × 6 mm), side wettable, quad flat no-lead (QFN) package.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS




NOTES
1. THE EXPOSED PAD (PIN 41) MUST BE SOLDERED TO PCB GROUND FOR RATED ELECTRICAL AND THERMAL PERFORMANCE.

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***Figure 3. Pin Configuration***

**Table 3. Pin Descriptions**

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | FREQ | Frequency Control pin for the internal Voltage Controlled Oscillator (VCO). Connect FREQ to GND for a fixed frequency of 370kHz. Connect FREQ to $INTV_{CC}$ for a fixed frequency of 2.25MHz. Program frequencies between 100kHz and 3MHz by using a resistor between FREQ and GND. Minimize the capacitance on FREQ. |
| 2 | MODE | Mode Select Input. This input determines how the LTC7892 operates at light loads. Connect MODE to GND to select Burst Mode® operation. An internal 100kΩ resistor to GND also invokes Burst Mode operation when MODE is floating. Connect MODE to $INTV_{CC}$ to force continuous inductor current operation. Tying MODE to $INTV_{CC}$ through a 100kΩ resistor selects the PS operation. |
| 3 | PLLIN/ SPREAD | External Synchronization Input to Phase Detector/Spread Spectrum Enable. When an external clock is applied to PLLIN/SPREAD, the PLL forces the rising BGxx1 signal to synchronize with the rising edge of the external clock. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator, or to GND to disable spread spectrum dithering. |
| 4 | RUN1 | Run Control Input for Channel 1. Forcing RUN1 less than 1.08V disables controller switching. Forcing RUN1 and RUN2 less than 0.7V shuts down the LTC7892, reducing $I_Q$ to approximately 1µA. Tie the RUN1 pin to $V_{BIAS}$ to ensure it is always in operation. |

| | | |
|---|---|---|
| 5 | RUN2 | Run Control Input for Channel 2. Forcing RUN2 less than 1.08V disables controller switching. Forcing RUN1 and RUN2 less than 0.7V shuts down the LTC7892, reducing $I_Q$ to approximately 1µA. Tie the RUN2 pin to $V_{BIAS}$ to ensure it is always in operation. |
| 6 | GND | Ground. The GND pin and the exposed pad must be soldered to PCB ground for rated electrical and thermal performance. |
| 7 | DRVUV | $DRV_{CC}$ UVLO and $EXTV_{CC}$ Switchover Program Pin. DRVUV determines the $INTV_{CC}$ UVLO and $EXTV_{CC}$ switchover rising and falling thresholds, as listed in *Table 1*. |
| 8 | DRVSET | $INTV_{CC}$ Regulation Program Pin. DRVSET sets the regulation point for the $INTV_{CC}$ LDO linear regulators. Connect DRVSET to GND to set $INTV_{CC}$ to 5V. Connect DRVSET to $INTV_{CC}$ to set $INTV_{CC}$ to 5.5V. Program voltages between 4V and 5.5V by placing a resistor (43kΩ to 110kΩ) between DRVSET and GND. The resistor and an internal 20µA source current create a voltage used by the $INTV_{CC}$ LDO regulator to set the regulation point. |
| 9 | DTCA | Dead Time Control Pin for Bottom FET Off to Top FET On Delay. Connect DTCA to GND to program an adaptive dead time delay of approximately 15ns. Connect a resistor between DTCA and GND to program a nonadaptive (open-loop) dead time delay from 7ns to 60ns. |
| 10 | DTCB | Dead Time Control Pin for Top FET Off to Bottom FET On Delay. Connect to GND to program an adaptive TG off to BG on a dead time delay of approximately 15ns. Connect a resistor between DTCB and GND to program a nonadaptive (open-loop) TG off to BG on dead time from 7ns to 60ns. |
| 11 | $SENSE2^+$ | Positive Input to the Differential Current Comparator for Channel 2. The $SENSE2^+$ pin supplies current to the current comparator for Channel 2 when $SENSE2^+$ is greater than $INTV_{CC}$. |
| 12 | $SENSE2^-$ | Negative Input to the Differential Current Comparator for Channel 2. The ITH2 pin voltage and controlled offset between the $SENSE2^+$ and $SENSE2^-$ pins, in conjunction with the current sense resistor ($R_{SENSE}$), set the current trip threshold. |
| 13 | $V_{FB2}$ | Error Amplifier Feedback Input for Channel 2. $V_{FB2}$ Receives the remotely sensed feedback voltage for channel 2 from an external resistive divider across the output. Tie $V_{FB2}$ to $INTV_{CC}$ for a 2-phase single output application, in which both channels share $V_{FB1}$, ITH1, and SS1. |
| 14 | ITH2 | Error Amplifier Output and Switching Regulator Compensation Point for Channel 2. The current comparator trip point increases with this control voltage. |
| 15 | SS2 | External Soft Start Input for Channel 2. SS2 regulates the $V_{FB2}$ voltage to the lesser of 1.2V or the voltage on the SS2 pin. An internal 12µA pull-up current source is connected to SS2. A capacitor to GND at SS2 sets the ramp time to the final regulated output voltage. The ramp time is equal to 1ms for every 10nF of capacitance. |
| 16 | ILIM | Current Comparator Sense Voltage Range Input. Tying ILIM to GND or $INTV_{CC}$ or floating it sets the maximum current sense threshold to one of three different levels (25mV, 75mV, and 50mV, respectively). |
| 17 | PGOOD2 | Power Good Open-Drain Logic Output for Channel 2. PGOOD2 is pulled to the ground when the voltage on $V_{FB2}$ is not within ±10% of its set point. |

| | | |
|---|---|---|
| 18 | TGUP2 | High Current Gate Driver Pull-Up for Top FET for Channel 2. TGUP2 pulls up to BOOST2. Tie TGUP2 directly to the top FET gate for maximum gate drive transition speed on the gate rising edge. A resistor can be tied between TGUP2 and the top FET gate to adjust the gate rising slew rate. |
| 19 | TGDN2 | High Current Gate Driver Pull-Down for Top FET for Channel 2. TGDN2 pulls down to SW. Tie TGDN2 directly to the top FET gate for maximum gate drive transition speed on the gate falling edge. A resistor can be tied between TGDN2 and the top FET gate to adjust the gate falling slew rate. |
| 20 | SW2 | Switch Node Connection to Inductor for Channel 2. |
| 21 | BOOST2 | Bootstrapped Supply to the Top Side Floating Driver for Channel 2. Connect a capacitor between the BOOST2 and SW2 pins. An internal switch provides power to the BOOST2 pin from $DRV_{CC}$ when the bottom FET turns on. The voltage swing at the BOOST2 pin is from $DRV_{CC}$ to ($V_{OUT2}$ + $DRV_{CC}$). |
| 22 | BGDN2 | High Current Gate Driver Pull-Down for Bottom FET for Channel 2. BGDN2 pulls down to GND. Tie BGDN2 directly to the bottom FET gate for maximum gate drive transition speed on the gate falling edge. A resistor can be tied between BGDN2 and the bottom FET gate to adjust the gate falling slew rate. BGDN2 also serves as the Kelvin sense of the bottom FET gate during turn-on. |
| 23 | BGUP2 | High Current Gate Driver Pull-Up for Bottom FET for Channel 2. BGUP2 pulls up to $DRV_{CC}$. Tie BGUP2 directly to the bottom FET gate for maximum gate drive transition speed on the gate rising edge. A resistor can be tied between BGUP2 and the bottom FET gate to adjust the gate falling slew rate. BGUP2 also serves as the Kelvin sense of the bottom FET gate during turn-off. |
| 24 | $DRV_{CC}$ | Gate Driver Power Supply Pin. The gate drivers are powered from $DRV_{CC}$. Connect $DRV_{CC}$ to $INTV_{CC}$ by a separate trace to the $INTV_{CC}$ bypass capacitor. |
| 25 | $INTV_{CC}$ | Output of the Internal Low Dropout Regulator. The $INTV_{CC}$ voltage regulation point is set by the DRVSET pin. $INTV_{CC}$ must be decoupled to ground with a 4.7µF to 10µF ceramic or other low equivalent series resistance (ESR) capacitor. |
| 26 | $EXTV_{CC}$ | External Power Input to an Internal LDO Connected to $DRV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal $V_{BIAS}$ LDO whenever $EXTV_{CC}$ exceeds the $EXTV_{CC}$ switchover voltage. See $EXTV_{CC}$ Connection *Power and Bias Supplies ($V_{BIAS}$, $EXTV_{CC}$, $DRV_{CC}$, $INTV_{CC}$)* section. Do not exceed 30V on $EXTV_{CC}$. Connect $EXTV_{CC}$ to the ground if the $EXTV_{CC}$ LDO is not used. |
| 27 | $V_{BIAS}$ | Main Supply Pin. A bypass capacitor should be tied between $V_{BIAS}$ and GND. |
| 28 | BGUP1 | High Current Gate Driver Pull-Up for Bottom FET for Channel 1. BGUP1 pulls up to $DRV_{CC}$. Tie BGUP1 directly to the bottom FET gate for maximum gate drive transition speed on the gate rising edge. A resistor can be tied between BGUP1 and the bottom FET gate to adjust the gate falling slew rate. BGUP1 also serves as the Kelvin sense of the bottom FET gate during turn-off. |
| 29 | BGDN1 | High Current Gate Driver Pull-Down for Bottom FET for Channel 1. BGDN1 pulls down to GND. Tie BGDN1 directly to the bottom FET gate for maximum gate drive transition speed on the gate falling edge. A resistor can be tied between BGDN1 and the bottom |

| | | |
|---|---|---|
| | | FET gate to adjust the gate falling slew rate. BGDN1 also serves as the Kelvin sense of the bottom FET gate during turn-on. |
| 30 | BOOST1 | Bootstrapped Supply to the Top Side Floating Driver for Channel 1. Connect a capacitor between the BOOST1 and SW1 pins. An internal switch provides power to the BOOST1 pin from $DRV_{CC}$ when the bottom FET turns on. The voltage swing at the BOOST1 pin is from $DRV_{CC}$ to ($V_{OUT1}$ + $DRV_{CC}$). |
| 31 | SW1 | Switch Node Connection to Inductor for Channel 1. |
| 32 | TGDN1 | High Current Gate Driver Pull-Down for Top FET for Channel 1. TGDN1 pulls down to SW. Tie TGDN1 directly to the top FET gate for maximum gate drive transition speed on the gate falling edge. A resistor can be tied between TGDN1 and the top FET gate to adjust the gate falling slew rate. |
| 33 | TGUP1 | High Current Gate Driver Pull-Up for Top FET for Channel 1. TGUP1 pulls up to BOOST1. Tie TGUP1 directly to the top FET gate for maximum gate drive transition speed on the gate rising edge. A resistor can be tied between TGUP1 and the top FET gate to adjust the gate rising slew rate. |
| 34 | PGOOD1 | Power Good Open Drain Logic Output for Channel 1. PGOOD1 is pulled to ground when the voltage on $V_{FB1}$ is not within ±10% of its set point. |
| 35 | VPRG1 | Output Voltage Control Pin for Channel 1. VPRG1 sets the adjustable output mode for Channel 1 using external feedback resistors or fixed 28V/24V output mode. Floating VPRG1 programs the output from 1.2V to 100V with an external resistor divider, regulating $V_{FB1}$ to 1.2V. Connect VPRG1 to $INTV_{CC}$ or GND to program the output to 28V or 24V, respectively, through an internal resistor divider on $V_{FB1}$. |
| 36 | SS1 | External Soft Start Input for Channel 1. SS1 regulates the $V_{FB1}$ voltage to the lesser of 1.2V or the voltage on the SS1 pin. An internal 12µA pull-up current source is connected to SS1. A capacitor to GND at SS1 sets the ramp time to the final regulated output voltage. The ramp time is equal to 1ms for every 10nF of capacitance. |
| 37 | ITH1 | Error Amplifier Output and Switching Regulator Compensation Point for Channel 1. The current comparator trip point increases with this control voltage. |
| 38 | $V_{FB1}$ | Error Amplifier Feedback Input for Channel 1. If the VPRG1 pin is floating, $V_{FB1}$ receives the remotely sensed feedback voltage for Channel 1 from an external resistive divider across the output. If VPRG1 is tied to $INTV_{CC}$ or GND, the $V_{FB1}$ pin receives the remotely sensed output voltage directly. |
| 39 | $SENSE1^-$ | Negative Input to the Differential Current Comparator for Channel 1. The ITH1 pin voltage and controlled offset between the $SENSE1^+$ and $SENSE1^-$ pins, in conjunction with the current sense resistor ($R_{SENSE}$), set the current trip threshold. |
| 40 | $SENSE1^+$ | Positive Input to the Differential Current Comparator for Channel 1. The $SENSE1^+$ pin supplies current to the current comparator for Channel 1 when $SENSE1^+$ is greater than $INTV_{CC}$. |
| 41 | GND (Exposed Pad) | Ground (Exposed Pad). The exposed pad must be soldered to PCB ground for rated electrical and thermal performance. |

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

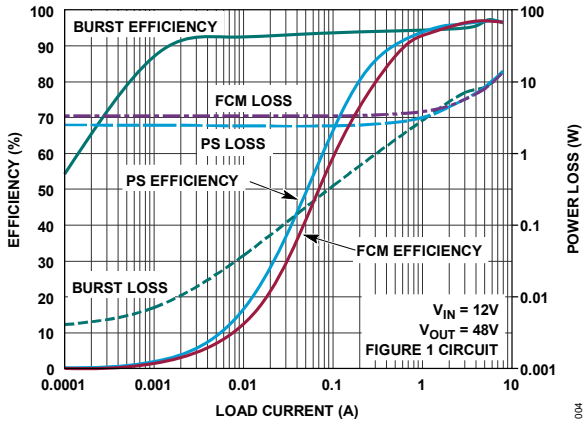



*Figure 4. Efficiency and Power Loss vs Load Current*

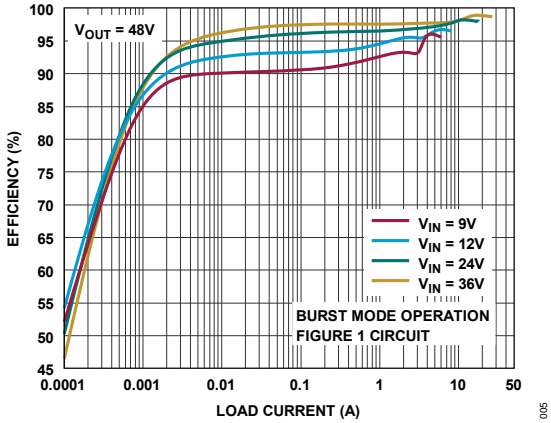



*Figure 5. Efficiency vs Load Current*

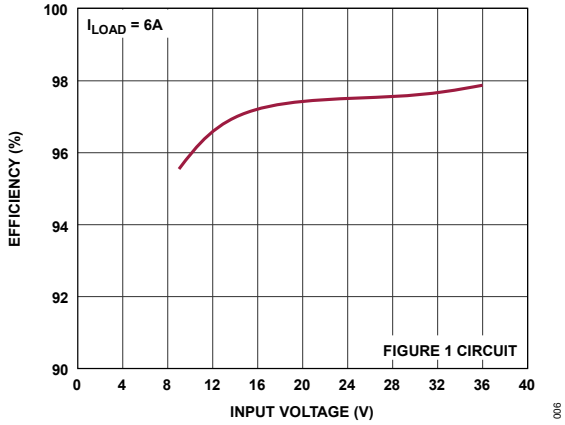



*Figure 6. Efficiency vs Input Voltage*

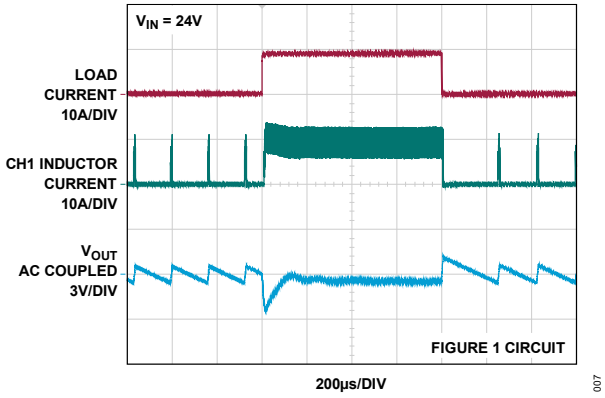



*Figure 7. Load Step Burst Mode® Operation*

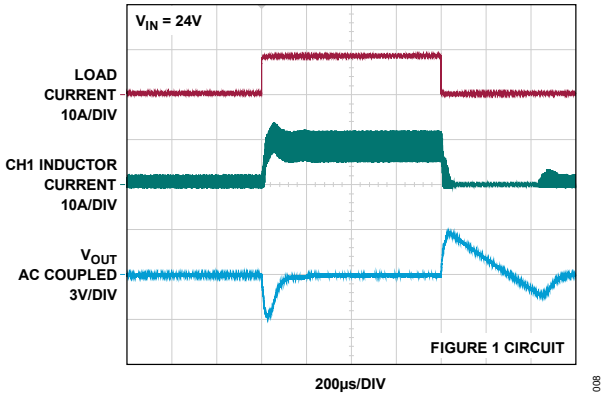



*Figure 8. Load Step PS Mode*

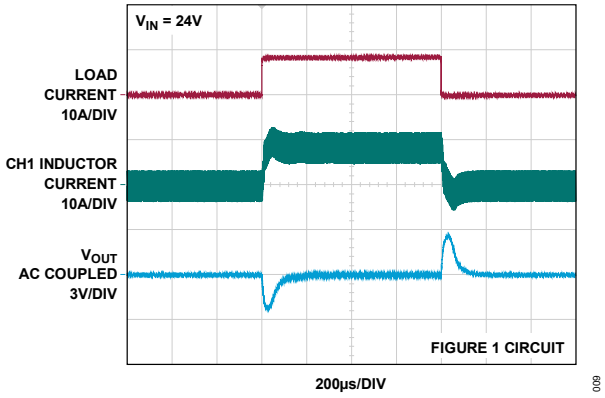



*Figure 9. Load Step FCM*

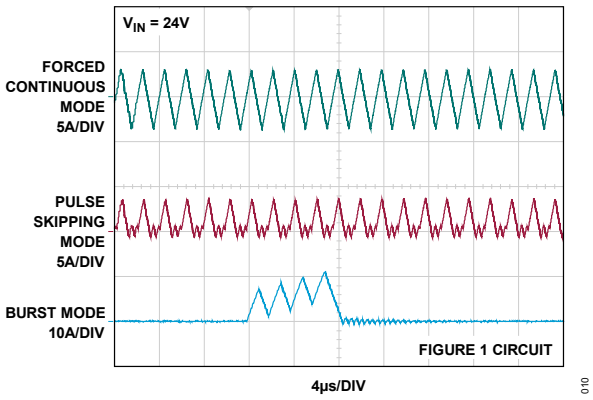



*Figure 10. Inductor Current at Light Load*

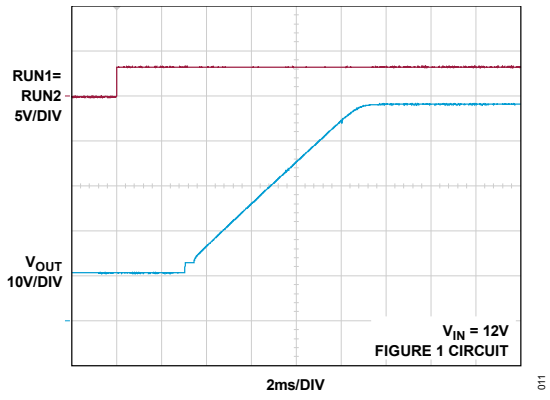



*Figure 11. Soft Start-Up*

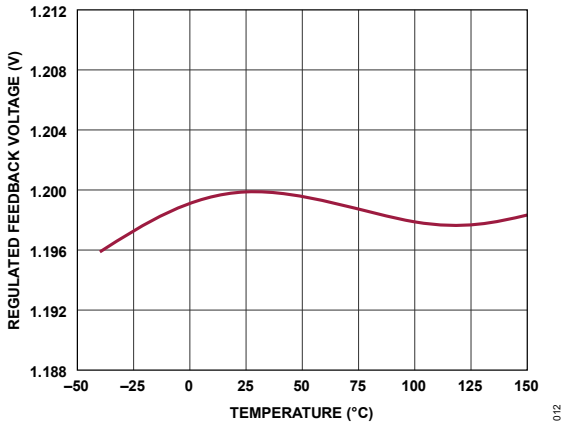



*Figure 12. Regulated Feedback Voltage vs Temperature*

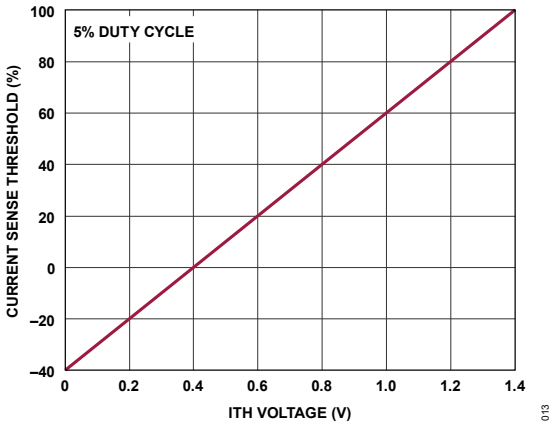



*Figure 13. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs $V_{ITHx}$ in FCM*

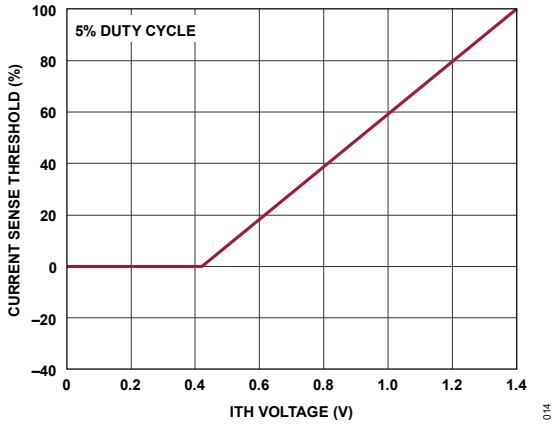



*Figure 14. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs $V_{ITHx}$ Voltage in PS Mode*

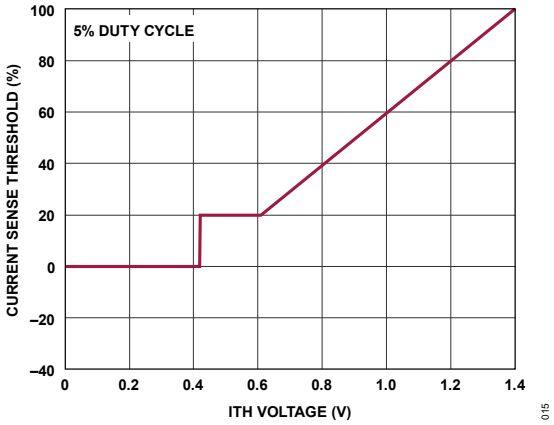



*Figure 15. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs $V_{ITHx}$ Voltage in Burst Mode*

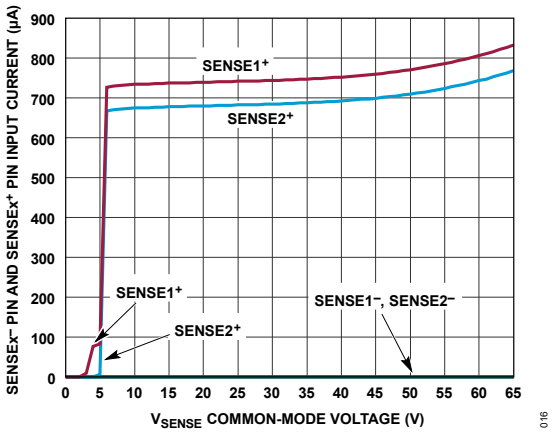



*Figure 16. SENSEx⁺ and SENSEx⁻ Pin Input Bias Current vs $V_{SENSE}$ Common-Mode Voltage*

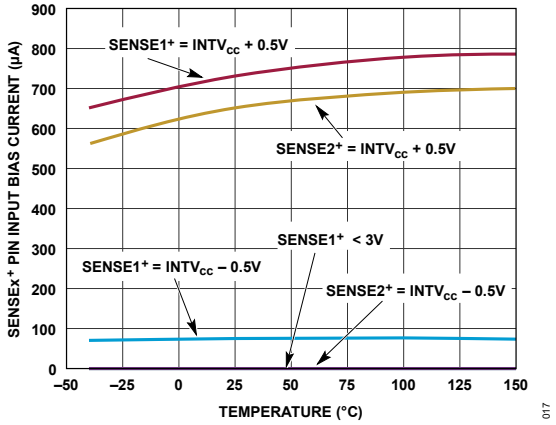



*Figure 17. SENSEx⁻ Pin Input Current vs. Temperature*

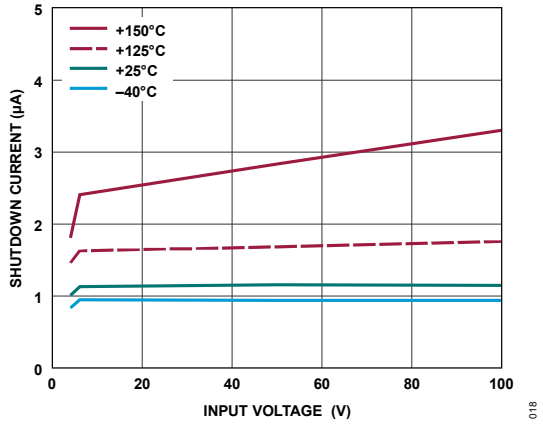



*Figure 18. Shutdown Current vs. Input Voltage*

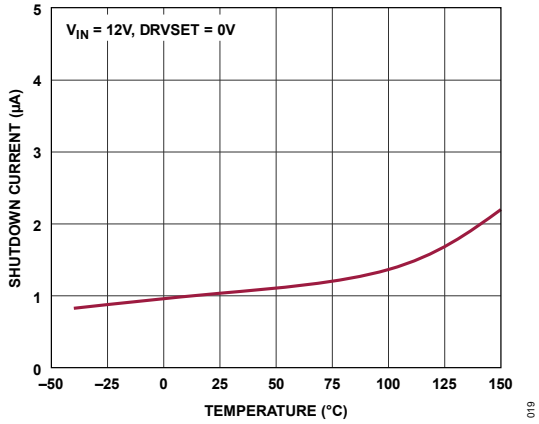



*Figure 19. Shutdown Current vs Temperature*

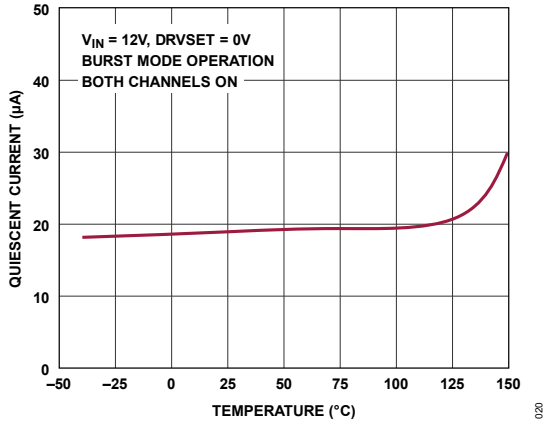



*Figure 20. Quiescent Current vs Temperature*

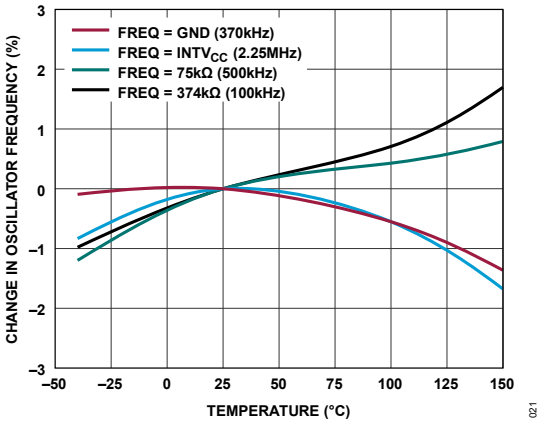



*Figure 21. Oscillator Frequency vs. Temperature*

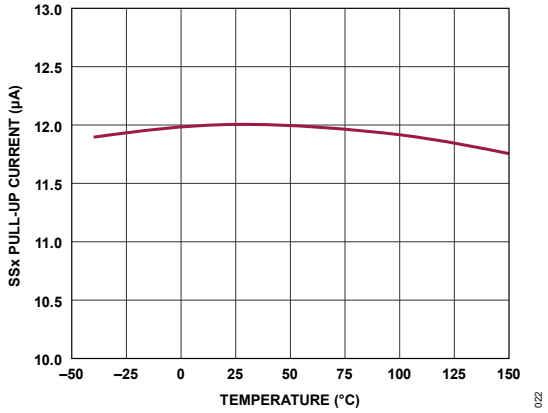



*Figure 22. SSx Pull-Up Current vs. Temperature*

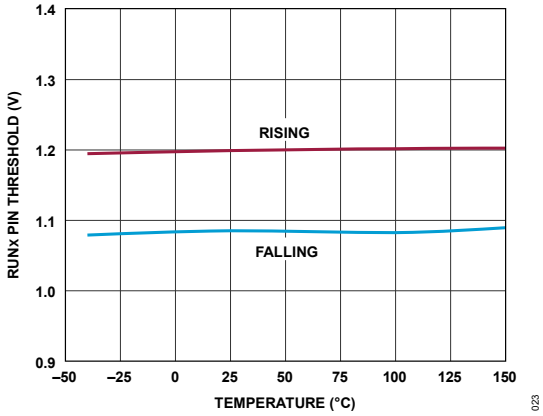



*Figure 23. RUNx Pin Threshold vs. Temperature*

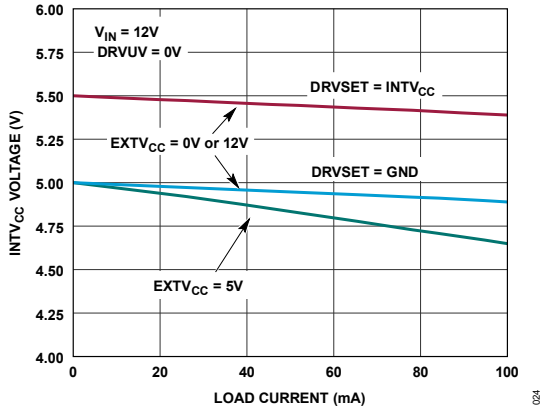



*Figure 24. $INTV_{CC}$ Voltage vs. Load Current*

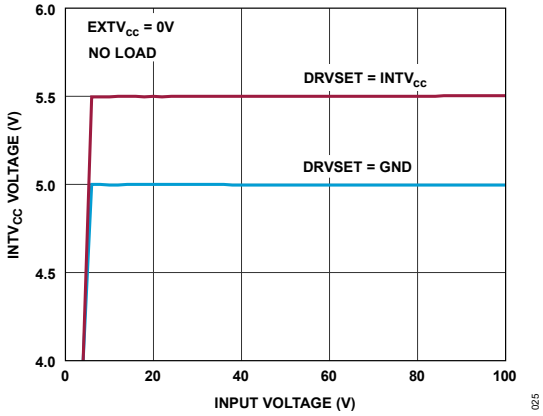



*Figure 25. $INTV_{CC}$ Voltage vs. Input Voltage*

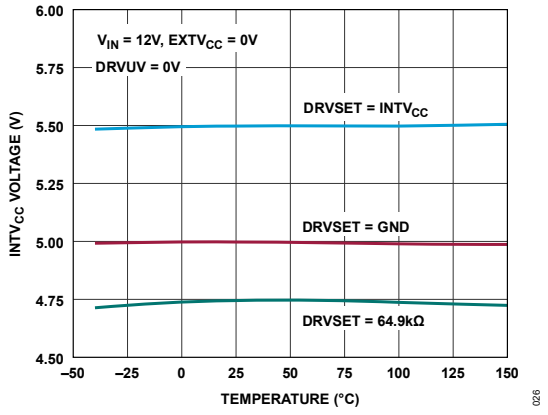



*Figure 26. $INTV_{CC}$ Voltage vs. Temperature*

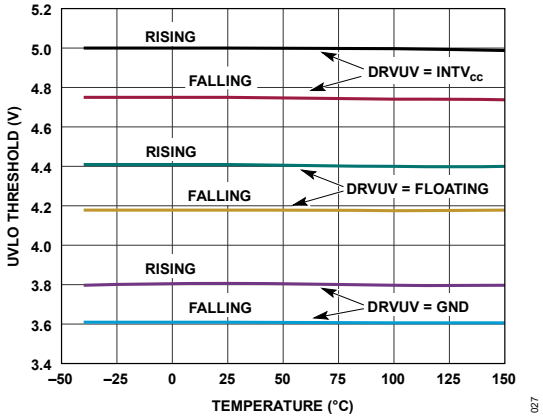



*Figure 27. UVLO Threshold vs. Temperature*

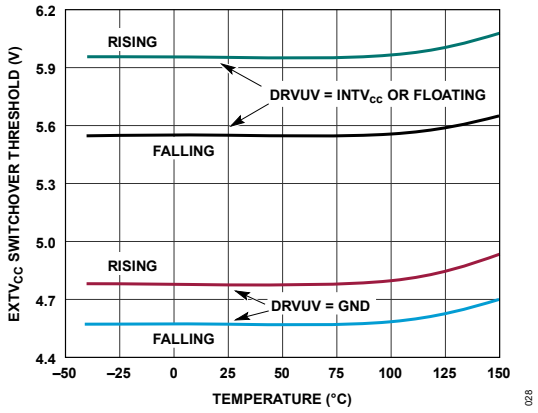



*Figure 28. $EXTV_{CC}$ Switchover Threshold vs. Temperature*

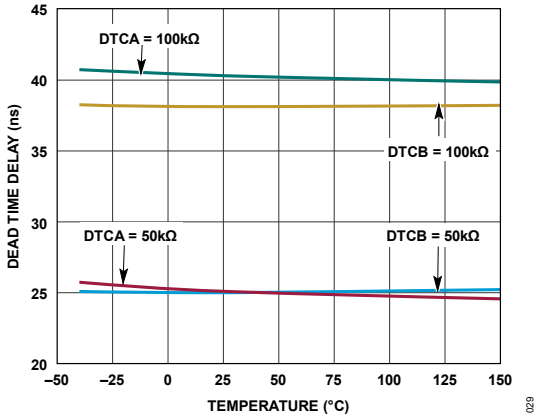



*Figure 29. Dead Time Delay vs. Temperature*

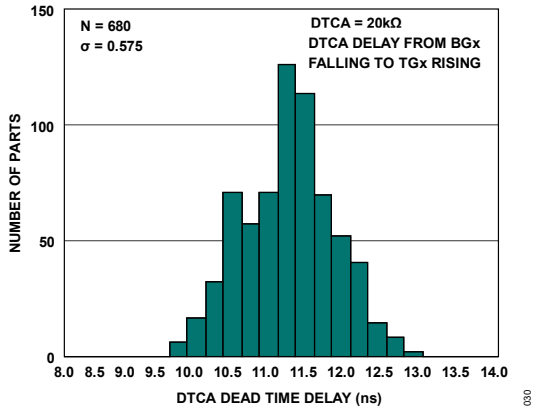



*Figure 30. DTCA = 20kΩ Dead Time Delay Histogram*

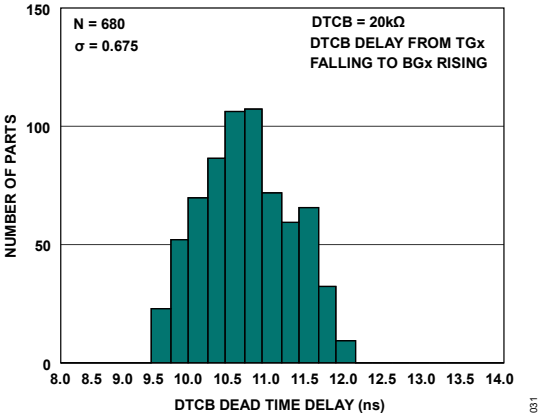



*Figure 31. DTCB = 20kΩ Dead Time Delay Histogram*

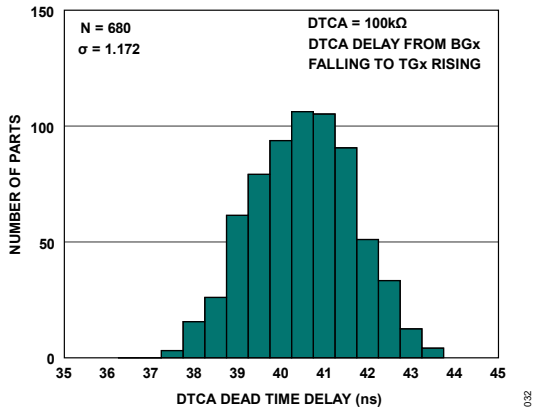



*Figure 32. DTCA = 100kΩ Dead Time Delay Histogram*

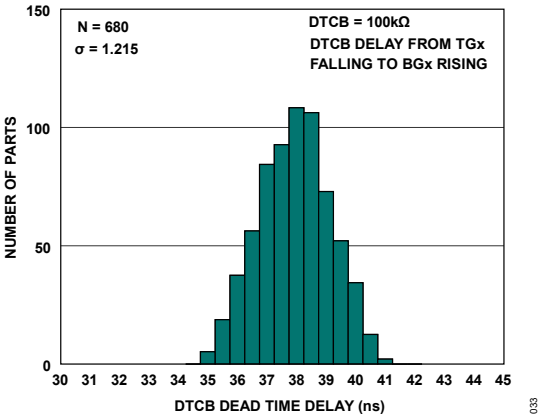
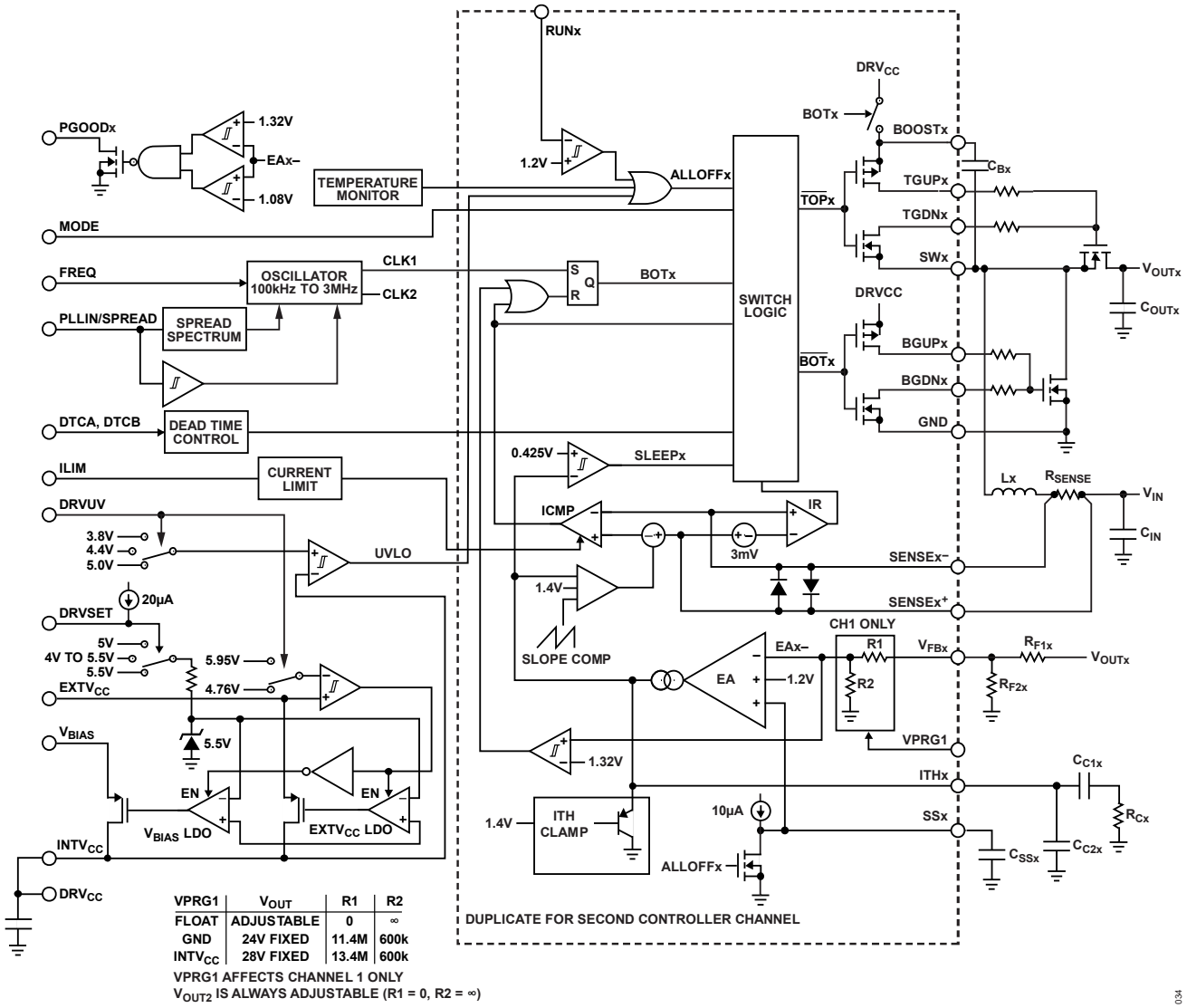



*Figure 33. DTCB = 100kΩ Dead Time Delay Histogram*

## FUNCTIONAL DIAGRAM




| VPRG1 | $V_{OUT}$ | R1 | R2 |
|---|---|---|---|
| FLOAT | ADJUSTABLE | 0 | ∞ |
| GND | 24V FIXED | 11.4M | 600k |
| $INTV_{CC}$ | 28V FIXED | 13.4M | 600k |

VPRG1 AFFECTS CHANNEL 1 ONLY

$V_{OUT2}$ IS ALWAYS ADJUSTABLE (R1 = 0, R2 = ∞)

*Figure 34. Functional Diagram*

# THEORY OF OPERATION

## Main Control Loop

The LTC7892 is a dual synchronous boost controller utilizing a constant frequency, peak current mode architecture. The two controller channels operate 180° out of phase, which reduces the required input capacitance and power supply-induced noise. During normal operation, the external bottom FET turns on when the clock sets the set/reset (SR) latch, causing the inductor current to increase. The main switch is turned off when the main current comparator, ICMP, resets the SR latch. After the bottom FET is turned off each cycle, the top FET is turned on, which causes the inductor current to decrease until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITHx pin, which is the output of the error amplifier. The error amplifier compares the output voltage feedback signal at the $V_{FBx}$ pin, (which is generated with an external resistor divider connected across the output voltage, $V_{OUTx}$, to GND) to the internal 1.2V reference voltage. When the load current increases, it causes a slight decrease in $V_{FBx}$ relative to the reference, which causes the error amplifier to increase the ITHx voltage until the average inductor current matches the new load current.

## Power and Bias Supplies ($V_{BIAS}$, $EXTV_{CC}$, $DRV_{CC}$, $INTV_{CC}$)

The $INTV_{CC}$ pin supplies power for the top and bottom FET drivers and most of the internal circuitry. The supply for the FET drivers is derived from the $DRV_{CC}$ pin, which must be tied to the $INTV_{CC}$ pin to supply power to the gate drivers. LDOs (low dropout linear regulators) are available from the $V_{BIAS}$ and $EXTV_{CC}$ pins to provide power to $INTV_{CC}$, which can be programmed from 4V to 5.5V through control of the DRVSET pin. When the $EXTV_{CC}$ pin is tied to a voltage less than its switchover voltage, the $V_{BIAS}$ LDO supplies power to $INTV_{CC}$. If $EXTV_{CC}$ is taken more than its switchover voltage, the $V_{BIAS}$ LDO regulator turns off, and the $EXTV_{CC}$ LDO is turned on. When enabled, the $EXTV_{CC}$ LDO regulator supplies power to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high-efficiency external source.

## High Side Bootstrap Capacitor

Each top FET driver is biased from the floating bootstrap capacitor $C_B$, which normally recharges through an internal switch between BOOSTx and $DRV_{CC}$ whenever the bottom FET turns on. The internal switch becomes high impedance whenever the bottom FET is off, which prevents the bootstrap capacitor from overcharging if SWx rings less than GND during the dead times.

If the input voltage increases to a voltage close to a voltage close to its output, the loop can enter dropout and attempt to turn on the top FET continuously. If the bottom FET is not turned on frequently enough to recharge the bootstrap capacitor, the top FET may not be fully enhanced, or it may even be completely off when the controller attempts to turn on the top FET.

## Dead Time Control (DTCA and DTCB Pins)

The LTC7892 dead time delays can be programmed from 7ns to 60ns through the configuration of the DTCA and DTCB pins. The DTCA pin programs the dead time associated with the bottom FET turning off and the top FET turning on (SWx going from low to high). The DTCB pin programs the dead time associated with the top FET turning off and the bottom FET turning on (SWx going from high to low).

Tying the DTCA pin to ground programs adaptive dead time control, which means the driver logic waits for the bottom FET to turn off before turning on the top FET. Adaptive dead time control results in dead times of approximately 15ns between BGx falling to TGx rising. Placing a resistor between the DTCA pin and ground programs, the open-loop delay between the bottom FET turning off and the top FET turning on. This delay can be programmed between 7ns and 60ns. See the *Dead Time Control (DTCA and DTCB Pins)* section for more information.

Tying the DTCB pin to ground programs adaptive dead time control, which means the driver logic waits for the top FET to turn off before turning on the bottom FET. Adaptive dead time control results in dead times of approximately 15ns between TGx falling to BGx rising. Placing a resistor between the DTCB pin and ground programs the open-loop delay between the top FET turning off and the bottom FET turning on. This delay can be programmed between 7ns and 60ns. See the *Dead Time Control (DTCA and DTCB Pins)* section for more information.

## Start-Up and Shutdown (RUN and SS Pins)

The two channels of the LTC7892 can be independently shut down using the RUN1 and RUN2 pins. Pulling a RUNx pin below 1.1V shuts down the main control loop for that channel. Pulling both RUNx pins below 0.7V disables both controllers and most internal circuits, including the $INTV_{CC}$ LDO regulators. In this shutdown state, the LTC7892 draws only 1µA of current from $V_{BIAS}$.

The RUNx pin needs to be externally pulled up or driven directly by logic. Each RUNx pin can tolerate up to 100V. See *Absolute Maximum Ratings* for more details. Therefore, the RUNx pin can be conveniently tied to $V_{IN}$ or $V_{BIAS}$ in always-on applications where one or both controllers are enabled continuously and never shut down. Additionally, a resistive divider from $V_{IN}$ to a RUNx pin can be used to set a precise input undervoltage lockout so that the power supply does not operate below a user-adjustable level.

The start-up of each channel's output voltage $V_{OUTx}$ is controlled by the voltage on the corresponding SSx pin. When the voltage on the SSx pin is less than the 1.2V internal reference voltage, the LTC7892 regulates the $V_{FBx}$ voltage to the SSx pin voltage instead of the 1.2V reference voltage. This allows the SSx pin to be used as a soft-start which smoothly ramps the output voltage on start-up. An external capacitor from the SSx pin to GND is charged by an internal 12µA pull-up current, creating a voltage ramp on the SSx pin. As the SSx voltage rises linearly from 0V to 1.2V (and beyond), the output voltage $V_{OUTx}$ rises smoothly to its final value.

## Light Load Operation: Burst Mode Operation, Pulse-Skipping Mode, or Forced Continuous Mode (MODE Pin)

The LTC7892 can be set to enter high-efficiency Burst Mode operation, constant frequency PS mode, or forced continuous conduction mode at low load currents.

To select the Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select PS mode, tie the MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V. An internal 100kΩ resistor to ground invokes Burst Mode operation when the MODE pin is floating, and PS mode when the MODE pin is tied to $INTV_{CC}$ through an external 100kΩ resistor.

When the controllers are enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of its maximum value, even though the voltage on the ITHx pin might indicate a lower value. If

the average inductor current is higher than the load current, the error amplifier will decrease the voltage on the ITHx pin. When the ITHx voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode), and both external FETs are turned off. The ITHx pin is then disconnected from the output of the error amplifier and parked at 0.45V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current ($I_Q$) drawn by the LTC7892. If one channel is in sleep mode and the other channel is shut down, the LTC7892 draws only 15µA of $I_Q$. If both channels are in sleep mode, the LTC7892 draws only 20µA of $I_Q$.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the output of the error amplifier rises. When the output voltage drops enough, the ITHx pin is reconnected to the output of the error amplifier, the sleep signal goes low, and the controller resumes normal operation by turning on the bottom FET on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the top FET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITHx pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in the Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

When the MODE pin is connected for pulse-skipping mode, the LTC7892 operates in pulse-width modulation (PWM) pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At very light loads, ICMP can remain tripped for several cycles and force the bottom FET to stay off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. PS mode provides higher low current efficiency than FCM, but not nearly as high as Burst Mode operation.

Unlike FCM and pulse-skipping mode, Burst Mode cannot be synchronized to an external clock. Therefore, if Burst Mode operation is selected and the switching frequency is synchronized to an external clock applied to the PLLIN/SPREAD pin, the LTC7892 switches from Burst Mode to FCM.

## Frequency Selection, Spread Spectrum, and Phase-Locked Loop (FREQ and PLLIN/SPREAD Pins)

The free-running switching frequency of the LTC7892 controller is selected using the FREQ pin. Tying FREQ to GND selects 370kHz, while tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 100kHz and 3MHz.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the LTC7892 can operate in spread spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency within typical boundaries of the frequency set by the FREQ pin and +20%.

A PLL is available on the LTC7892 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. The PLL of the LTC7892 aligns the turn-on of the external bottom FET of Channel 1 to the rising

edge of the synchronizing signal. The turn-on of the external bottom FET for Channel 2 is 180° out-of-phase to the rising edge of the external clock source.

The PLL frequency is prebiased to the free running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only needs to make slight changes to synchronize the rising edge of the external clock to the rising edge of BG1. For a more rapid lock-in to the external clock, use the FREQ pin to set the internal oscillator to approximately the frequency of the external clock. The PLL of the LTC7892 is guaranteed to lock to an external clock source whose frequency is between 100kHz and 3MHz.

The PLLIN/SPREAD pin is Transistor-transistor logic (TTL) compatible with thresholds of 1.6V (rising) and 1.1V (falling) and is guaranteed to operate with a clock signal swing of 0.5V to 2.2V.

## Output Overvoltage Protection

The LTC7892 has an overvoltage comparator for each channel that guards against transient overshoots and other more serious conditions that can cause output overvoltage. When the $V_{FBx}$ pin rises more than 10% above its regulation point of 1.2V, the bottom FET is turned off, and the inductor current is not allowed to reverse.

## Power Good

The LTC7892 has a PGOODx pin for each channel that is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOODx pin low when the $V_{FBx}$ voltage is not within ±10% of the 1.2V reference. The PGOODx pin is also pulled low when the RUNx pin is low (shut down). When the $V_{FBx}$ voltage is within the ±10% requirement, the MOSFET is turned off, and the PGOODx pin is allowed to be pulled up by an external resistor to a source no greater than 6V, such as $INTV_{CC}$.

When LTC7892 is operated in a 2-phase single output configuration, the output voltage is sensed by the $V_{FB1}$ pin only. The PGOOD1 pin is pulled low when the $V_{FB1}$ voltage is not within ±10% of the 1.2V reference. The PGOOD2 should be left floating.

# APPLICATIONS INFORMATION

*Figure 50* is a basic LTC7892 application circuit. External component selection is largely driven by the load requirement and begins with the selection of the inductor, current sense components, operating frequency, and light load operating mode. The remaining power stage components, consisting of the input and output capacitors, and power FETs can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then, the remaining external components are selected, such as for soft-start, biasing, and loop compensation.

## Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of FET switching and gate charge losses. In addition to this trade-off, the effect of inductor value on ripple current and low current operation must also be considered. The inductor value has a direct effect on the ripple current.

The maximum average inductor current ($I_{L(MAX)}$) in continuous conduction mode is equal to the maximum average output current ($I_{OUT(MAX)}$) multiplied by a factor of $V_{OUT}/V_{IN}$, or $I_{L(MAX)} = I_{OUT(MAX)} \bullet V_{OUT}/V_{IN}$. Be aware that the maximum output current decreases with decreasing $V_{IN}$. The choice of $I_{L(MAX)}$, therefore, depends on the maximum load current for a regulated $V_{OUT}$ at the minimum normal operating $V_{IN}$. The choice of $I_{L(MAX)}$, therefore, depends on the maximum load current for a regulated $V_{OUT}$ at the minimum normal operating $V_{IN}$. If the load current for a given $V_{IN}$ is exceeded, $V_{OUT}$ will decrease until the $I_{L(MAX)} = I_{OUT(MAX)} \bullet V_{OUT}/V_{IN}$ equation is satisfied.

The inductor ripple current ($\Delta I_L$) for a boost converter is given by Equation 1:

$$\Delta I_L = \frac{1}{f \bullet L} V_{IN} \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (1)$$

Accepting larger values of $\Delta I_L$ allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \bullet I_{L(MAX)}$. The maximum $\Delta I_L$ for a boost converter occurs at $V_{IN} = 1/2\ V_{OUT}$.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by $R_{SENSE}$. Lower inductor values (higher $\Delta I_L$) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low-current operation. In the Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

## Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High-efficiency regulators generally cannot afford the core loss found in low-cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance value selected. As inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire, and therefore, copper losses will increase.

Ferrite designs have a very low core loss and are preferred for high switching frequencies. Therefore, design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This collapse results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

## Current Sense Selection

The LTC7892 can be configured to use either inductor DC resistance (DCR) sensing or low-value resistor sensing. The choice between the two current sensing schemes is a design trade-off between cost, power consumption, and accuracy. DCR sensing is popular because it saves expensive current sensing resistors and is more power efficient, particularly in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. The selection of other external components begins with the selection of $R_{SENSE}$ (if $R_{SENSE}$ is used) and the inductor value.

The SENSEx$^+$ and SENSEx$^-$ pins are the inputs to the current comparator. The common-mode voltage range on these pins is 0V to 65V (see *Absolute Maximum Ratings* for more details), allowing the LTC7892 to operate from inputs over this full range. The SENSEx$^-$ pins are high impedance, drawing less than ≈1µA. This high impedance allows the current comparator to be used in inductor DCR sensing.

The impedance of the SENSEx$^+$ pin changes depending on the common-mode voltage. When less than $INTV_{CC}$ – 0.5V, the SENSEx$^+$ pin is relatively high impedance, drawing ≈ 75µA for SENSE1$^+$ and ≈ 1µA for SENSE2$^+$. When the SENSEx$^+$ pin is above $INTV_{CC}$ + 0.5V, a higher current (≈700µA) flows into each pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current. The SENSE1$^+$ pin has an additional ≈ 75µA current when its voltage is above 3.2V to bias internal circuitry from $V_{IN}$ instead of $V_{BIAS}$, which reduces the input referred supply current.

Filter components mutual to the sense lines must be placed close to the LTC7892, and the sense lines must run close together to a Kelvin connection underneath the current sense element, as shown in *Figure 35*. Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (see *Figure 37*), the R1 resistor should be placed close to the switching node to prevent noise from coupling into sensitive small-signal nodes.

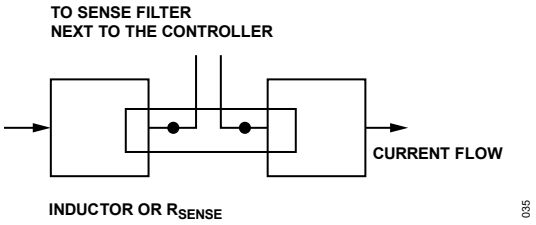



***Figure 35. Sense Lines Placement with Inductor or Sense Resistor***

## Low Value Resistor Current Sensing

*Figure 36* shows a typical sensing circuit using a discrete resistor. $R_{SENSE}$ is chosen based on the required output current. The current comparator has a maximum threshold $V_{SENSE(MAX)}$ of 50mV, 25mV, or 75mV, as determined by the state of the of the ILIM pin. The current comparator threshold voltage sets the peak inductor current.

Using the maximum inductor current ($I_{L(MAX)}$) and ripple current ($\Delta I_L$) (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 2, as follows:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (2)$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ as shown in *Table 1* (Electrical Characteristics table).

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal for lower inductor value (<3µH) or higher current (>5A) applications. This error is proportional to the input voltage and can degrade line regulation or cause loop instability. Placing an RC filter (filter resistor, $R_F$ and filter capacitor, $C_F$) into the SENSEx$^+$ and SENSEx$^-$ pins, as shown in *Figure 36*, can be used to compensate for this error. For optimal cancellation of the ESL, set the RC filter time constant to $R_F \times C_F = ESL/R_{SENSE}$. In general, select $C_F$ to be in the range of 1nF to 10nF and calculate the corresponding $R_F$. Surface-mount sense resistors in low ESL and wide footprint geometries are recommended to minimize this error. If not specified in the manufacturer's data sheet, the ESL can be approximated as 0.4nH for a resistor with a 1206 footprint and 0.2nH for a resistor with a 1225 footprint.

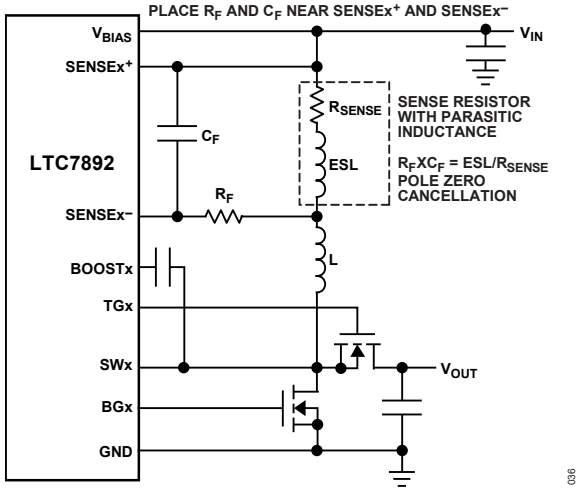



***Figure 36. Using a Resistor to Sense Current***

## Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7892 is capable of sensing the voltage drop across the inductor direct current resistance (DCR), as shown in *Figure 37*. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for low-value, high-current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

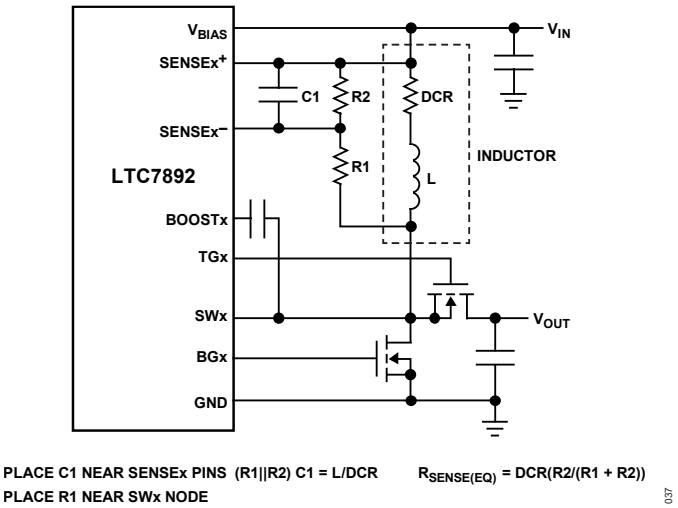



***Figure 37. Using the Inductor DCR to Sense Current ($R_{SENSE(EQUIV)}$ is the Equivalent Sensed Resistance)***

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1+R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using an inductance, capacitance, and resistance (LCR) meter, but the DCR tolerance is not always the same and varies with temperature. Refer to the manufacturer's data sheets for detailed information.

Using $I_{L(MAX)}$ and $\Delta I_L$ (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 3 as follows:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (3)$$

To ensure the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in *Table 1* (Electrical Characteristics table).

Next, determine the DCR of the inductor. When provided, use the maximum value noted by the manufacturer, typically given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for inductor temperature ($T_{L(MAX)}$) is 100°C. To scale the maximum inductor DCR ($DCR_{MAX}$) to the desired sense resistor value ($R_D$), use the divider ratio given by Equation 4, as follows:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}} \quad (4)$$

C1 is typically selected to be in the range of 0.1µF to 0.47µF. This range forces the equivalent resistance (R1||R2) to around 2kΩ, reducing the error resulting from the ≈1µA current of the $SENSE^-$ pin.

R1||R2 is scaled to the room temperature inductance, and the maximum DCR is given by Equation 5 as follows:

$$R1 \parallel R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1} \quad (5)$$

The sense resistor values are given by Equation 6 and Equation 7 as follows:

$$R1 = \frac{R1 \parallel R2}{R_D} \quad (6)$$

$$R2 = \frac{R1 \bullet R_D}{1 - R_D} \quad (7)$$

The maximum power loss (PLOSS) in R1 is related to the duty cycle and occurs in continuous mode at $V_{IN}$ = 1/2 $V_{OUT}$ given by Equation 8, as follows:

$$P_{LOSS} \text{ in } R1 = \frac{(V_{OUT} - V_{IN}) \bullet V_{IN}}{R1} \quad (8)$$

Ensure that R1 has a power rating higher than $P_{LOSS}$ in R1. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses, and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

## Setting the Operating Frequency

Selecting the operating frequency is a trade-off between efficiency and component size. High-frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses but requires larger inductance values and/or more output capacitance to maintain low output ripple voltage.

In higher voltage applications, transition losses contribute more significantly to power loss, and a proper balance between size and efficiency is achieved with a switching frequency between 300kHz and 900kHz. Lower voltage applications benefit from lower switching losses and can operate at switching frequencies up to 3MHz, if desired. The switching frequency is set using the FREQ and PLLIN/SPREAD pins, as shown in *Table 4*.

**Table 4. Setting the Switching Frequency using FREQ and PLLIN/SPREAD**

| FREQ PIN | PLLIN/SPREAD PIN | FREQUENCY |
|---|---|---|
| 0V | 0V | 370kHz |
| $INTV_{CC}$ | 0V | 2.25MHz |
| Resistor to GND | 0V | 100kHz to 3MHz |
| Any of the Above | External Clock 100kHz to 3MHz | Phase-Locked to External Clock |
| Any of the Above | $INTV_{CC}$ | Spread Spectrum $f_{OSC}$ modulated 0% to +20% |

Tying the FREQ pin to the ground selects 370kHz, whereas tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and the ground allows the frequency to be programmed anywhere between 100kHz and 3MHz. Choose a FREQ pin resistor ($R_{FREQ}$) from *Figure 38* or Equation 9, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{f_{osc}} \quad (9)$$

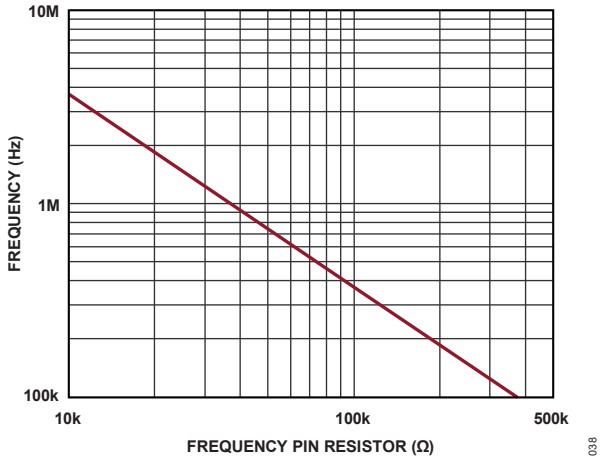



***Figure 38. Relationship between Oscillator Frequency and Resistor Value at the FREQ Pin***

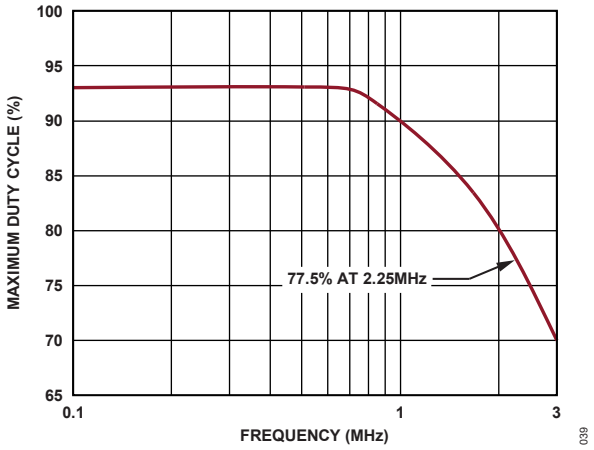



***Figure 39. Relationship between Maximum Duty Cycle and Operating Frequency***

A further constraint on the operating frequency is the maximum duty cycle of the boost converter. The maximum duty cycle ($DC_{MAX}$) is limited, as shown in *Figure 39*, and can be approximated as $DC_{MAX} = (1 - V_{IN(MIN)}/V_{OUT}) \cdot 100\%$. If the duty cycle is greater than $DC_{MAX}$, the output can lose regulation and may not maintain the constant frequency operation. An operation frequency should be selected so that the boost converter duty cycle is less than $DC_{MAX}$.

To improve EMI performance, spread spectrum mode can optionally be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When the spread spectrum mode is enabled, the switching frequency modulates within the frequency selected by the FREQ pin and is +20%. Spread spectrum mode may be used in any operating mode selected by the MODE pin (Burst Mode, PS mode, or FCM).

A PLL is also available on the LTC7892 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. After the PLL locks, the BGxx1 is synchronized to the rising edge of the external clock signal, and BGxx2 is 180° out of phase from BGxx1. See the *Phase-Locked Loop and Frequency Synchronization* section for more details.

## Selecting the Light-Load Operating Mode

The LTC7892 can be set to enter high-efficiency Burst Mode operation, constant frequency PS mode, or forced continuous conduction mode at light load currents. To select the Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select PS mode, tie the MODE pin to $INTV_{CC}$ through a 100kΩ resistor. An internal 100kΩ resistor from the MODE pin to the ground selects Burst Mode if the pin is floating. When synchronized to an external clock through the PLLIN/SPREAD pin, the LTC7892 operates in PS mode if it is selected. Otherwise, the LTC7892 operates in FCM. *Table 5* summarizes the use of the MODE pin to select the light load operating mode.

**Table 5.** ***Using the MODE Pin to Select Light Load Operating Mode***

| MODE PIN | LIGHT-LOAD OPERATING MODE | MODE WHEN SYNCHRONIZED |
|---|---|---|
| 0V or Floating | Burst Mode | FCM |
| 100kΩ to $INTV_{CC}$ | PS Mode | PS Mode |
| $INTV_{CC}$ | FCM | FCM |

The requirements of each application dictate the appropriate choice for light load operating mode. In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the top FET just before the inductor current reaches zero, preventing it from reversing and going negative. Therefore, the regulator operates in discontinuous operation. In addition, when the load current is light, the inductor current begins bursting at frequencies lower than the switching frequency and enters a low-current sleep mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light load.

In FCM, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of load. In this mode, the efficiency at light loads is considerably lower than in the Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In FCM, the output ripple is independent of the load current.

In PS mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At very light loads, the PWM comparator may remain tripped for several cycles and force the bottom FET to remain off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. PS mode provides higher light load efficiency than FCM, but not nearly as high as Burst Mode operation. Consequently, PS mode represents a compromise between light load efficiency, output ripple, and EMI.

In some applications, it can be desirable to change the light load operating mode based on the conditions present in the system. For example, if a system is inactive, one might select high-efficiency Burst Mode operation by keeping the MODE pin set to 0V. When the system wakes, the user can send an external clock to PLLIN/SPREAD, or tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode. These types of changes can allow an individual application to benefit from the advantages of each light load operating mode.

## Dead Time Control (DTCA and DTCB Pins)

The dead time delays of the LTC7892 can be adjusted from 7ns to 60ns through configuration of the DTCA and DTCB pins. Refer to the timing diagrams on *Figure 40* and *Figure 41* show the TGx minus SWx and BGx waveforms for each DTCx pin setting. In the *DTCx Pin Tied to Ground (Adaptive Dead Time Control)* and *DTCx Pin connected with a resistor to GND* sections, TGx represents the voltage sensed at the top FET gate (the threshold for the TGx falling is sensed at the TGUPx pin), and BGx represents the voltage sensed at the bottom FET (the thresholds for the BGx rising and falling are sensed at the BGDNx and BGUPx pins respectively). The DTCA pin programs the dead time associated with the bottom FET turning off and the top FET turning on (SWx transitioning low to high). The DTCB pin programs the dead time associated with top FET turning off and the bottom FET turning on (SWx transitioning high to low).

## DTCx Pin Tied to Ground (Adaptive Dead Time Control)

Tying the DTCA and DTCB pins to the GND program adaptive dead time control. In adaptive control (see *Figure 40*), the dead time is measured between one FET turning off and the other FET turning on. Tying the DTCA pin to GND fixes the delay between BGx falling and TGx minus SWx rising to approximately 15ns. Tying the DTCB pin to GND fixes the delay between TGx minus SWx falling and BGx rising to approximately 15ns.

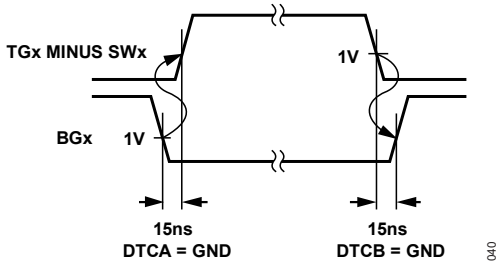



***Figure 40. DTC Pin tied to GND – Adaptive Dead Time Control***

## DTCx Pin connected with a resistor to GND

Connecting a resistor between the DTCx pin and GND programs an open-loop dead time delay from 7ns to 60ns between the TGx minus SWx and BGx edges (see *Figure 41*). A resistor tied to the DTCA pin programs an open loop delay between BGx falling and TGx minus SWx rising. A resistor tied to the DTCB pin and GND programs an open loop delay between TGx minus SWx falling and BGx rising. *Figure 42* shows the relationship between the DTCx pin resistor value and the programmed delay between TGx minus SWx and BGx edges. This resistor must not be less than 10kΩ or more than 200kΩ.

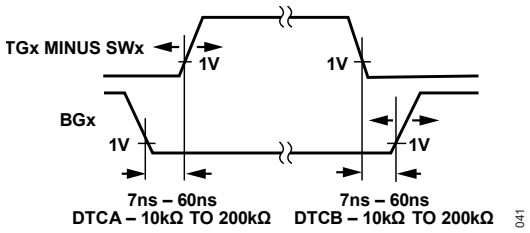



***Figure 41. DTCx Pin with Resistor to GND – Adjustable Dead Time Control***

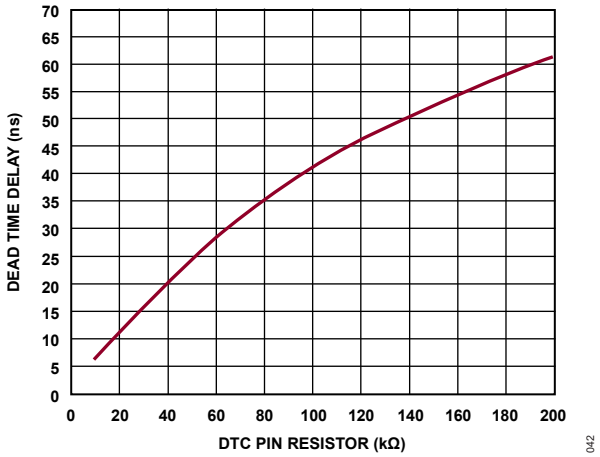



***Figure 42. Relationship between Dead Time Delay and Resistor Value at the DTCx Pin***

If one of the DTCx pins is programmed with a resistor, the other DTCx pin must be programmed with a resistor for proper dead time control operation. Unexpected dead time delays can result if one DTCx pin is programmed with a resistor while the other DTCx pin is tied to GND. The DTCx pins should only be connected to GND or a resistor tied to GND.

## Power FET Selection

Two external power FETs must be selected for each controller in the LTC7892: one N-channel FET for the bottom (main) switch and one N-channel FET for the top (synchronous) switch. The peak-to-peak gate drive levels are set by the INTVCC regulation point (4V to 5.5V). Most GaN FETs can be driven comfortably within this INTVCC regulation window. If using silicon MOSFETs, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the $BVD_{SS}$ specification for the FETs as well.

Selection criteria for the power FETs include the on resistance ($R_{DS(ON)}$), Miller capacitance ($C_{MILLER}$), input voltage, and maximum output current. $C_{MILLER}$, can be approximated from the gate charge curve typically provided in the datasheet of the FET manufacturer. $C_{MILLER}$ is equal to the increase in gate charge along the horizontal axis, while the curve is approximately flat, divided by the specified change in the voltage difference between the drain and source terminals of the FET ($V_{DS}$). This result is then multiplied by the ratio of the application applied $V_{DS}$ to the gate charge curve specified $V_{DS}$. When the IC is operating in continuous mode, the duty cycles for the top and bottom FETs are given by Equation 10 and Equation 11, as follows:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{10}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}} \tag{11}$$

The FET power dissipation at maximum output current is given by Equation 12 and Equation 13, as follows:

$$P_{MAIN} = \frac{(V_{OUT}-V_{IN})V_{OUT}}{V_{IN^2}}\left(I_{OUT(MAX)}\right)^2 \bullet (1+\delta)R_{DS(ON)} + \left(\frac{V_{OUT^3}}{V_{IN}}\right)\left(\frac{I_{OUT(MAX)}}{2}\right) \bullet (R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{V_{INTVCC}-V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f) \tag{12}$$

$$P_{SYNC} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} \tag{13}$$

where:

$P_{MAIN}$ is the power dissipation from the main switch
$\delta$ is the temperature dependency of $R_{DS(ON)}$ ($\delta \approx 0.005/°C$).
$R_{DR}$ is the effective driver resistance at the FET's Miller threshold voltage ($R_{DR} \approx 2\Omega$).
$V_{INTVCC}$ is the $INTV_{CC}$ voltage.
$V_{THMIN}$ is the typical FET minimum threshold voltage.
$P_{SYNC}$ is the power dissipation from the synchronous switch.

Both FETs have $I^2R$ losses ($I^2R$ is the power loss equation of the FETs when on in steady state), whereas the main N-channel equations include an additional term for transition losses, which are highest at low input voltages. For high input voltages, the high current efficiency generally improves with larger FETs. However, for low input voltages, the transition losses rapidly increase to the point that using a higher $R_{DS(ON)}$ device with lower $C_{MILLER}$ provides higher efficiency. The synchronous FET losses are greatest at high input voltages when the bottom switch duty factor is low.

## $C_{IN}$ and $C_{OUT}$ Selection

The input ripple current in a boost converter is relatively low (compared to the output ripple current) because the input current is continuous. The boost converter input capacitor ($C_{IN}$) voltage rating should exceed the maximum input voltage. Although ceramic capacitors are tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of $C_{IN}$ is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High-output current applications that also experience high-duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

The selection of the output capacitance ($C_{OUT}$) is driven by the output voltage ripple ($V_{RIPPLE}$) requirement. The output current in a boost converter is discontinuous. Therefore, both the effects of ESR and the bulk capacitance must be considered when choosing $C_{OUT}$. $V_{RIPPLE}$ due to charging and discharging the bulk capacitance of $C_{OUT}$ is given by Equation 14, as follows:

$$V_{RIPPLE} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f} \quad (14)$$

The ripple due to the voltage drop across the ESR ($\Delta V_{ESR}$) for $C_{OUT}$ is given by Equation 12, as follows:

$$\Delta V_{ESR} = \left(I_{L(MAX)} + \frac{1}{2}\Delta I_L\right) \bullet ESR \quad (15)$$

Where:

$\Delta I_L$ is the ripple current in the inductor.

$I_{L(MAX)}$ is the maximum average inductor current.

$I_{OUT(MAX)}$ is the maximum average output current.

f is the operating frequency.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Low ESR and high ripple current-rated capacitors such as OS-CON and POSCAP are available.

## Single Output 2-Phase Operation

For high-power applications, the two channels can be operated in a 2-phase single output configuration. With 2-phase operation, the two channels are operated 180° out-of-phase which effectively interleaves the output current pulses. The interleaved current pulses double the maximum output current while reducing the output capacitor ripple current. The reduction in output capacitor ripple current lowers the capacitance and ESR requirements of the high-frequency output capacitor for a given output ripple voltage requirement.

The ripple current requirements for the output capacitor shown in Equation 14 can be reduced in a 2-phase configuration, as shown in *Figure 43*. *Figure 43* illustrates the normalized output capacitor ripple current as a function of the duty cycle in a 2-phase configuration compared to a single-phase configuration. To choose a ripple current rating for the output capacitor in a 2-phase configuration, use the following steps:

1. Calculate the duty cycle range based on the output voltage and range of input voltage.
2. As shown in *Figure 43*, choose the worst-case high normalized ripple current as a percentage of the maximum load current.

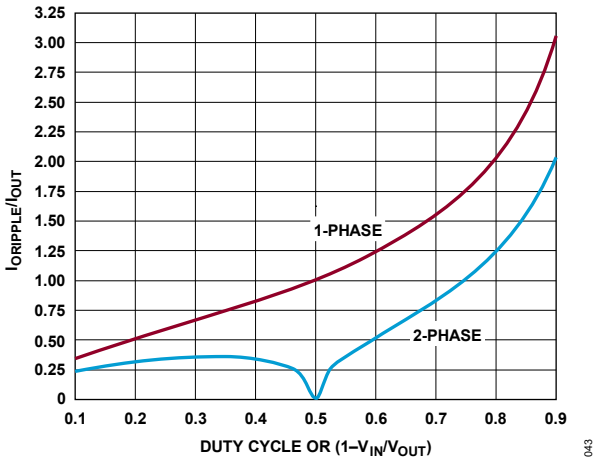



***Figure 43. Normalized Output Capacitor Ripple Current (RMS) for a Boost Converter***

To configure the LTC7892 for 2-phase operation, tie $V_{FB2}$ to $INTV_{CC}$, ITH2 to ground, SS2 to ground, PGOOD2 to ground (or left floating), and RUN2 to RUN1.

The RUN1, $V_{FB1}$, ITH1, and SS1 pins are then used to control both channels, but each channel uses its own ICMP and IR comparators to monitor their respective inductor currents.

*Figure 44* shows the configuration for a single output 2-phase operation and *Figure 50* shows a typical application configured for a single output 2-phase operation.

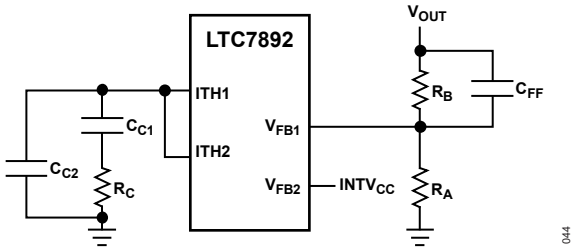



***Figure 44. Configuration for Single Output 2-Phase Operation***

## Setting the Output Voltage

The LTC7892 output voltages are each set by an external feedback resistor divider carefully placed across the output, as shown in *Figure 45* and *Figure 46*. The regulated output voltage is determined by Equation 16, as follows:

$$V_{OUT} = 1.2V(1 + \frac{R_B}{R_A}) \quad (16)$$

Place the $R_A$ and $R_B$ resistors close to the $V_{FBx}$ pin to minimize printed circuit board (PCB) trace length and noise on the sensitive $V_{FBx}$ node. Take care to route the $V_{FBx}$ trace away from noise sources, such as the inductor or the SWx trace. To improve frequency response, a feedforward capacitor ($C_{FF}$) can be used.

Channel 1 on the LTC7892 can be programmed to a fixed 28V or 24V output through control of the VPRG1 pin. *Figure 46* shows how the $V_{FB1}$ pin is used to sense the output voltage in fixed output mode. Tying VPRG1 to $INTV_{CC}$ or GND programs $V_{OUT1}$ to 28V or 24V, respectively. Floating VPRG1 sets $V_{OUT1}$ to adjustable output mode using external resistors.

The system must be designed so that the $V_{FB2}$ pin voltage is less than 3V. Otherwise, the LTC7892 will enter a 2-phase operation (See *Single Output 2-Phase Operation* section for more details). Applications that are most likely to cause this condition are applications where channel 2 is operated in dropout mode with high $V_{IN}$ voltages. For example, $R_A$ and $R_B$ for channel-2 are chosen so that $V_{OUT2}$ = 8V ($R_B/R_A$ = 5.67). When $V_{IN}$ is less than 8V, the converter will be regulating, and $V_{FB2}$ will be 1.2V. When $V_{IN}$ is greater than 8V, the converter will be in dropout, and $V_{FB2}$ will be $V_{OUT2}/5.67$. If $V_{IN}$ is greater than 17V, $V_{FB2}$ will be greater than 3V, and the LTC7892 will enter a 2-phase operation, and $V_{OUT2}$ will now be controlled by Channel 1.

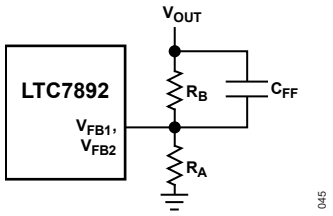



***Figure 45. Setting Adjustable Output Voltage***

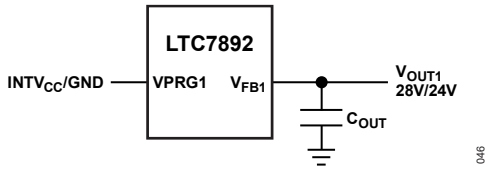



***Figure 46. Setting Fixed 28V or 24V Output Voltage***

## RUNx Pins and Undervoltage Lockout

The two channels of the LTC7892 are enabled using the RUN1 and RUN2 pins. The RUNx pin has a rising threshold of 1.2V with 120mV of hysteresis. Pulling a RUNx pin less than 1.08V shuts down the main control loop and resets the softstart for that channel. Pulling both RUN1 and RUN2 pins less than 0.7V disables the controllers and most internal circuits, including the $INTV_{CC}$ LDO regulators. In this state, the LTC7892 draws only ≈1µA of current from $V_{BIAS}$.

The RUNx pins are high impedance and must be externally pulled up, or pulled down, or driven directly by logic. The RUNx pin can tolerate up to 100V (the absolute maximum). Therefore, these pins can be conveniently tied to $V_{IN}$ in applications where the controller is enabled continuously and never shut down. Do not float the RUNx pins.

The RUNx pins can also be configured as precise UVLOs on the input supply with a resistor divider from $V_{IN}$ to ground, as shown in *Figure 47.*

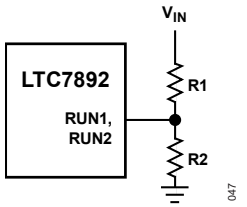



***Figure 47. Using the Run Pins as a UVLO***

The $V_{IN}$ UVLO thresholds can be computed using Equation 17 and Equation 18, as follows:

$$\text{UVLO RISING} = 1.2\text{V}\left(1 + \frac{\text{R1}}{\text{R2}}\right) \quad (17)$$

$$\text{ULVO FALLING} = 1.08\text{V}\left(1 + \frac{\text{R1}}{\text{R2}}\right) \quad (18)$$

The current that flows through the R1 and R2 divider directly adds to the shutdown, sleep, and active current of the LTC7892. Take care to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the MΩ range can be required to keep the impact on quiescent shutdown and sleep currents low.

## Soft Start (SSx Pins)

The start-up of each $V_{OUTx}$ is controlled by the voltage on the SSx pin (SS1 for channel 1, SS2 for channel 2). When the voltage on the SSx pin is less than the internal 1.2V reference, the LTC7892 regulates the $V_{FBx}$ pin voltage to the voltage on the SSx pin instead of the internal reference.

Soft start is enabled by simply connecting a capacitor from the SSx pin to GND. An internal 12µA current source charges the capacitor, providing a linear ramping voltage at the SSx pin. The LTC7892 regulates its feedback voltage (and hence $V_{OUTx}$) according to the voltage on the SSx pin, allowing $V_{OUTx}$ to rise smoothly from 0V to its final regulated value. For a desired soft-start time ($t_{SS}$), select a soft-start capacitor ($C_{SS}$) = $t_{SS}$ • 10nF/msec.

## $INTV_{CC}$ Regulators (OPTI-DRIVE)

The LTC7892 features two separate internal LDO linear regulators that supply power at the $INTV_{CC}$ pin from either the $V_{BIAS}$ pin or the $EXTV_{CC}$ pin, depending on the $EXTV_{CC}$ pin voltage and connections to the DRVSET and DRVUV pins. The $DRV_{CC}$ pin is the supply pin for the FET gate drivers and must be connected to the $INTV_{CC}$ pin. The $V_{BIAS}$ LDO regulator and the $EXTV_{CC}$ LDO regulator regulate $INTV_{CC}$ between 4V and 5.5V, depending on how the DRVSET pin is set. Each LDO regulator can provide a peak current of at least 100mA.

Bypass the $INTV_{CC}$ pin with a minimum of 4.7µF ceramic capacitor placed as close as possible to the pin. It is recommended to place an additional 1µF ceramic capacitor next to the $DRV_{CC}$ pin and GND pins to supply the high-frequency transient currents required by the FET gate drivers.

The DRVSET pin programs the $INTV_{CC}$ supply voltage, and the DRVUV pin selects the different $INTV_{CC}$ UVLO and $EXTV_{CC}$ switchover threshold voltages. *Table 6* summarizes the different DRVSET pin configurations along with the voltage settings that go with each configuration. *Table 7* summarizes the different DRVUV pin configurations and voltage settings. Tying the DRVSET pin to $INTV_{CC}$ programs $INTV_{CC}$ to 5.5V. Tying the DRVSET pin to GND programs $INTV_{CC}$ to 5.0V. Place a 43kΩ to 100kΩ resistor between DRVSET and GND to program the $INTV_{CC}$ voltage between 4V to 5.5V, as shown in *Figure 48*.

**Table 6. DRVSET Pin Configurations and Voltage Settings**

| DRVSET Pin | $INTV_{CC}$ Voltage (V) |
|---|---|
| GND | 5.0V |
| $INTV_{CC}$ | 5.5V |
| Resistor to GND 43kΩ to 100kΩ | 4V to 5.5V |

**Table 7. DRVUV Pin Configurations and Voltage Settings**

| DRVUV Pin | $INTV_{CC}$ UVLO Rising and Falling Thersholds (V) | $EXTV_{CC}$ Switchover Rising and Falling Thresholds (V) |
|---|---|---|
| GND | 3.8V and 3.6V | 4.76V and 4.54V |
| Floating | 4.4V and 4.18V | 5.95V and 5.56V |
| $INTV_{CC}$ | 5V and 4.75V | 5.95V and 5.56V |

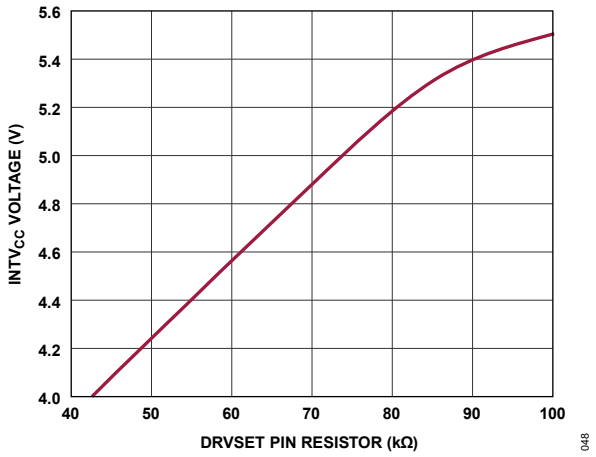



***Figure 48. Relationship Between $INTV_{CC}$ Voltage and Resistor Value at the DRVSET Pin***

High input voltage applications in which large FETs are being driven at high frequencies can exceed the maximum junction temperature rating for the LTC7892. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the $V_{BIAS}$ LDO regulator or the $EXTV_{CC}$ LDO regulator. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.76V or 5.95V, as determined by the DRVUV pin), the $V_{BIAS}$ LDO regulator is enabled.

Power dissipation for the IC, in this case is equal to $V_{BIAS}$ • $INTV_{CC}$ current ($I_{INTVCC}$). The gate charge current is dependent on operating frequency, as discussed in the *Efficiency Considerations* section. To estimate the junction temperature, use the equation detailed in *Table 2*. For example, the LTC7892 $INTV_{CC}$ current is limited to less than 46mA from a 36V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature given by Equation 19.

$$T_J = 70°C + (46mA)(36V)(33°C/W) = 125°C \quad (19)$$

To prevent exceeding the maximum junction temperature, check the input supply current while operating in continuous conduction mode (MODE = $INTV_{CC}$) at maximum $V_{BIAS}$.

When the voltage applied to $EXTV_{CC}$ rises above its rising switchover threshold, the $V_{BIAS}$ LDO regulator turns off, and the $EXTV_{CC}$ LDO regulator is enabled. The $EXTV_{CC}$ LDO regulator remains on as long as the voltage applied to $EXTV_{CC}$ remains above its falling switchover threshold. The $EXTV_{CC}$ LDO regulator attempts to regulate the $INTV_{CC}$ voltage to the voltage as programmed by the DRVSET pin. Therefore, while $EXTV_{CC}$ is less than the programmed voltage set by the DRVSET pin, the LDO regulator is in dropout, and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage (up to an absolute maximum of 30V), $INTV_{CC}$ is regulated to the programmed voltage. If more current is required through the $EXTV_{CC}$ LDO regulator than is specified, add an external Schottky diode between the $EXTV_{CC}$ and $INTV_{CC}$ pins. In this case, do not apply more than 6V to the $EXTV_{CC}$ pin.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from an external supply. This is accomplished by tying the $EXTV_{CC}$ pin directly to an external supply that is greater than the $INTV_{CC}$ regulation point.

Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in Equation 15 from 125°C to the results as given by Equation 20, as follows:

$$T_J = 70°C + (46mA)(8.5V)(33°C/W) = 83°C \quad (20)$$

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This connection causes the internal $V_{BIAS}$ LDO regulator to power $INTV_{CC}$, resulting in an efficiency penalty of up to 10% or more at high $V_{BIAS}$ voltages.
2. $EXTV_{CC}$ connected directly to $V_{IN}$. This connection is the normal connection for an application with $V_{IN}$ in the 5V to 30V range and provides significant thermal gains if $V_{BIAS}$ is tied to $V_{OUT}$.
3. $EXTV_{CC}$ connected directly to an external supply. If an external supply is available in the 5V to 30V range, it can be used to power $EXTV_{CC}$, provided that it is compatible with the FET gate drive requirements. This supply may be higher or lower than $V_{BIAS}$; however, a lower $EXTV_{CC}$ voltage results in higher efficiency.

## Topside FET Driver Supply ($C_B$)

External bootstrap capacitors $C_B$ connected to the BOOSTx pins supply the gate drive voltages for the topside FETs. Capacitor $C_B$ in *Figure 34* is charged through an internal switch from $DRV_{CC}$ when the SWx pin is low, and the bottom FET is turned on. The on resistance of the internal switch is approximately 7Ω.

When the topside FET is to be turned on, the driver places the $C_B$ voltage across the gate-source of the desired FET, which enhances the FET and turns on the topside switch. The switch node voltage, SWx, rises to $V_{OUT}$, and the BOOSTx pin follows. With the topside FET on, the boost voltage is more than the output voltage: $V_{BOOST} = V_{OUT} + V_{INTVCC}$. The value of the boost capacitor $C_B$ needs to be 100 times that of the total input capacitance of the topside FETs. For a typical application, a value of $C_B = 0.1\mu F$ is generally sufficient.

## Minimum On-Time Considerations

The minimum on-time ($t_{ON(MIN)}$) is the shortest time duration that the LTC7892 is capable of turning on the bottom FET. $T_{ON(MIN)}$ is determined by internal timing delays and the gate charge required to turn on the bottom FET. Low-duty cycle applications can approach this minimum on-time limit. Ensure the results in Equation 21, as follows:

$$t_{ON(MIN)} < \frac{V_{OUT} - V_{IN}}{V_{OUT} \bullet f} \quad (21)$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC7892 begins to skip cycles. The output voltage continues to regulate, but the ripple voltage and current will increase. The minimum on-time for the LTC7892 is approximately 100ns. If $V_{IN}$ increases, thereby further decreasing the duty cycle, more cycles are skipped, and the LTC7892 can turn on the top FET continuously. If the bottom FET is not turned on frequently enough to recharge the bootstrap capacitor, the top FET will not fully enhance, or it can be completely off when the LTC7892 turns on the top FET. Thus, the LTC7892 cannot achieve 100% top FET on operation.

## Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating (such as a short from $INTV_{CC}$ to ground), internal overtemperature shutdown circuitry will shut down the LTC7892. When the internal die temperature exceeds 180°C, the $INTV_{CC}$ LDO regulator and the gate drivers are disabled. When the die cools to 160°C, the LTC7892 enables the $INTV_{CC}$ LDO regulator and resumes operation, beginning with a soft-start startup. Avoid long-term overstress ($T_J$ > 125°C) because it can degrade the performance or shorten the life of the device.

## Phase-Locked Loop and Frequency Synchronization

The LTC7892 has an internal PLL that allows the turn-on of the bottom FET of channel 1 to be synchronized to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin. The turn-on of channel 2 bottom FET is 180° out of phase with the external clock.

Rapid phase-locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. Before synchronization, the PLL is prebiased to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase-lock and synchronization. Although it is not required, placing the free-running frequency be near the external clock frequency prevents the oscillator from passing through a large range of frequencies as the PLL locks.

When synchronized to an external clock, the LTC7892 operates in pulse-skipping mode if it is selected by the MODE pin, or in forced continuous mode otherwise. The LTC7892 is guaranteed to synchronize to an external clock applied to the PLLIN/SPREAD pin that swings up to at least 2.2V and down to 0.5V or less. Note that the LTC7892 can only be synchronized to an external clock frequency within the range of 100kHz to 3MHz.

## Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Analyzing individual losses is useful for determining what limits the efficiency and which change would produce the most improvement. Percent efficiency can be expressed by Equation 22 as follows:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...) \quad (22)$$

where L1, L2, L3, and so on, are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7892 circuits: IC $V_{BIAS}$ current, $INTV_{CC}$ regulator current, $I^2R$ losses, and bottom-side FET transition losses.

1. The $V_{BIAS}$ current is the DC supply current given in *Table 1* (Electrical Characteristics table), which excludes FET drivers and control currents. Other than at very light loads in Burst Mode operation, $V_{BIAS}$ current typically results in a small (<0.1%) loss.

2. The $INTV_{CC}$ current is the sum of the FET driver and control currents. The FET driver current results from switching the gate capacitance of the power FETs. Each time a FET gate is switched from low to high to low again, a packet of charge (dQ) moves from $INTV_{CC}$ to GND. The resulting dQ/time duration (dt) is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, gate charge current ($I_{GATECHG}$) = frequency (f) x ($Q_T$ + $Q_B$), where $Q_T$ and $Q_B$ are the gate charges of the top and bottom FETs.

3. $I^2R$ losses are predicted from the DC resistances of the input fuse (if used), FET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode, the average output current flows through L and $R_{SENSE}$, but is chopped between the top and bottom FETs. If the two FETs have approximately the same $R_{DS(ON)}$, the resistance of one FET can simply be summed with the resistances of L, $R_{SENSE}$, and ESR to obtain the $I^2R$ losses.

4. Transition losses apply only to the bottom FETs and become significant only when operating at higher output voltages (typically 20V or greater) or at high frequency (MHz range). Transition losses can be estimated using Equation 23, as follows:

$$\text{TRANSITION LOSS} = (1.7)\frac{V_{OUT}^3}{V_{IN}} I_{L(MAX)} \bullet C_{MILLER} \bullet f \quad (23)$$

where:

$I_{L(MAX)}$ is the maximum average inductor current.
$C_{MILLER}$ is the Miller capacitance.
f is the operating frequency.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system-level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that $C_{IN}$ has adequate charge storage and very low ESR at the switching frequency. A 25W supply typically requires a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses, including inductor core losses, generally account for less than 2% of the total additional loss.

## Checking Transient Response

To check the regulator loop response, look at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, $V_{OUTx}$ shifts by an amount equal to $\Delta I_{LOAD}$ • (ESR), where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$, generating the feedback error signal that forces the regulator to adapt to the current change and return $V_{OUTx}$ to its steady-state value. During this recovery time $V_{OUTx}$ can be monitored for excessive overshooting or ringing, which would indicate a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITHx pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time, and settling at this test point truly reflect the closed-loop response. Assuming a predominantly second-order system, the phase margin and/or damping factor can be estimated using the percentage of overshoot seen at the ITHx pin. The bandwidth can also be estimated by examining the rise time at the ITHx pin. The ITHx external components shown in the *Typical Applications* section provide an adequate starting point for most applications.

The ITHx series compensation resistor ($R_C$) and capacitor ($C_C$) filter set the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their initial values) to optimize transient response once the final PCB layout is done and the specific output capacitor type and value are determined. The output capacitors must be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current, with a rise time of 1µs to 10µs, produces output voltage and ITHx pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power FET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop. Therefore, this signal cannot be used to determine the phase margin. For this reason, it is better to look at the ITHx pin signal, which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop increases by increasing $R_C$, and the bandwidth of the loop will increase by decreasing $C_C$. If $R_C$ increases by the same factor that $C_C$ is decreased, the zero frequency is kept the same, keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with $C_{OUT}$, causing a rapid drop in $V_{OUTx}$. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of $C_{LOAD}$ to $C_{OUT}$ is greater than 1:50, the switch rise time must be controlled so that the load rise time is limited to approximately $C_{LOAD}$ • 25µs/µF. Therefore, a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

## Design Example

As a design example, assume the nominal input voltage ($V_{IN(NOMINAL)}$) = 12V, $V_{IN(MAX)}$ = 20V, $V_{OUTx}$ = 24V, $I_{OUT}$ = 4A, and f = 1MHz.

Use the following steps to design an application circuit:

1. Set the operating frequency. The frequency is not one of the internal preset values, so a resistor from the FREQ pin to GND is required, with a value given by Equation 24, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{1\text{MHz}} = 37\text{k}\Omega \quad (24)$$

2. Determine the inductor value. Initially, select a value based on an inductor ripple current of 30%. The inductor value can then be calculated by Equation 25, as follows:

$$L = \frac{V_{IN}}{f \bullet \Delta I_L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right) = 2.4\mu\text{H} \quad (25)$$

   The highest value of the ripple current occurs when $V_{IN}$ = (1/2) • $V_{OUT}$. In this case, the ripple at $V_{IN}$ = 12V is 31%.

3. Verify that the minimum on-time of 100ns is not violated. The minimum on-time occurs at $V_{IN(MAX)}$, as shown in Equation 26:

$$t_{ON(MIN)} < \frac{V_{OUT} - V_{IN(MAX)}}{V_{OUT} \bullet f} = \frac{4\text{V}}{24\text{V} \bullet 1\text{MHz}} = 166\text{ns} \quad (26)$$

   This time is sufficient to satisfy the minimum on-time requirement. If the minimum on time is violated, the LTC7892 skips pulses at high input voltage, resulting in lower frequency operation and higher inductor current ripple than desired. If undesirable, this behavior can be avoided by decreasing the frequency (with the inductor value accordingly adjusted) to avoid operation near the minimum on-time.

4. Select the $R_{SENSE}$ resistor value. The peak inductor current is the maximum DC output current plus half the inductor ripple current, or 8A x (1 + 0.31 / 2) = 9.24A in this case. The $R_{SENSE}$ resistor value is then calculated based on the minimum value for the maximum current sense threshold (45mV for ILIM = float) given by Equation 27, as follows:

$$R_{SENSE} \leq \frac{45mV}{9.24A} \approx 4m\Omega \quad (27)$$

   To allow for additional margin, a lower value $R_{SENSE}$ can be used. However, be sure that the inductor saturation current has a sufficient margin above $V_{SENSE(MAX)}/ R_{SENSE}$, where the maximum value of 55mV is used for $V_{SENSE(MAX)}$.

5. Select the feedback resistors. Choosing 1% resistors: $R_A$ = 5kΩ and $R_B$ = 95.3kΩ yields an output voltage of 24.07V. The resistance values selected give a feedback divider current of 24.07V / (5kΩ + 95.3kΩ) = 240µA.

6. Select the FETs. The best way to evaluate FET performance in a particular application is to build and test the circuit on the bench, facilitated by an LTC7892 evaluation board. However, an educated guess about the application is helpful to initially select FETs. Because this is a high current, low voltage application, $I^2R$ losses will likely dominate over transition losses for the bottom FET. Therefore, choose a FET with a lower $R_{DS(ON)}$ as opposed to a lower gate charge to minimize the combined loss terms. The top FET does not experience transition losses, and its power loss is generally dominated by $I^2R$ losses. For this reason, the top FET is typically chosen to have a lower $R_{DS(ON)}$ and subsequently, higher gate charge than the bottom FET.

7. When using silicon MOSFETs, be sure to select logic level threshold MOSFETs because the gate drive voltage is limited to 5.5V ($INTV_{CC}$).

8. Select the output capacitor. $C_{OUT}$ is chosen to filter the square current in the output. The maximum output current peak is given by Equation 28, as follows:

$$I_{OUT(PEAK)} = I_{OUT(MAX)} \bullet \left(1 + \frac{RIPPLE\%}{2}\right) = 4 \bullet \left(1 + \frac{31\%}{2}\right) = 4.62A \quad (28)$$

   A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 23.1mV (assuming ESR dominates the ripple).

9. Determine the bias supply components. If another supply is available that is above the $INTV_{CC}$ regulation voltage and below $V_{IN}$, for example, an 8.5V supply, connect that supply to $EXTV_{CC}$ to improve the efficiency. For a 6.7ms soft start, select a 0.1µF capacitor for the SSx pin. As a first-pass estimate for the bias components, select the $INTV_{CC}$ capacitance ($C_{INTVCC}$) = 4.7µF and boost supply capacitor ($C_B$)= 0.1µF.

10. Determine and set application-specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread spectrum, or phase-locked frequency is desired. The RUNx pin can be used to control the minimum input voltage for regulator operation or can be tied to $V_{IN}$ for always-on operation. Use ITHx compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary. Program the DTCA and DTCB pins for the desired dead time delays.

## PCB Board Layout Checklist

*Figure 49* shows the current waveforms present in the various branches of the synchronous boost converters operating in the continuous mode.

When laying out the printed circuit board, use the following checklist should be used to ensure proper operation of the IC.

Place the top and bottom N-channel FETs (MTOPx and MBOTx) and the high frequency (ceramic) $C_{OUTx}$ capacitors as shown in *Typical Applications* section within 1cm of each other.

Route the TGUPx and TGDNx traces together and connect them as close as possible to the top FET gate. Route the BGDNx and BGUPx traces together and connect them as close as possible to the bottom FET gate. If using gate resistors, connect the resistor connections to the FET gate as close as possible to the FET. Connecting TGUPx and TGDNx further away from the top FET gate, as well as connecting BGUPx and BGDNx further away from the bottom FET gate, can adversely affect the operation of the LTC7892's adaptive dead time control.

The combined IC GND pin and the GND return of $C_{INTVCC}$ must return to the combined $C_{OUT}$ negative terminals. The path formed by the bottom N-channel FET and the $C_{IN}$ capacitor must have short leads and PCB trace lengths. Connect the output capacitor's negative terminals as close as possible to the negative terminals of the input capacitor by placing the capacitors next to each other and away from the loop.

Connect the LTC7892 $V_{FBx}$ pin resistive dividers to the positive terminals of $C_{OUT}$ and the signal GND. Place the divider close to the $V_{FBx}$ pin to minimize noise coupling into the sensitive $V_{FBx}$ node. The feedback resistor connections must not be along the high-current input feeds from the input capacitors.

Route the $SENSEx^-$ and $SENSEx^+$ leads together with minimum PCB trace spacing. Route these traces away from the high-frequency switching odes on an inner layer, if possible. The filter capacitor between $SENSEx^+$ and $SENSEx^-$ must be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.

Connect the $INTV_{CC}$ decoupling capacitor close to the IC, between the $INTV_{CC}$ and the power GND pin. This capacitor carries the current peaks of the FET drivers. Place an additional 1µF ceramic capacitor next to the $DRV_{CC}$ and GND pins to help improve noise performance.

Keep the switching nodes (SW1 and SW2), top gate nodes (TGUP1/TGDN1 and TGUP2/TGDN2), and boost nodes (BOOST1 and BOOST2) away from sensitive small-signal nodes, especially from the voltage and current sensing feedback pins of the other channel. All of these nodes have large and fast-moving signals. Therefore, keep these nodes on the output side of the LTC7892 and ensure they occupy the minimum PCB trace area.

Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PCB as the input and output capacitors, with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider, and the GND pin of the IC.

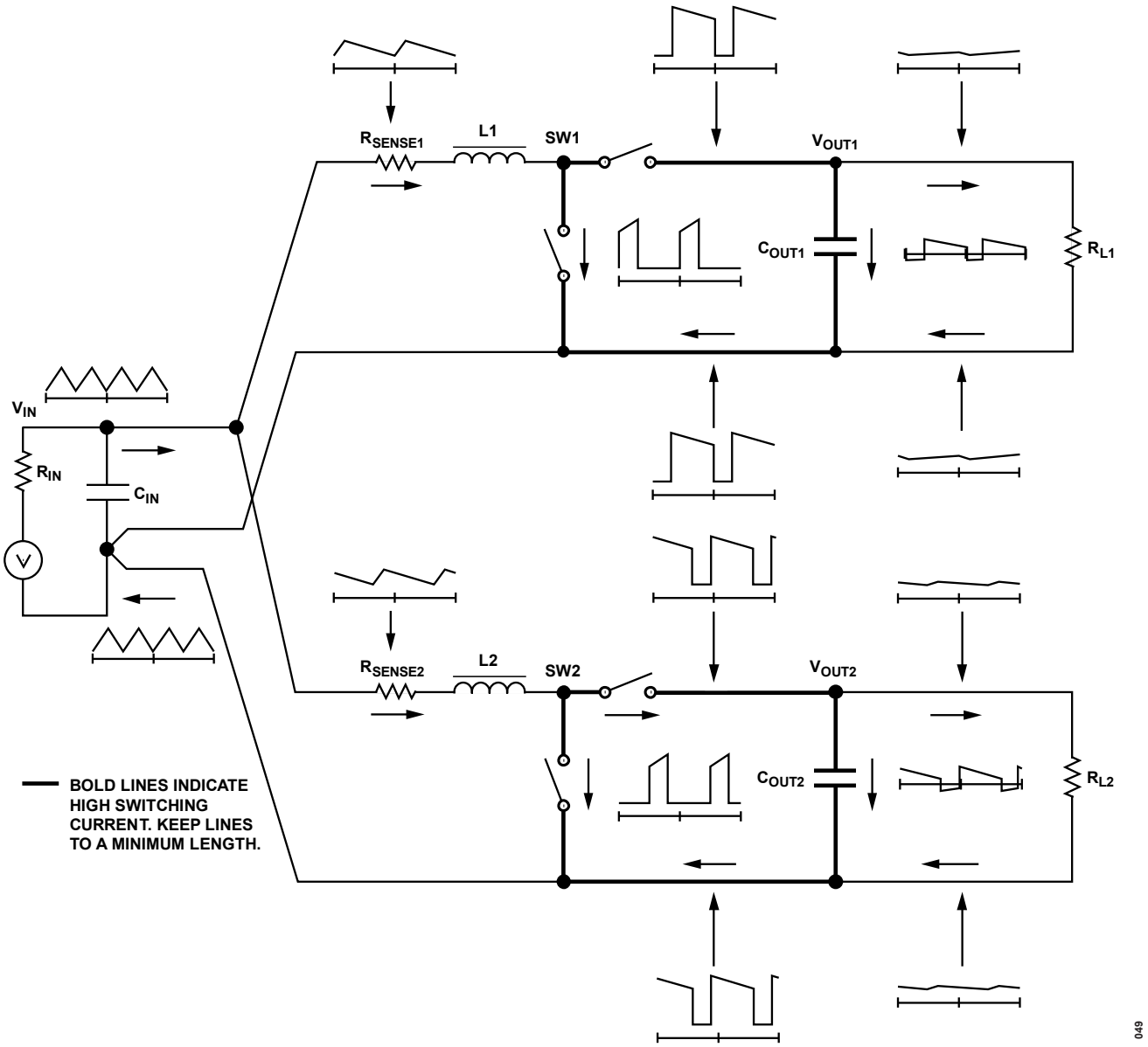



*Figure 49. Branch Current Waveforms*

## PCB Layout Debugging

Start with one channel on at a time. Use a DC to 50 MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (the SWx pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation is maintained over the input voltage range down to dropout and until the output load drops to less than the low current operation threshold, typically 25% of the maximum designed current level in Burst Mode operation.

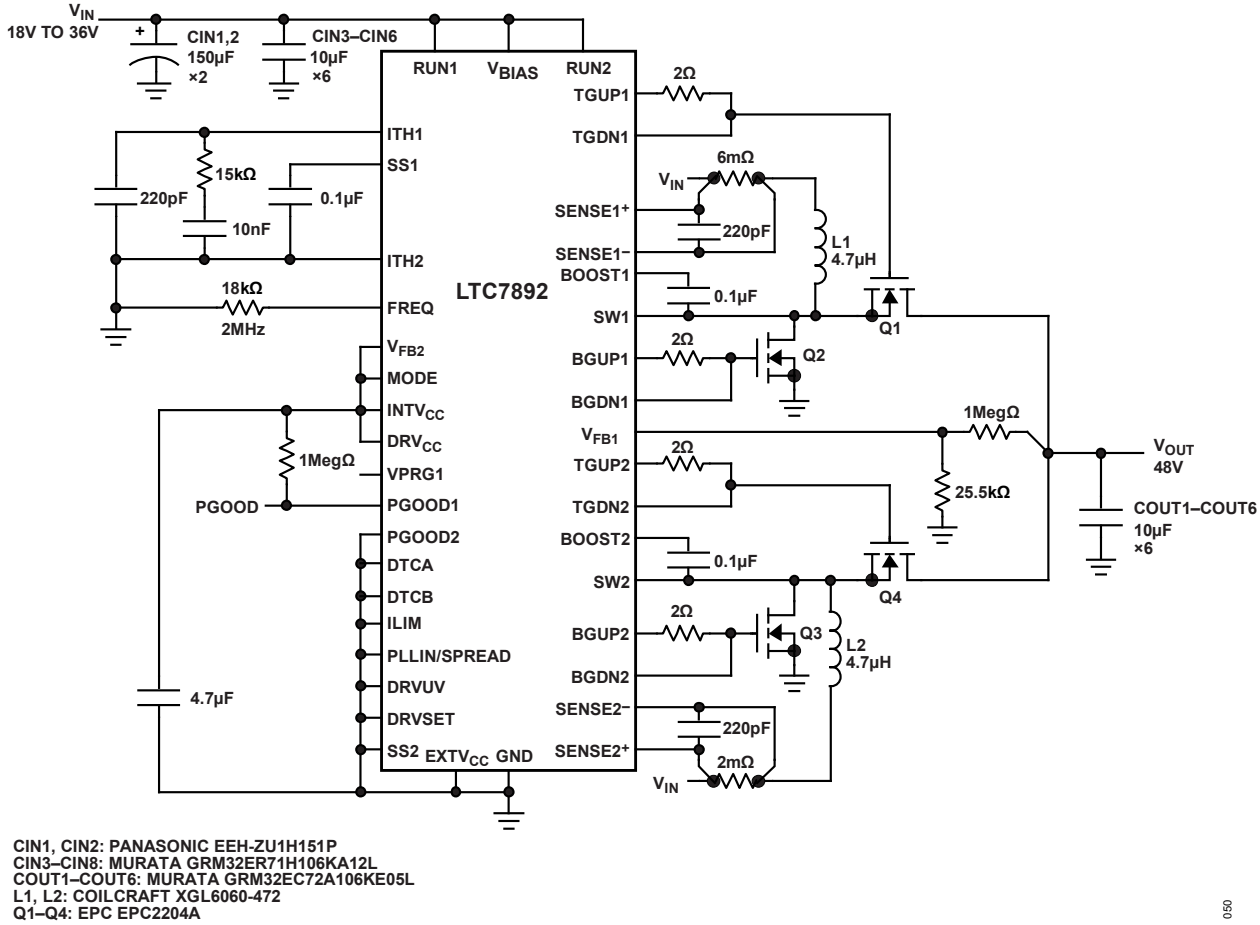
The duty-cycle percentage is maintained from cycle to cycle in a well-designed, low-noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can tame an improper PCB layout if regulator bandwidth optimization is not required. Turn on both controllers at the same time after each controller is checked for its individual performance. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top FET, which occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty-cycle jitter.

Reduce $V_{BIAS}$ from its nominal level to verify the operation of the regulator at the maximum duty cycle. Check the operation of the undervoltage lockout circuit by further lowering $V_{BIAS}$ while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOSTx, SWx, TGxxx, and possibly BGxxx connections and the sensitive voltage and current pins. Place the capacitor across the current sensing pins next to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high-frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between $C_{IN}$, the top FET, and the bottom FET components to the sensitive current and voltage sensing traces. In addition, investigate the common GND path voltage pickup between these components and the GND pin of the IC.

A problem that may be missed in an otherwise properly working switching regulator results when the current sensing leads are hooked up backward. The output voltage under this improper hookup is maintained, but the advantages of current mode control are not realized. Compensation of the voltage loop is more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor. The regulator maintains control of the output voltage even during this condition.

## TYPICAL APPLICATIONS




CIN1, CIN2: PANASONIC EEH-ZU1H151P
CIN3–CIN8: MURATA GRM32ER71H106KA12L
COUT1–COUT6: MURATA GRM32EC72A106KE05L
L1, L2: COILCRAFT XGL6060-472
Q1–Q4: EPC EPC2204A

*Figure 50. High Frequency (2MHz), Dual-Phase, Single 48V Output Boost Converter Using GaN FETs*

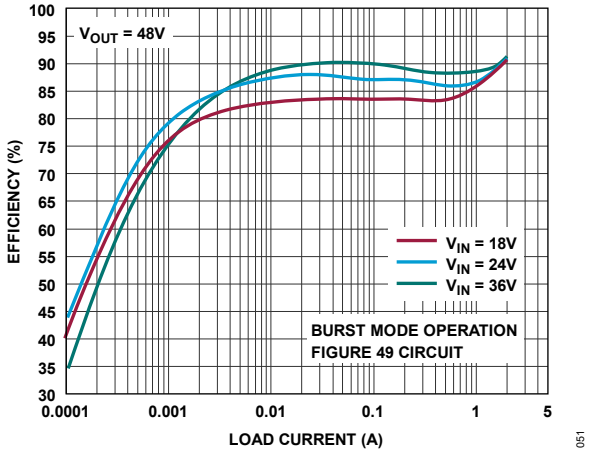


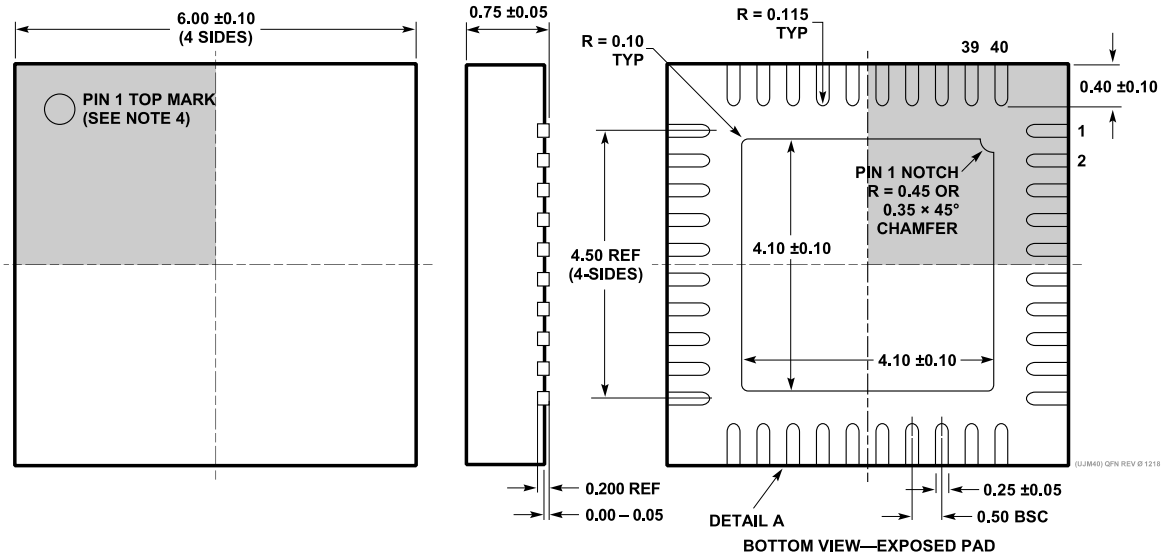

*Figure 51. Efficiency vs Load Current for Figure 50*

## RELATED PARTS

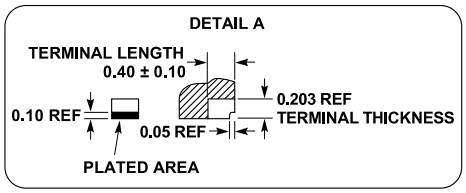
| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3788 | 38V, Multiphase Dual Output Synchronous Step-Up Controller | 4.5V (Down to 2.5V After Start-Up) ≤ $V_{IN}$ ≤ 38V, $V_{OUT}$ Up to 60V, PLL Fixed Frequency of 50kHz to 900kHz, 5mm × 5mm, QFN-32, SSOP-28 |
| LTC3897 | 65V, PolyPhase Synchronous Boost Controller with Input/Output Protection | 4.5V ≤ $V_{IN}$ ≤ 65V, 75V Peak, $V_{OUT}$ Up to 60V, PLL Fixed Frequency 75kHz to 550kHz, $I_Q$ = 55µA, TSSOP-38, 5mm × 7mm, QFN-38 |
| LTC3786 | 38V, Low $I_Q$ Synchronous Boost Controller with PassThru | 4.5V (Down to 2.5V After Start-Up) ≤ $V_{IN}$ ≤ 38V, $V_{OUT}$ Up to 60V, PLL fixed frequency of 50kHz to 900kHz, 3mm × 3mm, QFN-32, MSOP-16E |
| LTC3787 | 38V, Multiphase, Dual Channel Synchronous Boost Controller with PassThru | 4.5V (Down to 2.5V After Start-Up) ≤ $V_{IN}$ ≤ 38V, $V_{OUT}$ Up to 60V, PLL Fixed Frequency of 50kHz to 900kHz, 4mm × 5mm, QFN-28, SSOP-28 |
| LTC3784 | 60V, Low $I_Q$, Multiphase Synchronous Boost Controller with PassThru | 4.5V (Down to 2.5V After Start-Up) ≤ $V_{IN}$ ≤ 60V, $V_{OUT}$ Up to 60V, PLL Fixed Frequency of 50kHz to 900kHz, $I_Q$ = 28µA, 4mm x 5mm, QFN-28, SSOP-28 |
| LTC7890 | 100V, Low $I_Q$, Dual, 2-Phase Synchronous Step-Down Controller for GaN FETs | 4V ≤ $V_{IN}$ ≤ 100V, $V_{OUT}$ Up to 60V, PLL Fixed Frequency of 100kHz to 3MHz, $I_Q$ = 5µA, 6mm x 6mm, QFN-40 (Side Wettable) |
| LTC7891 | 100V, Low $I_Q$, Synchronous Step-Down Controller for GaN FETs | 4V ≤ $V_{IN}$ ≤ 100V, 0.8 ≤ $V_{OUT}$ ≤ 60V, PLL Fixed Frequency of 100kHz to 3MHz, $I_Q$ = 5µA, 4mm x 5mm, QFN-28 (Side Wettable) |
| LTC7893 | 100V, Low $I_Q$, Synchronous Boost Controller for GaN FETs | 4V (Down to 1V After Start-Up) ≤ $V_{IN}$ ≤ 60V, $V_{OUT}$ Up to 100V, PLL Fixed Frequency of 100kHz to 3MHz, $I_Q$ = 15µA, 4mm x 5mm, QFN-28 (Side Wettable) |
| LT8418 | 100V, Half-Bridge GaN Driver with Smart Integrated Bootstrap Switch | 3.85V to 5.5V Operation, 4A/0.6Ω Peak Pull-up, 8A/0.2Ω Peak Pull-down, 10ns (typ) Propagation Delay, 1.67mm x 1.67mm, 12-Ball WLCSP |

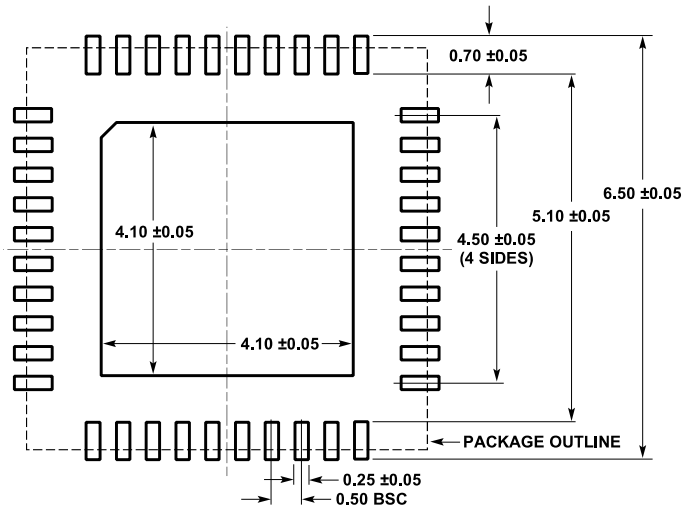
# OUTLINE DIMENSIONS

**UJM Package**
**40-Lead Plastic Side Wettable QFN (6mm x 6mm)**
(Reference LTC DWG # 05-08-1681 Rev Ø)




NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH
   MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND
   BOTTOM OF PACKAGE




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

# ORDERING GUIDE

**Table 8. Ordering Guide**

| LEAD-FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC7892AUJM#PBF | LTC7892AUJM#TRPBF | LTC7892 UJM | 40-Lead QFN (6mm × 6mm, Plastic Side Wettable) | −40°C to 125°C |
| **AUTOMOTIVE PRODUCTS*** | | | | |
| LTC7892AUJM#WPBF | LTC7892AUJM#WTRPBF | LTC7892 UJM | 40-Lead QFN (6mm × 6mm, Plastic Side Wettable) | −40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with the #TRMPBF suffix.

*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.