ADSP21835W-EV-SOM ® Manual

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ANALOG DEVICES

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Regulatory Compliance

The *ADSP21835W-EV-SOM* evaluation board is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer-end product or as a portion of a consumer-end product. The board is an open system design, which does not include a shielded enclosure and, therefore, may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The *ADSP21835W-EV-SOM* evaluation board contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused boards in the protective shipping package.	

Contents

1 Preface

Thank you for purchasing the Analog Devices, Inc. System-on-Module (SoM) *ADSP21835W-EV-SOM* evaluation board.

The *ADSP21835W-EV-SOM* primarily hosts the ADSP-21835W audio processor, 8 Gbit of ISSI DDR3 memory, a 512 Mbit Quad SPI FLASH, voltage regulation, a FTDI UART to USB interface, and a high speed external connector array that contains all of the peripheral I/O signals. Through the high speed external connector array, the *ADSP21835W-EV-SOM* is intended for use with a growing family of SoM carrier products that contain a variety of peripherals to support different applications. The SoM carrier base products that exist today are the *EV-SOMCRR-EZKIT* and *EV-SOMCRR-EZLITE*.

The CrossCore Embedded Studio® (CCES) software development tool chain is required for a full evaluation of this hardware platform. The *ADSP21835W-EV-SOM* can also be used in a limited standalone mode while not plugged into a SoM Carrier such as the *EV-SOMCRR-EZKIT* or *EV-SOMCRR-EZLITE*. The standalone mode is useful for evaluating the CCES Software Development Tools and benchmarking software algorithms that do not require peripheral I/O.

The evaluation board is designed to be used in conjunction with the CrossCore Embedded Studio®3.0.0+ development environment for advanced application code development and debug, with features that enable the ability to:

- Create, compile, assemble, and link application programs written in C++, C, and assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers

Purpose of This Manual

This manual provides instructions for installing the product hardware (board). This manual describes the operation and configuration of board components and provides guidelines for running code on the board.

Manual Contents

The manual consists of:

- *Using the board*

  Provides basic board information.

- *Hardware Reference*

  Provides information about the hardware aspects of the board.

- *Bill of Materials*

  A companion file in PDF format that lists all of the components used on the board is available on the website at http://www.analog.com/ADSP21835W-EV-SOM.

- *Schematic*

  A companion file in PDF format documenting all of the circuits used on the board is available on the website at http://www.analog.com/ADSP21835W-EV-SOM.

Technical Support

You can reach Analog Devices technical support in one of the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:

  http://ez.analog.com/community/dsp

- Submit your questions to technical support directly at:

  http://www.analog.com/support

- E-mail your questions about processors, DSPs, and tools development software from ***CrossCore Embedded Studio*** or ***VisualDSP++®***:

  If using CrossCore Embedded Studio or VisualDSP++ choose ***Help*** > ***Email Support***. This creates an e-mail to processor.tools.support@analog.com and automatically attaches your CrossCore Embedded Studio or VisualDSP++ version information and `license.dat` file.

- E-mail your questions about processors and processor applications to:

  processor.support@analog.com

- Contact your Analog Devices sales office or authorized distributor. Locate one at:

  http://www.analog.com/adi-sales

Supported Integrated Circuit

This evaluation system supports the Analog Devices ADSP-21835W IC.

Supported Tools

Information about code development tools for the *ADSP21835W-EV-SOM* evaluation board and ADSP-2183x product family is available at:

http://www.analog.com/ADSP21835W-EV-SOM

Product Information

Product information can be obtained from the Analog Devices website and the online help system.

Information about the ADSP-21835W product family is available at:

Analog Devices Website

The Analog Devices website, http://www.analog.com, provides information about a broad range of products - analog integrated circuits, amplifiers, converters, transceivers, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, MyAnalog.com is a free feature of the Analog Devices website that allows customization of a web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

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EngineerZone

EngineerZone is a technical support forum from Analog Devices, Inc. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

2 Using the Board

This chapter provides information on the major components and peripherals on the board, along with instructions for installing and setting up the emulation software.

Product Overview

Below is an image of the *ADSP21835W-EV-SOM* board.

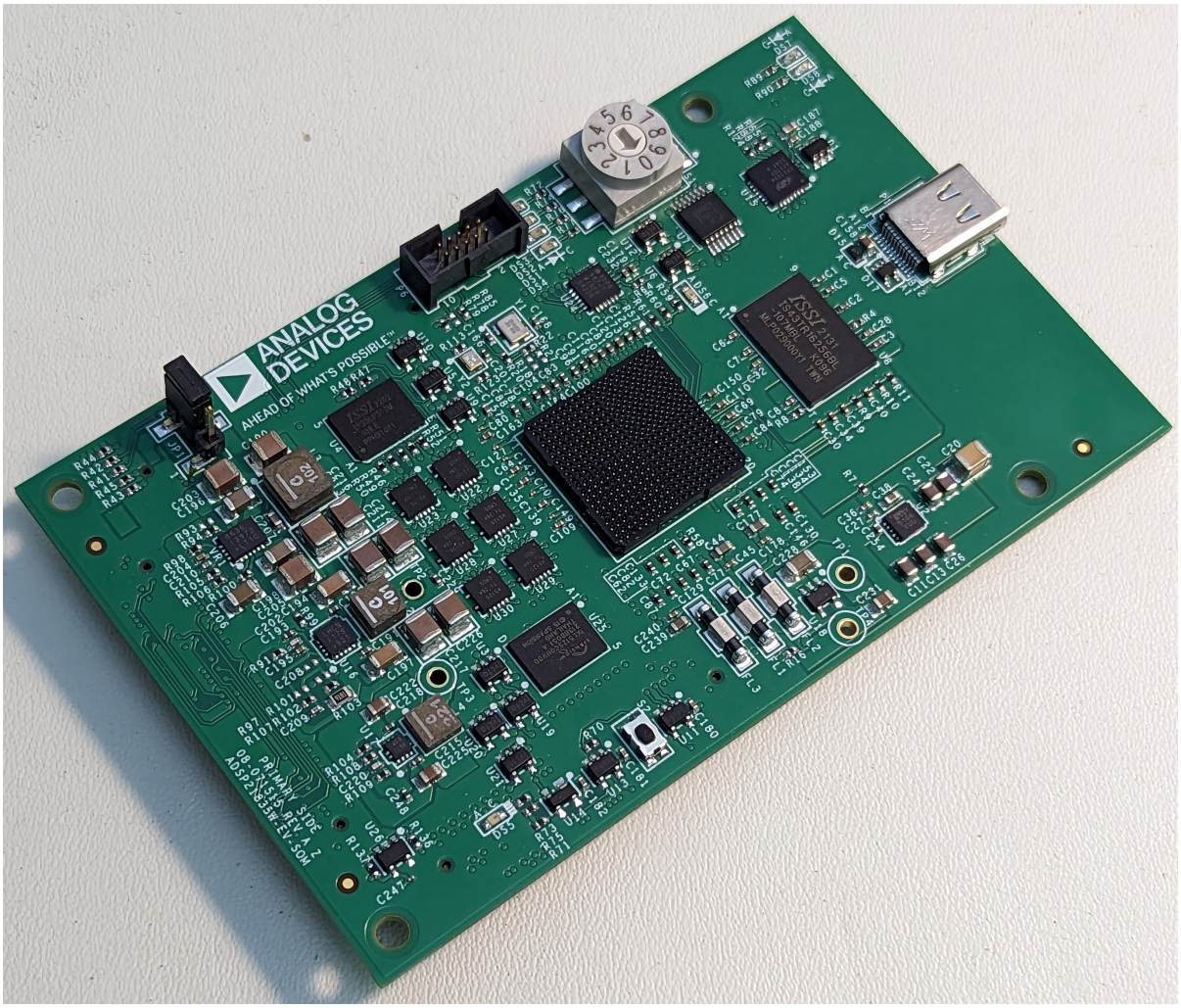

Figure 2-1: Board View

The board features:

- Analog Devices ADSP-21835W processor
  - SHARC-FX Core
  - 400 ball BGA
  - 25 MHz oscillator
- DDR3 Memory
  - 256Mx16 bit (4Gbit)
  - ISSI IS43TR16256BL-107MBL
  - 1.39V
- SPI Flash Quad (`SPI2`) Memory
  - 512Mbit
  - ISSI IS25LP512M - 512M-bit Serial Flash Memory with Dual and Quad SPI
  - Single/Dual/Quad SPI
- HyperFlash Memory
  - 512Mbit FLASH/64Mbit RAM
  - Cypress S71KL512SC0BHB003
  - xSPI HyperBus Device
- Debug Interface (JTAG)
  - JTAG 10-pin 0.05” header
- LEDs
  - Eight LEDs: one power (green), one board reset (red), three general-purpose (amber), one fault (red) and two UART leds (amber)
- Pushbuttons
  - One pushbutton, RESET
- SoM Interface Connector
  - DAI
  - SPORT

- SPI
- UART
- TWI
- Link Port
- GPIO
- MLB
- RESET
- GND/3.3V/5V/12V output

Package Contents

Your *ADSP21835W-EV-SOM* package contains the following items.

- *ADSP21835W-EV-SOM* board

Contact the vendor where you purchased your *ADSP21835W-EV-SOM* evaluation board or contact Analog Devices, Inc. if any item is missing.

Default Configuration

The ***Default Hardware Setup*** figure shows the default settings for jumpers and switches and the location of the jumpers, switches, connectors, and LEDs. Confirm that your board is in the default configuration before using the board.

Default Config

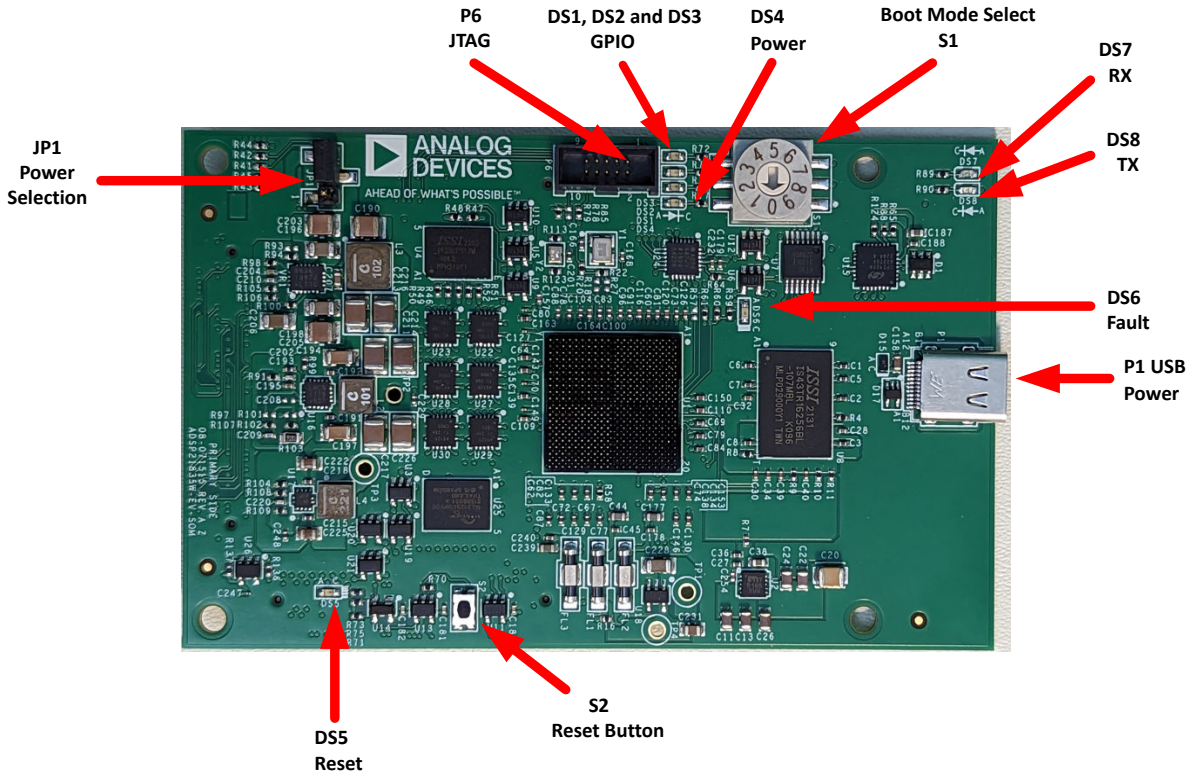

Figure 2-2: Default Hardware Setup

CrossCore Embedded Studio (CCES) Setup

Information on using the CCES tools is available at: https://analog.com/cces-quickstart

Debug Interface

The *ADSP21835W-EV-SOM* provides a JTAG connection via `P6`. This is for attaching an emulator, such as the ICE-1000 or ICE-2000 for debugging.

When the *ADSP21835W-EV-SOM* is connected to a carrier board the Debug Agent on the carrier board can be used. To use this Debug Agent, all postions on SW1 (on the carrier board) must be in the ON position. If an emulator, such as the ICE-1000 or ICE-2000, is used instead all postions on SW1 must be in the OFF position.

Board Power

The *ADSP21835W-EV-SOM* is powered via `USB Type C` when the board is in standalone mode. When in this mode the jumper on `JP1` should be on Pins 1-2 to select power input from `USB Type C`. When the *ADSP21835W-EV-SOM* is connected to a carrier board the power is supplied via the carrier board. When in this mode the jumper on `JP1` should be on Pins 2-3 to select power input from the carrier board.

Power-On-Self Test

The Power-On-Self-Test Program (POST) tests all the EZ-KIT carrier board peripherals and validates functionality as well as connectivity to the processor. Once assembled, each EZ-KIT carrier board is fully tested for an extended period of time with POST for all the compatible SoM modules. All EZ-KIT carrier boards are shipped with POST preloaded into flash memory. The POST is executed by resetting the board and connecting the USB To UART to your PC with an open terminal window. The POST also can be used as a reference for a custom software design or hardware troubleshooting.

Note that the source code for the POST program is included in the Board Support Package (BSP) along with the readme file that describes how the board is configured to run POST.

Example Programs

Example programs are provided with the *ADSP21835W-EV-SOM* Board Support Package (BSP) to demonstrate various capabilities of the product. The programs can be found in the `ADSP21835W-EV-SOM\examples` installation folder. Refer to the readme file provided with each example for more information.

Reference Design Information

A reference design info package is available for download on the Analog Devices Web site. The package provides information on the schematic design, layout, fabrication, and assembly of the board.

The information can be found at:

http://www.analog.com/ADSP21835W-EV-SOM

IS25LP512M - 512M-bit Serial Flash Memory with Dual and Quad SPI

The IS25LP512M Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O, as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 133MHz allow for equivalent clock rates of up to 532MHz (133MHz x 4) which equates to 66.5Mbytes of data throughput. The IS25xE series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock.These transfer rates can outperform 16-bit Parallel Flash memories, allowing for efficient memory access to support XIP (eXecute In Place) operation.

The memory array is organized into programmable pages of 256/512 bytes. This family supports page program mode where 1 to 256/512 bytes of data are programmed in a single command.

QPI (Quad Peripheral Interface) supports 2-cycle instructions, further reducing instruction times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64K/256Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

IS43TR16256BL - 256Mx16 4Gb DDR3 SDRAM

- Low Voltage (L): VDD and VDDQ = 1.35V + 0.1V, -0.067V - Backward compatible to 1.5V
- High speed data transfer rates with system frequency up to 933 MHz
- 8 internal banks for concurrent operation
- 8n-Bit pre-fetch architecture
- Programmable CAS Latency
- Programmable Additive Latency: 0, CL-1,CL-2
- Programmable CAS WRITE latency (CWL) based on tCK
- Programmable Burst Length: 4 and 8
- Programmable Burst Sequence: Sequential or Interleave
- BL switch on the fly
- Auto Self Refresh(ASR)
- Self Refresh Temperature(SRT)
- Refresh Interval: 7.8 µs (8192 cycles/64 ms) Tc= -40°C to 85°C 3.9 µs (8192 cycles/32 ms) Tc= 85°C to 95°C 1.95 µs (8192 cycles/16 ms) Tc= 95°C to 105°C 0.97 µs (8192 cycles/8 ms) Tc= 105°C to 115°C
- Partial Array Self Refresh
- Asynchronous RESET pin
- TDQS (Termination Data Strobe) supported (x8 only)
- OCD (Off-Chip Driver Impedance Adjustment)
- Dynamic ODT (On-Die Termination)
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Write Leveling
- Up to 200 MHz in DLL off mode

LT8636 - 42V, 5A/7A Peak Synchronous Step-Down Silent Switcher with 2.5µA Quiescent Current

The LT8636 synchronous step-down regulator features Silent Switcher architecture designed to minimize EMI emissions while delivering high efficiency at high switching frequencies. Peak current mode control with a 30ns minimum on-time allows high step-down ratios even at high switching frequencies.

The LT8636's ultralow 2.5µA quiescent current—with the output in full regulation—enables applications requiring highest efficiency at very small load currents. A CLKOUT pin enables synchronizing other regulators to the LT8636.

Burst Mode operation enables ultralow standby current consumption, forced continuous mode can control frequency harmonics across the entire output load range, or spread spectrum operation can further reduce EMI emissions. Soft-start and tracking functionality is accessed via the TR/SS pin, and an accurate input voltage UVLO threshold can be set using the EN/UV pin.

LTC3307A - 5V, 3A Synchronous Step-Down Silent Switcher in 2mm × 2mm LQFN

The LTC3307A is a very small, high efficiency, low noise, monolithic synchronous 3A step-down DC/DC converter operating from a 2.25V to 5.5V input supply. Using constant frequency, peak current mode control at switching frequencies up to 3MHz and minimum on-time as low as 22ns, this regulator achieves fast transient response with small external components. Silent Switcher architecture minimizes EMI emissions.

The LTC3307A operates in forced continuous or pulse skip mode for low noise, or low-ripple Burst Mode operation for high efficiency at light loads, ideal for battery-powered systems. The IC regulates output voltages as low as 500mV. Other features include output overvoltage protection, short-circuit protection, thermal shutdown, clock synchronization, and up to 100% duty cycle operation for low dropout. The device is available in a low profile 12-lead 2mm × 2mm × 0.74mm LQFN package with exposed pad for low thermal resistance.

LTC3310S - 5V, 10A Synchronous Step-Down Silent Switcher 2 in 3mm × 3mm LQFN

The LTC3310S is a very small, low noise, monolithic step-down DC/DC converter capable of providing up to 10A of output current from a 2.25V to 5.5V input supply. The device employs Silent Switcher 2 architecture with internal hot loop bypass capacitors to achieve both low EMI and high efficiency at switching frequencies as high as 5MHz. For systems with higher power requirements, multi-phasing parallel converters is readily implemented.

The LTC3310S uses a constant-frequency, peak current mode control architecture for fast transient response. A 500mV reference allows for low voltage outputs. 100% duty cycle operation delivers low drop out.

Other features include a power good signal when the output is in regulation, precision enable threshold, output overvoltage protection, thermal shutdown, a temperature monitor, clock synchronization, mode selection and output short circuit protection.

ADP151 - Ultralow Noise, 200 mA, CMOS Linear Regulator

The ADP151 is an ultralow noise, low dropout (LDO) linear regulator that operates from 2.2 V to 5.5 V and provides up to 200 mA of output current. The low 135 mV dropout voltage at 200 mA load improves efficiency and allows operation over a wide input voltage range.

Using an innovative circuit topology, the ADP151 achieves ultralow noise performance without the necessity of a bypass capacitor, making the device ideal for noise-sensitive analog and RF applications. The ADP151 also achieves ultralow noise performance without compromising the power supply rejection ratio (PSRR) or transient line and load performance. The low 265 µA of operating supply current at 200 mA load makes the ADP151 suitable for battery-operated portable equipment.

The ADP151 also includes an internal pull-down resistor on the EN input.

The ADP151 is specifically designed for stable operation with tiny 1 µF, ±30% ceramic input and output capacitors to meet the requirements of high performance, space constrained applications.

The ADP151 is capable of 16 fixed output voltage options, ranging from 1.1 V to 3.3 V.

Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADP151 is available in tiny 5-lead TSOT, 6-lead LFCSP, and 4-ball, 0.4 mm pitch, halide-free WLCSP packages for the smallest footprint solution to meet a variety of portable power application requirements.

3 Hardware Reference

This chapter describes the hardware design of the *ADSP21835W-EV-SOM*.

System Architecture

The board's configuration is shown in the ***Block Diagram*** figure.

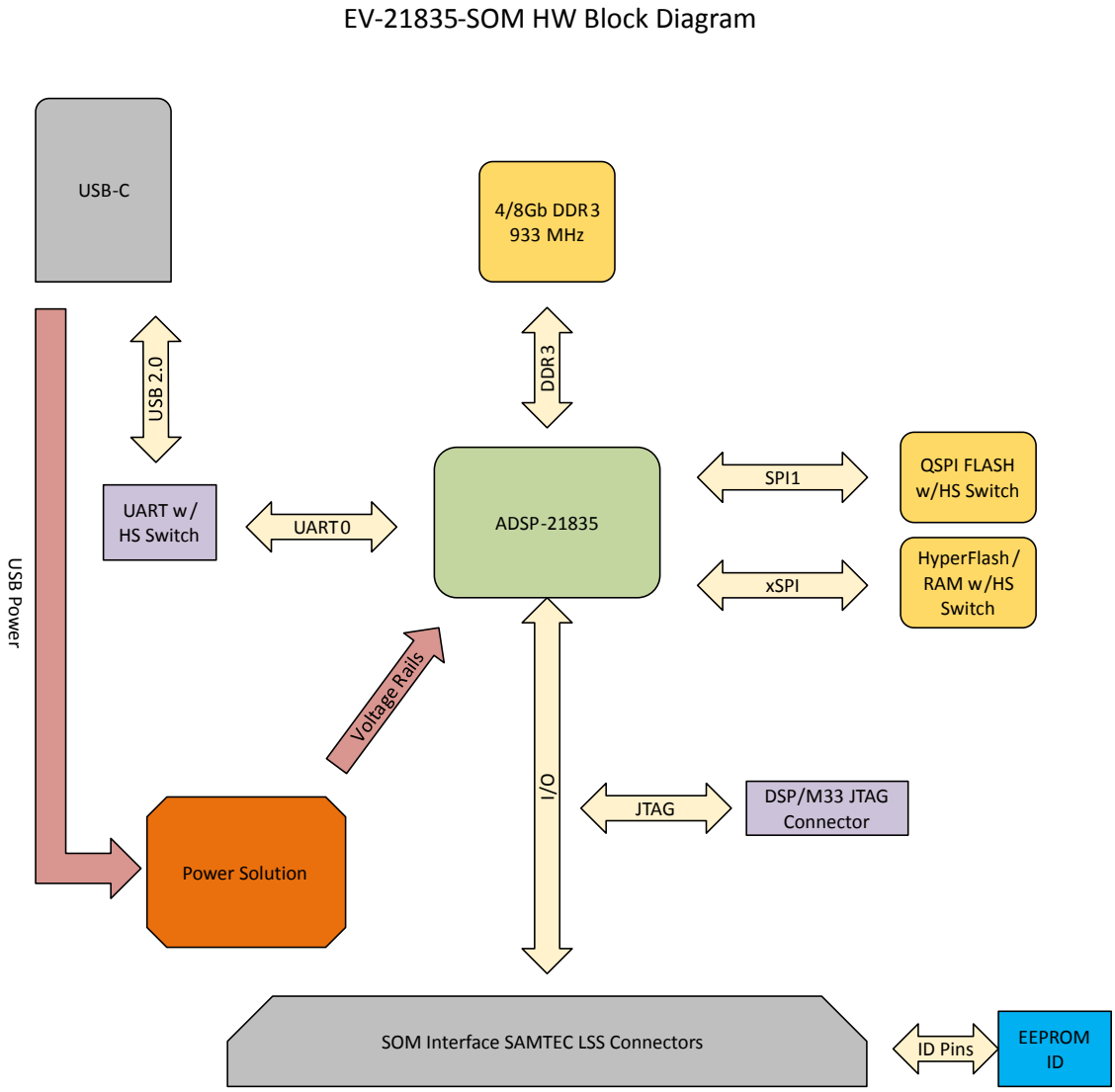

Figure 3-1: Block Diagram

This System on Module is designed to demonstrate the ADSP-21835W processor's capabilities. The board has a 25 MHz input clock and runs at a max core clock frequency of 1GHz.

User I/O to the processor is provided in the form of two pushbuttons and three LEDs.

The software-controlled switches (SoftConfig) facilitate the switch multi-functionality by disconnecting the push-buttons from their associated processor pins and reusing the pins elsewhere on the board.

Software-Controlled Switches (SoftConfig)

On the board, most of the traditional mechanical switches and jumpers have been replaced by I^2C software-controlled switches. The remaining mechanical switches are provided for the boot mode and pushbuttons. Reference any `SoftConfig*.c` file found in the installation directory for an example of how to set up the SoftConfig feature of

the board through software. The SoftConfig section of this manual serves as a reference to any user that intends to modify an existing software example. If software provided by ADI is used, there should be little need to reference this section.

NOTE: Care should be taken when changing SoftConfig settings not to create a conflict with interfaces. This is especially true when connecting extender cards.

Overview of SoftConfig

In order to further clarify the use of electronic single FET switches and multi-channel bus switches, an example of each is illustrated and compared to a traditional mechanical switching solution. This is a generic example that uses similar FET and bus switch components that are on the board.

After this generic discussion there is a detailed explanation of the SoftConfig interface specific to the *ADSP21835W-EV-SOM*.

The ***Example of Individual FET Switches*** figure shows two individual FET switches (Pericom PI3A125CEX) with reference designators UA and UB. Net names ENABLE_A and ENABLE_B control UA and UB. The default FET switch enable settings in this example are controlled by resistors RA and RB which pull the enable pin 1 of UA and UB to ground (low). In a real example, these enable signals are controlled by the IO expander. The default pull-down resistors connects the signals EXAMPLE_SIGNAL_A and EXAMPLE_SIGNAL_B and also connects signals EXAMPLE_SIGNAL_C and EXAMPLE_SIGNAL_D. To disconnect EXAMPLE_SIGNAL_A from EXAMPLE_SIGNAL_B, the IO expander is used to change ENABLE_A to a logic 1 through software that interfaces with the Microchip. The same procedure for ENABLE_B disconnects EXAMPLE_SIGNAL_C from EXAMPLE_SIGNAL_D.

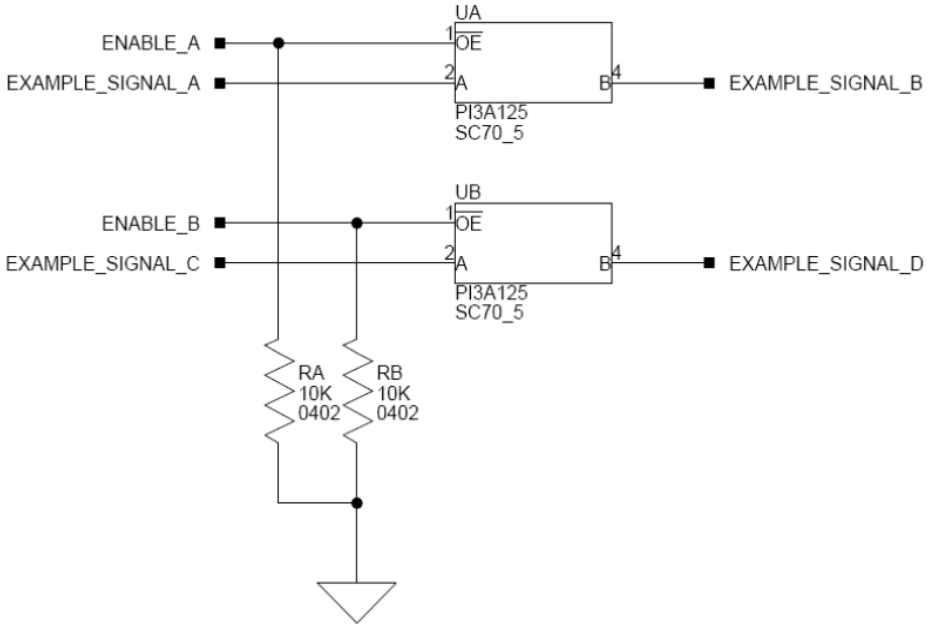

Figure 3-2: Example of Individual FET Switches

The following figure shows the equivalent circuit to the ***Example of Individual FET Switches*** figure but utilizes mechanical switches that are in the same package. Notice the default is shown by black boxes located closer to the ***ON*** label of the switches. In order to disconnect these switches, physically move the switch to the OFF position.

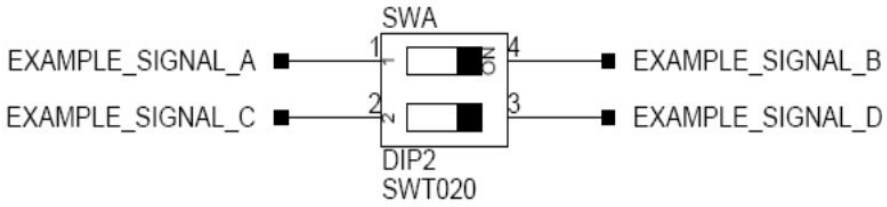

Figure 3-3: Example of a Mechanical Switch (Equivalent to Example of Individual FET Switches Figure)

The ***Example of Bus Switch*** figure shows a bus switch example, reference designator `UC` (Pericom PI3LVD512ZHE), selecting between lettered functionality and numbered functionality. The signals on the left side are multiplexed signals with naming convention letter_number. The right side of the circuit shows the signals separated into letter and number, with the number on the lower group (`0B1`) and the letter on the upper group (`0B2`). The default setting is controlled by the signal `CONTROL_LETTER_NUMBER` which is pulled low. This selects the number signals on the right to be connected to the multiplexed signals on the left by default. In this example, the IO expander is not shown but controls the signal `CONTROL_LETTER_NUMBER` and allows the user to change the selection through software.

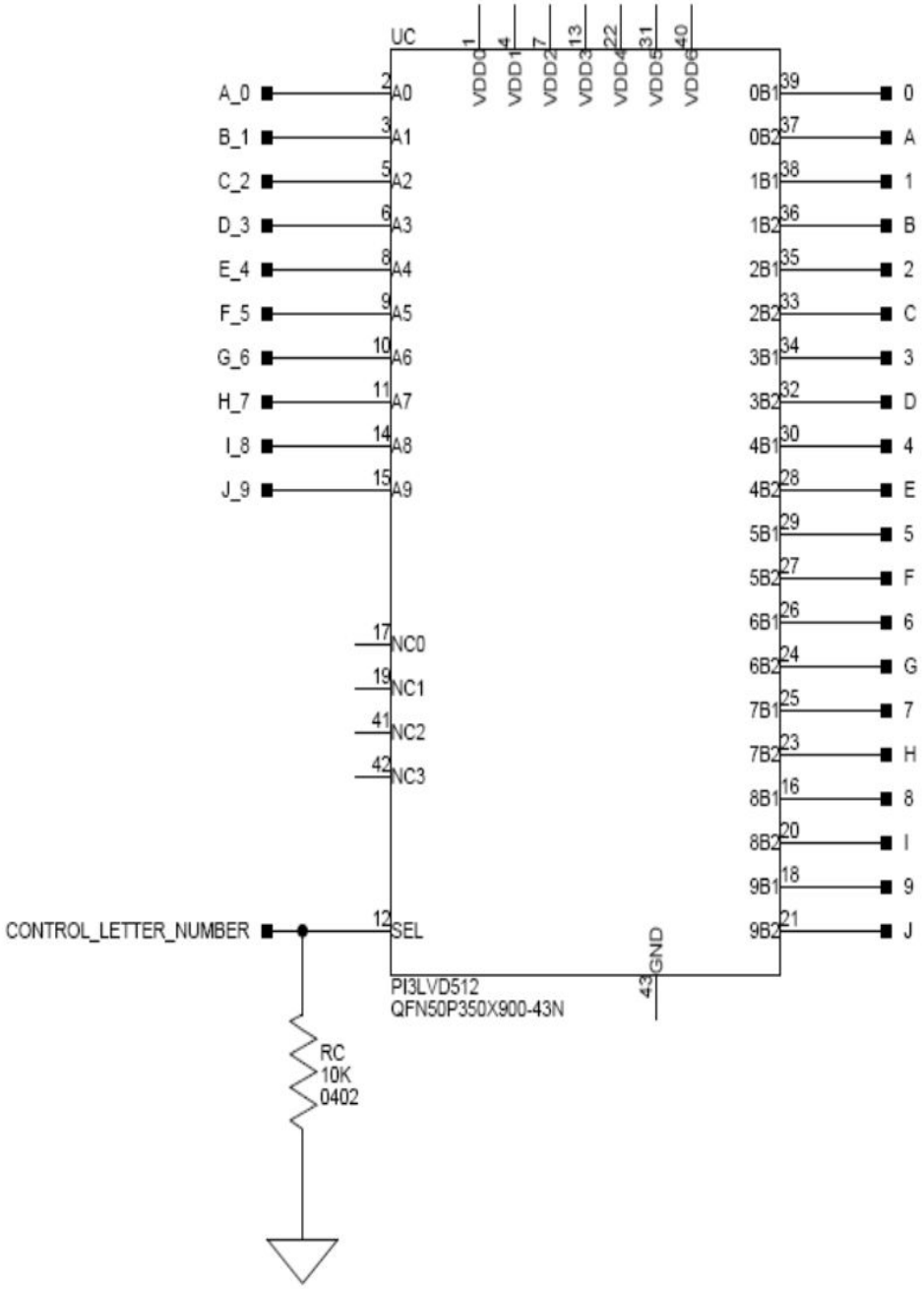

Figure 3-4: Example of a Bus Switch

The following figure shows the equivalent circuit to the ***Example of Bus Switch*** figure but utilizes mechanical switches. Notice the default for reference designators SWC and SWD is illustrated by black boxes located closer to the ***ON*** label of the switches to enable the number signals by default. Also notice the default setting for reference designators SWE and SWF is OFF. In order to connect the letters instead of the numbers, the user physically changes all switches on SWC and SWD to the OFF position and all switches on SWE and SEF to the ON position.

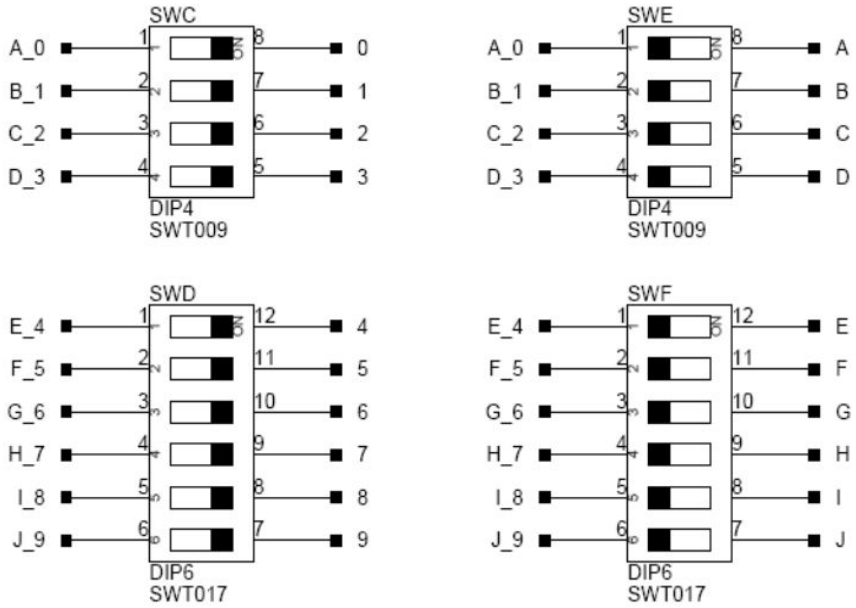

Figure 3-5: Example of a Mechanical Switch (Equivalent to Example of Bus Switch)

SoftConfig on the Board

The Analog Devices ADP5587-1 GPIO extenders provide control for individual electronic switches. The TWI interface of the processor communicates with the GPIO extender devices. There are individual switches with default settings that enable basic board functionality.

The ***Default Processor Interface Availability*** table lists the processor and board interfaces that are available by default. Note that only interfaces affected by software switches are listed in the table.

Table 3-1: Default Processor Interface Availability

Interface	*Availability by Default*
UART0	USB to UART IC
SPI 1 Flash	Quad mode enabled
xSPI	xSPI device enabled,xSPI to SOM Interface disabled
LEDs	Enabled

Programming SoftConfig Switches

On the board, an ADI ADP5587-1 devices exist. The ADP5587 can be configured as a GPIO extender or a keypad interface. It is used as a GPIO Extended on the System on Module evaluation board.

Refer to the ASP5587-1 datasheet for programming information. https://www.analog.com/media/en/technical-documentation/data-sheets/adp5587.pdf

Each example in the Board Support Software (BSP) includes source files that program the soft switches, even if the default settings are being used. The `README` for each example identifies only the signals that are being changed

from their default values. The code that programs the soft switches is located in the `SoftConfig_XXX.c` file in each example where XXX is the name of the baord.

The part number of the ADP5587-1 determines the address of the IC. The ADP5587ACPZ has (***I^2C Hardware Address 0x68*** and the ADP5587ACPZ-1 has ***I^2C Hardware Address 0x60***).

Table below ***Output Signals of ADP5587-1 GPIO Expander (U24)*** show the output signals of the ADI GPIO extender (***U24***), with a TWI address of `0110 100X`, where `X` represents the read or write bit. The signals that control an individual FET have an entry in the ***FET*** column. The ***Component Connected*** column shows the board IC that is connected if the FET is enabled. The (`U24`) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it is in ***bold*** font in the ***Processor Signal*** column.

Table 3-2: Output Signals of ADP5587-1 GPIO Extender (U24)

Connection	*Signal Name*	*Description*	*FET*	*Processor Signal (if applicable)*	*Connected*	*Default*
C9	DS1	GPIO LED		None	LED4	Low
C8	DS2	GPIO LED		None	LED5	Low
C7	DS3	GPIO LED		None	LED2	Low
R3	$\overline{\text{SPI1FLASH\_CS\_EN}}$	Enable SPI Flash CS	U3	PA_05/SPI2_SEL1b/ OSPI_SEL1b/SMC0_D05/ SPI2_SSb	U11	High
R2	$\overline{\text{SPI1D2\_D3\_EN}}$	Enabel SPI Flash Quad Mode	U4 U5	PA_02/SPI2_D2/OSPI_D2/ TWI3_SCL/SMC0_D02/ TM0_ACLK3 PA_03/SPI2_D3/ OSPI_D3/TWI3_SDA/ SMC0_D03	U11	High
R1	$\overline{\text{UART0\_EN}}$	Enable FTDI UART to USB	U8	PA_06/SPI0_CLK/ UART0_TXb/OSPI_D4/ SMC0_D06/TM0_ACLK1 PA_07/SPI0_MISO/ UART0_RXb/OSPI_D5/ SMC0_D07/TM0_ACI0	U7	Low
R0	$\overline{\text{UART0\_FLOW\_EN}}$	Enables UART Flow Control on FTDI	U8	PA_08/SPI0_MOSI/ UART0_RTSb/OSPI_D6/ SMC0_D08/TM0_ACLK2 PA_09/SPI0_SEL1b/ UART0_CTSb/OSPI_D7/ SMC0_D09/SPI0_SSb	U7	Low
C0	$\overline{\text{SOM\_TWI2\_EN}}$	Enables TWI2 on SOM connector		TWI2		High
C1	$\overline{\text{SOM\_TWI1\_EN}}$	Enables TWI2 on SOM connector		TWI1		High

Table 3-2: Output Signals of ADP5587-1 GPIO Extender (U24) (Continued)

Connection	*Signal Name*	*Description*	*FET*	*Processor Signal (if applicable)*	*Connected*	*Default*
C2	$\overline{\text{TWI1\_EN}}$	Enables TWI on SOM		TWI1		Low
C3	$\overline{\text{SOM\_XSPI\_EN}}$	Enables xSPI on SOM connector		xSPI		High
C4	$\overline{\text{XSPI\_EN}}$	Enables xSPI on SOM		xSPI		Low

Switches

This section describes operation of the switches. The switch locations are shown in the ***Switch/Jumper Locations*** figure.

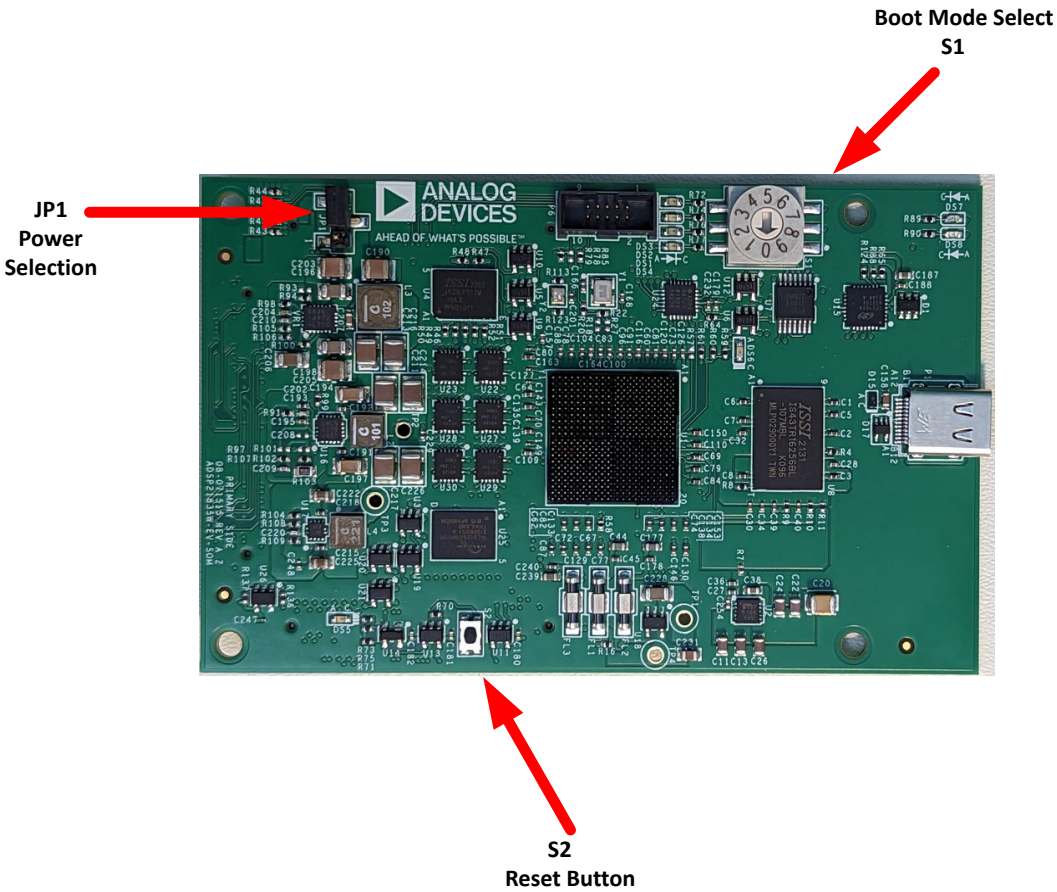

Figure 3-6: Switch/Jumper Locations

Boot Mode Select (S1)

The Boot Mode selection switch selects between the different boot modes of the processor. The ***Boot Mode Switch*** table shows the available boot mode settings. By default, the processor boots from SPI2 master boot which uses the on-board SPI flash memory.

Table 3-3: Boot Mode Switch

Position	*Processor Boot Mode*
0	No Boot
1	*SPI 1 Master Boot (Default)*
2	SPI 1 Slave Boot
3	UART0 Boot
4	Link Port 0 Boot
5	xSPI Master Boot
6	Reserved
7	Reserved

Reset Pushbutton (S2)

The reset pushbutton resets the ADSP-21835W processor. The reset signal also is connected to the expansion connectors via the SYS_HWRSTsignal. Reset (DS5) is used to indicate when the board is in reset.

Jumpers

This section describes functionality of the configuration jumpers. The ***Switch/Jumper Locations*** figure shows the jumper locations.

Power (JP1)

The Power jumper selects the input power source to the EV-SC598-SOM. Pin 1-2 selects power input from the P1 USB Port and Pin 2-3 selects Power from the SoM Interface Connection. When using the EV-SOMCRR-EZKIT or other plug in carrier board, use Jumper setting Pin 2-3.

LEDs

This section describes the on-board LEDs. The ***LED Locations*** figure shows the LED locations.

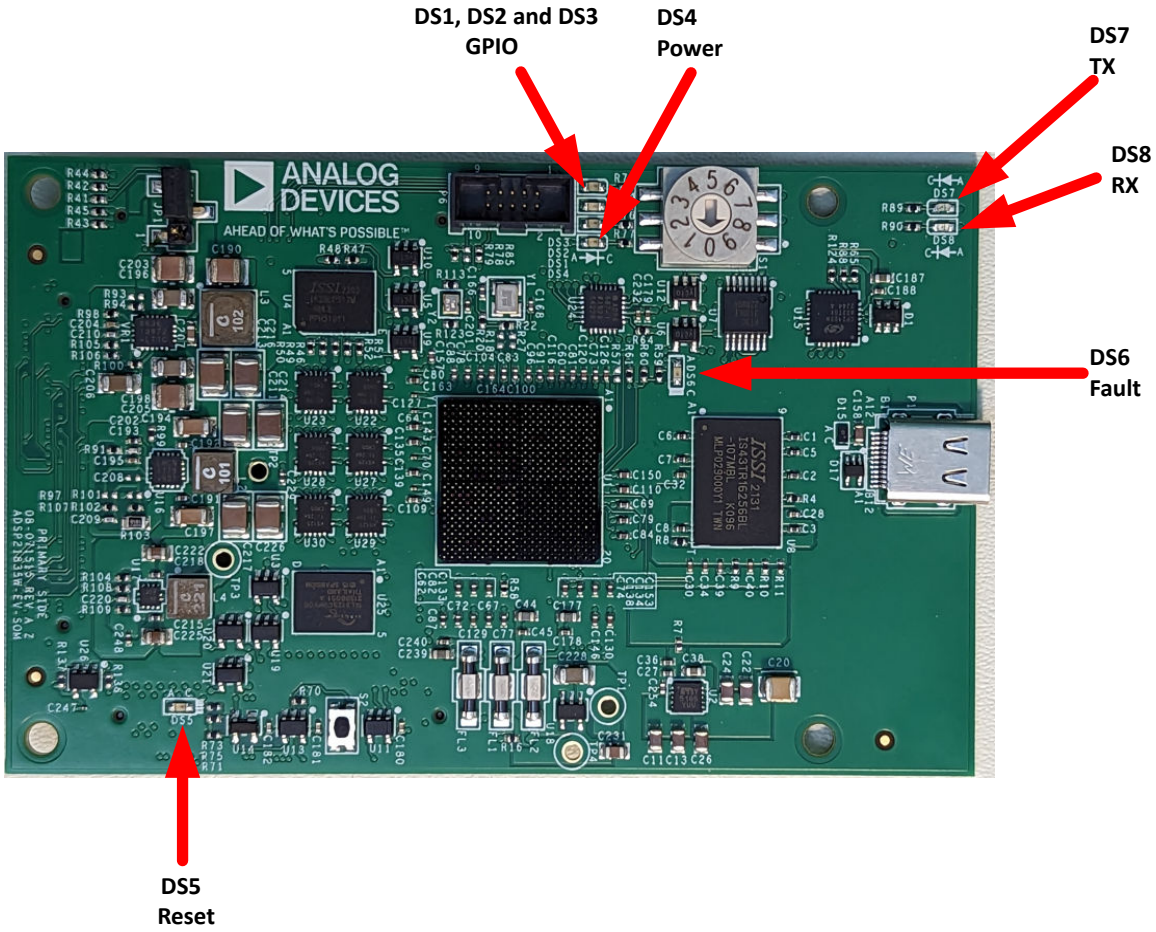

Figure 3-7: LED Locations

Fault (DS6)

When ON, it indicates a system fault. For more information, refer to the ADSP-2183xHardware Reference Manual.

Power (DS4)

When ON (green), it indicates that power is being supplied to the board properly.

GPIO (DS1, DS2, DS3)

Three LEDs are connected to the SoftConfig(see the ***GPIO LEDs*** table). The LEDs are active low and are turned ON (amber) by writing to the U24 SoftConfig IC.

Table 3-4: GPIO LEDs

Reference Designator	*Programmable Flag Pin*
DS1	SoftSwitch
DS2	SoftSwitch

Table 3-4: GPIO LEDs (Continued)

Reference Designator	*Programmable Flag Pin*
DS3	SoftSwitch

Reset (DS5)

When ON (red), it indicates that the board is in reset. A master reset is asserted by pressing S2, which activates the LED. For more information, see Reset Pushbutton (S2).

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in the ***Connector Locations*** figure.

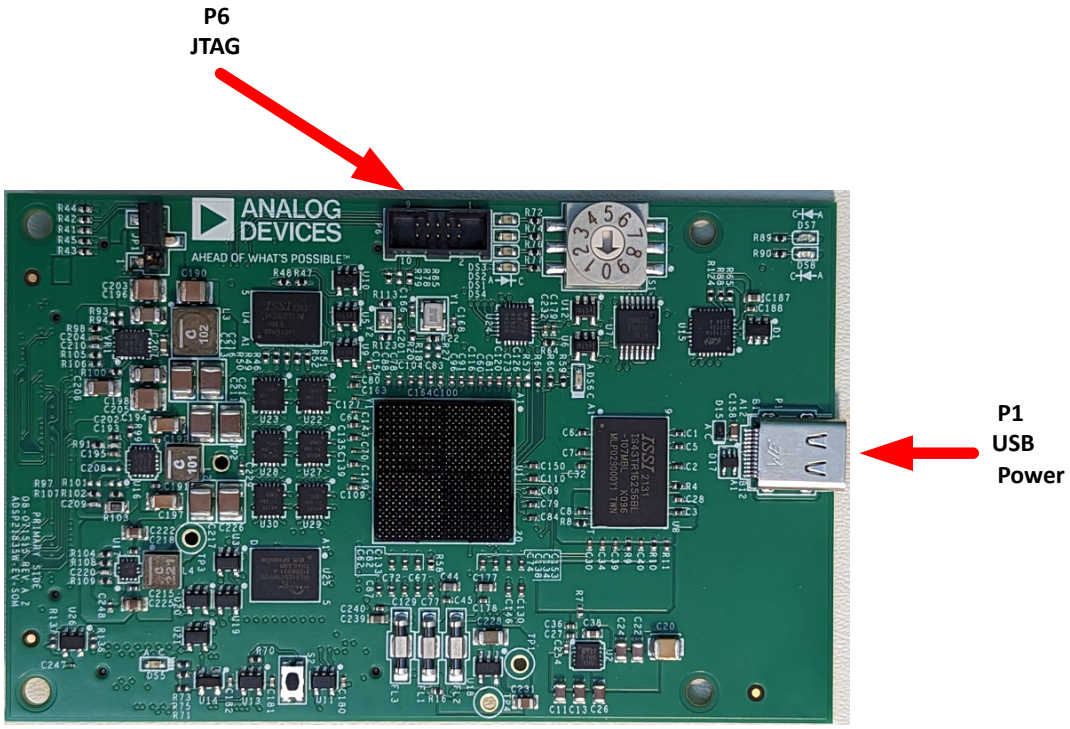

Figure 3-8: Connector Locations Top View

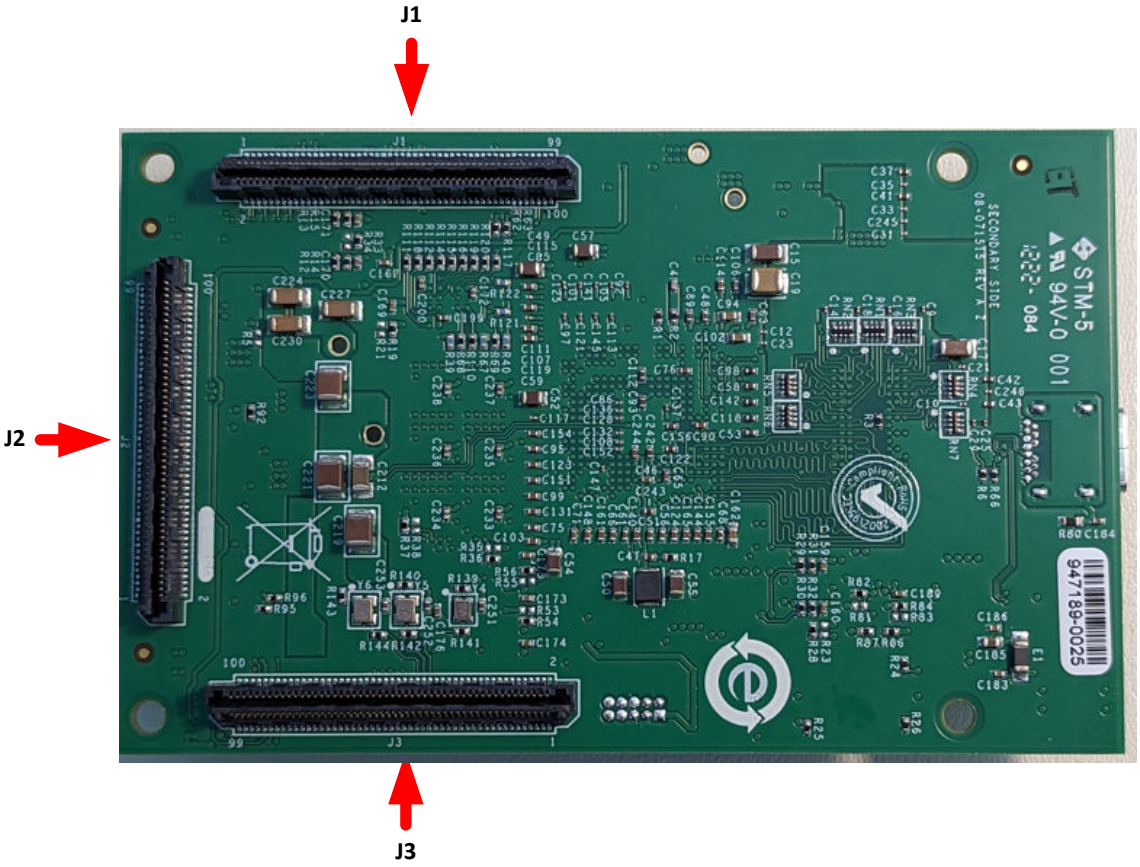

Figure 3-9: Connector Locations Bottom View

JTAG (P6)

The JTAG header provides debug connectivity for the processor. This is a 0.05" shrouded through-hole connector from SAMTEC (SHF-105-01-L-D-SM-K). This connector mates with ICE- 1000, ICE-2000, and any newer Analog Devices emulators. For more information, see Debug Interface

USB Type C Connector (P1)

USB Type C Power Delivery for powering the SoM when JP1 is set to position 1-2. And USB to UART signals to Silicon Labs CP2102N-A02-GQFN28

Part Description	*Manufacturer*	*Part Number*
USB Type C	MOLEX	1054500101
Mating Cable		
USB Type C	ANY	ANY

SoM Interface Connection (J1, J2 and J3)

The SoM Interface consists of three SAMTEC high speed connectors that provide the DSP peripheral signals for use with a plug in baseboard. The *SoM Connector* figure shows the connector locations on the back of the board.

These signals are based upon the peripheral signal needs, which allows multiple DSPs to be used with this connection. These connectors are self-mating and the pinout here reflects the connectors on the EV-SC594-SOM.

The *SoM Interface A Connector (J1)*, *SoM Interface B Connector (J2)*, and *SoM Interface C Connector (J3)* tables show the signal associated with each pin on the connectors.

Table 3-5: SoM Interface A Connector (J1)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND1	21	DAI0_PIN10	41	DAI0_PIN20	61	NU	81	SPI3_MOSI
2	GND2	22	DAI1_PIN10	42	DAI1_PIN20	62	USB_D2	82	~USB_RESET
3	DAI0_PIN01	23	DAI0_PIN11	43	GND3	63	NU	83	~SPI3_SEL1
4	DAI1_PIN01	24	DAI1_PIN11	44	GND4	64	USB_D3	84	GPIO6
5	DAI0_PIN02	25	DAI0_PIN12	45	GND5	65	NU	85	GPIO5
6	DAI1_PIN02	26	DAI1_PIN12	46	GND6	66	USB_D4	86	GPIO7
7	DAI0_PIN03	27	DAI0_PIN13	47	HADC_VIN0	67	NU	87	GND9
8	DAI1_PIN03	28	DAI0_PIN13	48	HADC_VIN4	68	USB_D5	88	CNT_UD
9	DAI0_PIN04	29	DAI0_PIN14	49	HADC_VIN1	69	NU	89	MLB_CLKP
10	DAI1_PIN04	30	DAI1_PIN14	50	HADC_VIN5	70	USB_D6	90	CNT_ZM
11	DAI0_PIN05	31	DAI0_PIN15	51	HADC_VIN2	71	NU	91	MLB_CLKN
12	DAI1_PIN05	32	DAI1_PIN15	52	HADC_VIN6	72	USB_D7	92	CNT_DG
13	DAI0_PIN06	33	DAI0_PIN16	53	HADC_VIN3	73	NU	93	MLB_SIGP
14	DAI1_PIN06	34	DAI1_PIN16	54	HADC_VIN7	74	USB_NXT	94	GND10
15	DAI0_PIN07	35	DAI0_PIN17	55	GND7	75	NU	95	MLB_SIGN
16	DAI1_PIN07	36	DAI1_PIN17	56	GND8	76	USB_STP	96	MLB_CLK
17	DAI0_PIN08	37	DAI0_PIN18	57	NU	77	SPI3_CLK	97	MLB_DATP
18	DAI1_PIN08	38	DAI1_PIN18	58	USB_D0	78	USB_DIR	98	MLB_SIG
19	DAI0_PIN09	39	DAI0_PIN19	59	NU	79	SPI3_MISO	99	MLB_DATN
20	DAI1_PIN09	40	DAI1_PIN19	60	USB_D1	80	USB_CLK	100	MLB_DAT

Table 3-6: SoM Interface B Connector (J2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND1	21	OSPI_D7	41	TWI2_SDA	61	MSI_D3	81	LINKPORT0_D7
2	GND2	22	SPI1_SEL2b	42	UART2_RXb	62	GND8	82	LINKPORT1_D7
3	SP2_OSPI_MISO	23	SPI2_SEL2b	43	UART0_TXb	63	MSI_D4	83	LINKPORT0_D6

Table 3-6: SoM Interface B Connector (J2) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
4	SPI0_CLK	24	GND3	44	UART2_RTSb	64	CAN0_TX	84	LINKPORT1_D6
5	SP2_OSPI_MOSI	25	GND4	45	UART0_RXb	65	MSI_D5	85	LINKPORT0_D5
6	SPI0_MISO	26	SPI0_RDY	46	UART2_CTSb	66	CAN0_RX	86	LINKPORT1_D5
7	SPI2_OSPI_D2	27	SPI2_OSPI_DQS	47	UART0_RTSb	67	MSI_D6	87	LINKPORT0_D4
8	SPI0_MOSI	28	SPI1_RDY	48	GND6	68	GND	88	LINKPORT1_D4
9	SP2_OSPI_D3	29	NU	49	UART0_CTSb	69	MSI_D7	89	LINKPORT0_D3
10	SPI0_SSb	30	SPI2_RDY	50	GPIO1	70	CAN1_TX	90	LINKPORT1_D3
11	SP2_OSPI_CLK	31	TWI0_SCL	51	GND5	71	GND7	91	LINKPORT0_D2
12	SPI0_SEL2b	32	UART1_TXb	52	GPIO2	72	CAN1_RX	92	LINKPORT1_D2
13	SP2_OSPI_SSb	33	TWI0_SDA	53	NU	73	NU	93	LINKPORT0_D1
14	SPI1_CLK	34	UART1_RXb	54	NU	74	NU	94	LINKPORT1_D1
15	OSPI_D4	35	TWI1_SCL	55	MSI_D0	75	NU	95	LINKPORT0_D0
16	SPI1_MISO	36	UART1_RTSb	56	MSI_CLK	76	NU	96	LINKPORT1_D0
17	OSPI_D5	37	TWI1_SDA	57	MSI_D1	77	NU	97	LINKPORT0_ACK
18	SPI1_MOSI	38	UART1_CTSb	58	MSI_CMD	78	NU	98	LINKPORT1_ACK
19	OSPI_D6	39	TWI2_SCL	59	MSI_D2	79	GND9	99	LINKPORT0_CLK
20	SPI1_SSb	40	UART2_TXb	60	MSI_CDb	80	GND10	100	LINKPORT1_CLK

Table 3-7: SoM Interface C Connector (J3)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND1	21	ETH0_RXCLK_REFCLK	41	GND7	61	PPI_D05	81	PPI_D15
2	GND2	22	GND4	42	CLK1	62	PPI_D17	82	~UART3_RX
3	ETH0_MDIO	23	ETH0_RXCTL_CRS	43	PPI_CLK	63	PPI_D06	83	PPI_D16
4	ETH1_MDIO	24	ETH0_PTPCLKIN0	44	CLK2	64	PPI_D18	84	~UART3_RTS
5	ETH0_MDC	25	GND3	45	PPI_FS1	65	PPI_D07	85	GND11
6	ETH1_MDC	26	ETH0_PTPAUX-IN0	46	GND8	66	PPI_D19	86	~UART3_CTS
7	ETH0_MD_INT	27	ETH0_TXD3	47	PPI_FS2	67	PPI_D08	87	VDD_EXT
8	ETH1_RXD1	28	ETH0_PTPPPS0	48	JTG0_TMS/ SWDIO	68	PPI_D20	88	SYS_FAULT

Table 3-7: SoM Interface C Connector (J3) (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
9	ETH0_GPIO_1	29	ETH0_TXD2	49	PPI_FS3	69	PPI_D09	89	VDD_VREF
10	ETH1_RXD0	30	ETH0_PTPPPS1	50	JTG0_TCK/ SWCLK	70	PPI_D21	90	GND12
11	ETH0_GPIO_2	31	ETH0_TXD1	51	PPI_D00	71	PPI_D10	91	VDD_A
12	ETH1_TXEN	32	ETH0_PTPPPS2	52	JTG0_TDO/SW0	72	PPI_D22	92	VDD_DMC
13	ETH0_RXD3	33	ETH0_TXD0	53	PPI_D01	73	PPI_D11	93	VDD_INT
14	ETH1_TXD0	34	ETH0_PTPPPS3	54	JTG0_TDI	74	PPI_D23	94	$\overline{\text{SYS\_HWRST}}$
15	ETH0_RXD2	35	ETH0_TXCLK	55	PPI_D02	75	PPI_D12	95	PWR_SEQ_GOOD
16	ETH1_TXD1	36	GND5	56	$\overline{\text{JTG0\_TRST}}$	76	GND10	96	$\overline{\text{SoM\_Reset}}$
17	ETH0_RXD1	37	ETH0_TXEN	57	PPI_D03	77	PPI_D13	97	VDD1
18	ETH1_CRS	38	SYS_CLKOUT	58	$\overline{\text{TARGET\_RESET}}$	78	ETH1_R EFCLK	98	VSS1
19	ETH0_RXD0	39	GND6	59	PPI_D04	79	PPI_D14	99	VDD2
20	ETH1_INTb	40	AUDIO_CLK	60	GND9	80	UART3_ TX	100	VSS2

Table 3-8: Mating Connector

Part Description	*Manufacturer*	*Part Number*
100-pin, 0.64 mm	SAMTEC	LSS-150-01-L-DV-A-K
Mating Connector		
100-pin, 0.64 mm	SAMTEC	LSS-150-01-L-DV-A-K