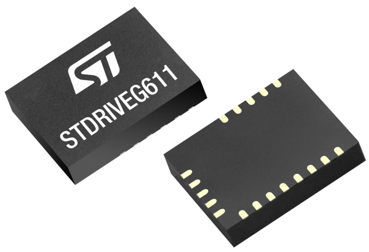
STDRIVEG611

Datasheet

High voltage and high-speed half-bridge gate driver for GaN power switches



QFN 4 x 5 x 1 mm

Product status link
STDRIVEG611

Product label
SUSTAINABLE TECHNOLOGY

Features

- High voltage rail up to 600 V
- dV/dt transient immunity ±200 V/ns
- Driver with separated sink and source path for optimal driving:
  - 2.4 A and 1.2 Ω sink
  - 1.0 A and 3.7 Ω source
- High-side and low-side linear regulators for 6 V gate driving voltage
- Fast high-side startup time: 5 µs
- 45 ns propagation delay, 15 ns minimum output pulse
- High switching frequency (> 1 MHz)
- Embedded 600 V bootstrap diode
- Full support of GaN hard-switching operation
- Comparator for overcurrent detection with Smart Shutdown
- UVLO function on VCC, V_{HS}, and V_{LS}
- Separated logic inputs and shutdown pin
- Fault pin for overcurrent, overtemperature and UVLO reporting
- Stand-by function for low consumption mode
- Separated PGND for Kelvin source driving and current shunt compatibility
- 3.3 V to 20 V compatible inputs with hysteresis and pull-down

Applications

- Motor driver for home appliances, pumps, and compressors
- Factory automation, servo, and industrial drives
- E-bikes and power tools
- Class D audio amplifiers
- DC/DC and resonant converters, PFC, battery charger and adapters

Description

The STDRIVEG611 is a high-voltage half-bridge gate driver for N-channel Enhancement Mode GaN.

The high-side driver section is designed to stand a voltage rail up to 600 V and can be easily supplied by the integrated bootstrap diode.

High current capability, short propagation delay with excellent delay matching, and integrated LDOs make the STDRIVEG611 optimized for driving high-speed GaN.

The STDRIVEG611 features supply UVLOs tailored to hard switching applications, interlocking to avoid cross-conduction conditions and an overcurrent comparator with SmartSD.

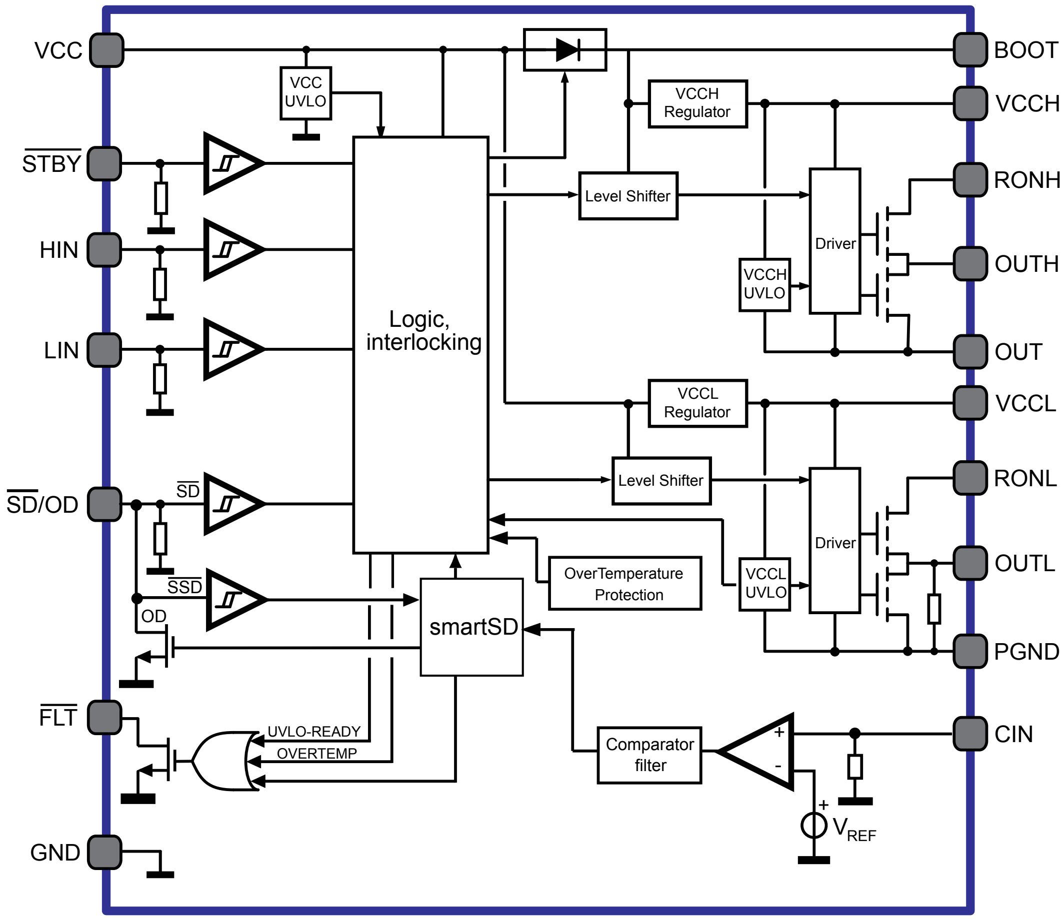
The input pins extended range allows easy interfacing with controllers. A standby pin allows to reduce the power consumption during inactive periods or burst mode.

The STDRIVEG611 operates in the industrial temperature range, -40 °C to 125 °C.

The device is available in a compact QFN 4x5x1 mm package with 0.5 mm pitch.

1 Block diagram

Figure 1. **STDRIVEG611 block diagram**



2 Typical application schematics

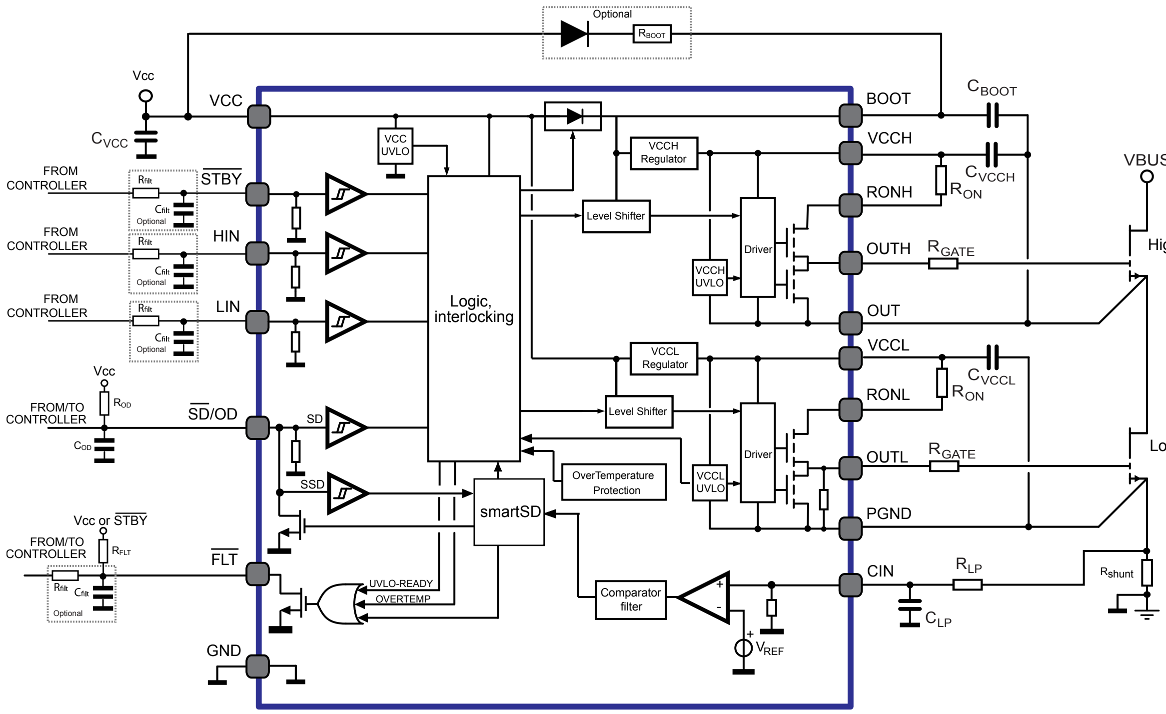


Figure 2. Typical application schematic

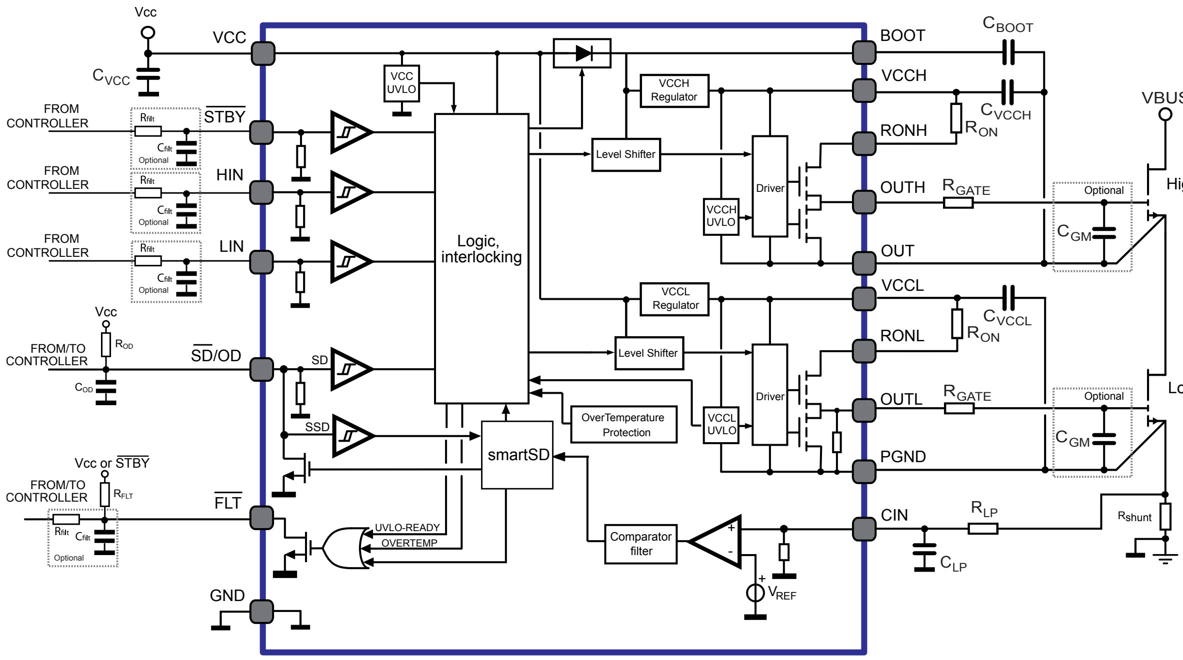


Figure 3. Typical motor control application schematic with slow dV/dt

3 Pin description

Figure 4. **STDRIVEG611 pin connection**

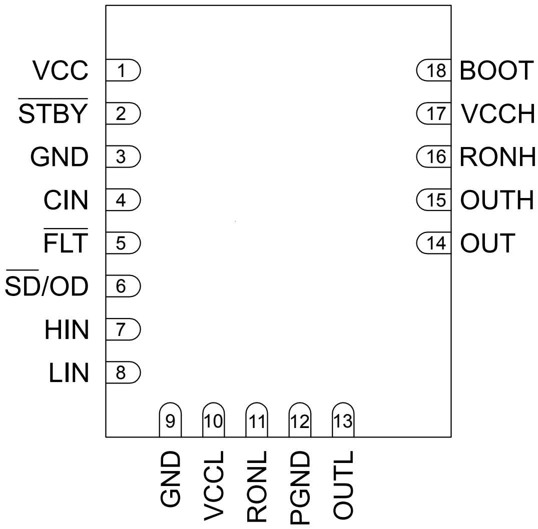


Table 1. **STDRIVEG611 pin list**

Pin N.	Name	Type	Function
1	VCC	Power	Supply voltage of logic section. A small bypass capacitor (100 nF typ.) very close to the pin is required to get a clean bias voltage for the signal part of the IC. The large bulk capacitor that is normally used to supply the controller is sufficient to supply the STDRIVEG611 as well: if not present, a value larger than 2.2 μF is suggested. The input of the low-side driver regulator is internally connected to this pin.
2	$\overline{\text{STBY}}$	Input	Standby mode activation pin. Setting this pin to GND, the IC enters a low consumption mode to facilitate the design of low consumption topologies. The internal pull-down resistor is there to avoid uncertain voltage application when IC is not biased.
3, 9	GND	Power	Ground pins. Common potential of the Logic section of the device. These pins have both an electrical and thermal purpose: tying these pins to a proper copper area effectively enhances power dissipation (typically required only on high frequency applications).
4	CIN	Input	Comparator input pin for SmartSD. In case of triggering, both GaN are immediately turned off and $\overline{\text{SD}}$/OD is pulled low. Connect to GND if not used.
5	$\overline{\text{FLT}}$	Output	Fault signaling pin. An open drain MOSFET is turned on to pull the $\overline{\text{FLT}}$ pin down when UVLO, standby, comparator, or overtemperature protection are active. Connect to GND if not used.
6	$\overline{\text{SD}}$/OD	Input/ Output	Shutdown input (active low) / open drain output for comparator with smartSD. When this pin is pulled to GND, the IC immediately interrupts the switching activity defined by LIN and HIN. When CIN exceeds the threshold, SmartSD interrupts the switching activity and pulls low the $\overline{\text{SD}}$/OD pin. Once the overcurrent ends, the open drain is released. The internal pull-down resistor is there to avoid uncertain voltage application when IC is not biased.
7	HIN	Input	High-side logic input pin. Driving pulses to control the high-side switch can be applied to this pin. A Schmitt trigger comparator, 20 V tolerant, buffers the input signal before driving level shifters.
8	LIN	Input	Low-side logic input pin. Driving pulses to control the low-side switch can be applied to this pin. A Schmitt trigger comparator, 20 V tolerant, buffers the input signal before driving level shifters.
10	VCCL	Power	Output of the linear regulator that supplies the output stage of the low-side driver. A ceramic capacitor equal or greater than 47 nF (X7R, 16 V) must be placed as close as possible between this pin and PGND.
11	RONL	Output	A resistor connected between this pin and VCCL sets the turn-on resistor source current of the low-side driver. Mounting the resistor as close as possible to the RONL pin optimizes the operation of the driver.

Pin N.	Name	Type	Function
12	PGND	Power	Reference potential of low-side driver, to be connected to low-side GaN Kelvin source and VCCL capacitor.
13	OUTL	Output	Low-side driver output. To be connected to the low-side gate through the turn-off resistor. Sink/ source gate current flows through this pin.
14	OUT	Power	Reference potential of high-side driver, to be connected to high-side GaN Kelvin source, BOOT, and VCCH capacitors.
15	OUTH	Output	High-side driver output. To be connected to the high-side gate through the turn-off resistor. Sink/ source gate current flows through this pin.
16	RONH	Output	A resistor connected between this pin and VCCH sets the turn-on resistor source current of the high-side driver. Mounting the resistor as close as possible to the RONH pin optimizes the operation of the driver.
17	VCCH	Power	Output of linear regulator that supplies the output stage of high-side driver. A ceramic capacitor equal or greater than 47 nF (X7R, 16 V) must be placed as close as possible between this pin and OUT.
18	BOOT	Power	Supply voltage of high-side floating driver. A ceramic capacitor equal or greater than 47 nF (X7R, 50 V) must be placed as close as possible between this pin and OUT. The input of the high-side driver regulator is internally connected to this pin.

4 Device ratings

4.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 2 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages referred to ground pins unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
VCC	Logic supply voltage		-0.3 to 21	V
PGND	Low-side driver ground vs. logic ground	VCC = 14 V	-7 to 7	V
$V_{VCC\text{-}PGND}$	Logic supply vs. low-side driver ground		-0.3 to 21	V
V_{VCCL_max}	Regulated low-side driver supply vs. logic ground		-0.3 to 21	V
V_{LS}	Regulated low-side driver supply voltage (1) (2)		-0.3 to 21	V
I_{LS_OUT}	Low-side regulator maximum current (1)	(2)	Self-limited	A
$V_{VCC\text{-}VCCL\_max}$	Maximum low-side dropout voltage		-0.3 to self-regulated	V
V_{OUTL_max}	Low-side output to PGND voltage	DC values	-0.3 to VCCL+0.3	V
V_{RONL_max}	Low-side turn-on resistor pin max. voltage		V_{OUTL}-0.3 to VCCL+0.3	V
V_{BOOT}	BOOT pin voltage referred to GND		-0.3 to 621	V
V_{BO}	High-side regulator input voltage (1)		-0.3 to 21	V
V_{HS}	Regulated high-side driver supply voltage (1) (2)		-0.3 to 21	V
I_{HS_OUT}	High-side regulator maximum current (1)	(2)	Self-limited	A
$V_{BOOT\text{-}VCCH\_max}$	Maximum high-side dropout voltage		-0.3 to self-regulated	V
V_{OUTH_max}	High-side output to OUT voltage	DC values	-0.3 to VCCH+0.3	V
V_{RONH_max}	High-side turn-on resistor pin max. voltage		V_{OUTH}-0.3 to VCCH+0.3	V
dV_{OUT}/dt_{max}	Maximum OUT voltage slew rate (3)		200	V/ns
CIN	Comparator input voltage		-0.3 to 21	V
V_{in_max}	Logic inputs voltage range (LIN, HIN, $\overline{SD}$/OD, $\overline{STBY}$, $\overline{FLT}$)		-0.3 to 21	V
I_{FLT_max}	Maximum $\overline{FLT}$ pin current (DC inward)	VCC = 7 V	10	mA
I_{OD_max}	Maximum $\overline{SD}$/OD pin current (DC inward)	VCC = 12 V	10	mA
T_J	Junction temperature		-40 to 150	°C
T_{stg}	Storage temperature		-55 to 150	°C
ESD	HBM (Human Body Model)	ANSI/ESDA/JEDEC JS-001-2017	2 (4)	kV
	CDM (Charged Device Model)	ANSI/ESDA/JEDEC JS-002-2018	1	kV

1. *V_{LS} = $V_{VCCL\text{-}PGND}$, V_{HS} = $V_{VCCH\text{-}OUT}$, V_{BO} = $V_{BOOT\text{-}OUT}$.*
2. *The internal low-side and high-side voltage regulators are not intended to be connected to external load nor voltage sources.*
3. *Range estimated by characterization on a limited number of samples, not tested in production.*
4. *High voltage pin 18 vs. GND has 1500 V rating*

4.2 Recommended operating conditions

All voltages referred to ground pins unless otherwise specified. The junction temperature must be maintained within recommended operating conditions with proper thermal design.

Table 3. Recommended operating conditions

Symbol	Parameter	Note	Min.	Max.	Unit
VCC	Logic supply voltage		10.7	18	V
$V_{VCC-PGND}$	Logic supply voltage vs. PGND		7.5	20	V
PGND	Low-side driver ground		-3	3	V
V_{BO}	$V_{BOOT-OUT}$ pin voltage	(1)	7.5	20	V
V_{OUT}	DC output voltage		-9.3 (2)	520	V
	Transient output voltage	t_{trans} < 1 ms		600	V
VCCL	Low-side driver voltage vs. GND		3		V
CIN	Comparator input voltage		0	15	V
V_i	Logic inputs voltage range		0	20	V
C_{VCCH}, C_{VCCL}	Driver supply voltage bypass capacitors (3)		47	470	nF
C_{BOOT}	High-side driver linear regulator input capacitors (4)		C_{VCCH}	3300	nF
t_{INmin}	Minimum duration of input pulse		50		ns
f_{SW}	Switching frequency (5)	Duty cycle = 50%		2	MHz
T_{J-op}	Junction temperature		-40	125	°C

1. *V_{BOOT} = $V_{BOOT-GND}$ must be ≥ 5 V to propagate high-side commands.*
2. *V_{BO} = 20 V, VCC = 10.7 V*
3. *X7R, 16 V, Ceramic capacitor having ESR lower or equal to 50 mΩ.*
4. *X7R, 50 V, Ceramic capacitor having ESR lower or equal to 50 mΩ.*
5. *Actual limit depends on power dissipation constraints.*

4.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(J-A)}$	Thermal resistance junction-to-ambient (1)	85	°C/W
$R_{th(J-A)}$	Thermal resistance junction-to-ambient (2)	110	°C/W

1. *The thermal resistance is obtained simulating the device mounted on a 2s2p (4 layer) FR4 board according to JESD51-7 without PCB thermal vias.*
2. *The thermal resistance is obtained simulating the device mounted on a 1s0p (1 layer) FR4 board according to JESD51-3.*

5 Electrical characteristics

Testing conditions: T_J = 25 °C, VCC = V_{BO} = $\overline{SD}$/OD = $\overline{STBY}$ = 12 V, $\overline{FLT}$ = floating, RONL = VCCL, RONH = VCCH, OUT = PGND = CIN = GND, C_{VCCH} = C_{VCCL} = 47 nF (X7R,16 V), C_{BOOT} = 47 nF (X7R, 50 V).

All voltages referred to GND, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic section supply						
VCC_{thON}	VCC UVLO turn-ON threshold		9.5	10	10.6	V
VCC_{thOFF}	VCC UVLO turn-OFF threshold		9.0	9.5	10.1	V
VCC_{hys}	VCC UV hysteresis		0.3	0.5	0.7	V
I_{QVCC}	VCC quiescent supply current	$\overline{STBY}$ = $\overline{SD}$/OD = 5 V; LIN = HIN = 0 V; OUT = 15 V		900	1200	µA
		LIN = $\overline{STBY}$ = $\overline{SD}$/OD = 5 V; HIN = 0 V; OUT = 15 V		1020	1350	µA
I_{QVCCU}	VCC undervoltage supply current	VCC = 7.0 V		570	760	µA
I_{SBVCC}	VCC standby supply current	$\overline{STBY}$ = 0 V		500	650	µA
I_{SVCC}	VCC switching supply current	$\overline{STBY}$ = $\overline{SD}$/OD = 5 V, V_{BO} = 15 V; LIN = ¬ HIN; f_{SW} = 500 kHz, D = 50% OUTL load 330 pF		3	3.5	mA
$t_{startup}$	VCC startup time from VCC = 10.5 V to OUTL high	LIN = $\overline{STBY}$ = $\overline{SD}$/OD = 5 V; HIN = 0 V			12	µs
Gate driver voltage regulators VCCL (V_{LS}) and VCCH (V_{HS})						
V_{HS} V_{LS}	VCCx regulator output voltage	I_{VCCx} < 10 mA_{DC}	5.55	6	6.45	V
		T_J = -40 °C to +125 °C (1)	5.4		6.6	V
V_{HSthON} V_{LSthON}	VCCx UVLO turn-on voltage		4.45	4.8	5.15	V
		T_J = -40 °C to +125 °C (1)			5.25	V
$V_{HSthOFF}$ $V_{LSthOFF}$	VCCx UVLO turn-off voltage		4.3	4.65	4.95	V
		T_J = -40 °C to +125 °C (1)	4.2			V
$V_{HSthHYS}$ $V_{LSthHYS}$	VCCx UVLO hysteresis			0.2		V
V_{DROP_H}	High-side regulator drop-out voltage	BOOT = 12 V; OUT = 6 V; I_{VCCH} = 10 mA			0.6	V
High-side driver section						
I_{QBO}	V_{BO} quiescent supply current	$\overline{STBY}$ = $\overline{SD}$/OD = 3.3 V; LIN = HIN = 0 V; V_{BO} = 12 V		240	340	µA
		HIN = $\overline{STBY}$ = $\overline{SD}$/OD = 3.3 V; LIN = 0 V; V_{BO} = 12 V		270	360	µA
I_{SBO}	V_{BO} switching supply current	$\overline{SD}$/OD = $\overline{STBY}$ = 3.3 V; OUT = 0 V; V_{BOOT} = 12 V HIN f_{SW} = 500 kHz, D = 50% OUTH load 330 pF		3.1	3.8	mA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{HSstart}$	High-side startup time	LIN = 3.3 V & OUT= 0 V; D_{BOOT} = STTH1R06, R_{BOOT}= 2.2 Ω From V_{BO} > 8 V to OUTH enable			5	µs
I_{LK}	High voltage leakage current	BOOT = OUT = 600 V			11	µA
R_{DBOOT}	Bootstrap diode on-resistance	LIN = 3.3 V; HIN = 0 V; $V_{VCC-BOOT}$ = 0.5 V		120		Ω
Output driving buffers						
I_{SO}	Peak source current		0.75	1.05	1.3	A
		T_J = -40 °C to +125 °C (1)	0.55		1.6	
I_{SI}	Peak sink current		1.9	2.4	3.0	A
		T_J = -40 °C to +125 °C (1)	1.4		3.7	
R_{SO}	Source R_{DSon}	I = 10 mA	3.0	3.7	4.5	Ω
		T_J = -40 °C to +125 °C (1)	2.2		7.0	
R_{SI}	Sink R_{DSon}	I = 10 mA	0.85	1.2	1.55	Ω
		T_J = -40 °C to +125 °C (1)	0.7		2.2	
R_{BLEED}	Low-side gate bleeder	VCCL = VCC = 0 V, PGND = GND, OUTL = 0.1 V	75	100	125	kΩ
Logic inputs and timings						
V_{ih}	High level logic threshold voltage		2	2.27	2.5	V
		T_J = -40 °C to +125 °C (1)			2.7	
V_{il}	Low level logic threshold voltage		1.1	1.31	1.45	V
		T_J = -40 °C to +125 °C (1)	0.8			
V_{ihys}	Logic input threshold hysteresis		0.7	0.96	1.2	V
V_{SSD}	SmartSD unlatch threshold		0.5	0.65	0.8	V
		T_J = -40 °C to +125 °C (1)			0.9	
I_{INh}	LIN, HIN logic '1' input bias current	LIN, HIN = 3.3 V	15	22	36	µA
I_{INl}	LIN, HIN logic '0' input bias current	LIN, HIN = 0 V			1	µA
R_{PD_IN}	LIN, HIN pull-down resistor	LIN, HIN = 3.3 V	90	150	220	kΩ
I_{SDh}	$\overline{SD}$/OD logic '1' input bias current	$\overline{SD}$/OD = 3.3 V	7	10	15	µA
I_{SDl}	$\overline{SD}$/OD logic '0' input bias current	$\overline{SD}$/OD = 0 V			1	µA
R_{PD_SD}	$\overline{SD}$/OD pull-down resistor	$\overline{SD}$/OD = 3.3 V	220	330	450	kΩ
R_{ON_OD}	$\overline{SD}$/OD on-resistance	$\overline{SD}$/OD = 400 mV; CIN = 2 V	25	40	58	Ω
I_{OL_SD}	$\overline{SD}$/OD low level sink current		7	10	16	mA
t_{OD_fall}	$\overline{SD}$/OD loaded fall time	C_L= 10 nF; R_{PU} = 10 kΩ to 5 V 90% to 10 % $\overline{SD}$/OD		0.75		µs
I_{STBYh}	$\overline{STBY}$ logic '1' input bias current	$\overline{STBY}$ = 3.3 V	7	10	15	µA
I_{STBYl}	$\overline{STBY}$ logic '0' input bias current	$\overline{STBY}$ = 0 V			1	µA
R_{PD_STBY}	$\overline{STBY}$ pull-down resistor	$\overline{STBY}$ = 3.3 V	220	330	450	kΩ
R_{ON_FLT}	$\overline{FLT}$ on-resistance	V_{FLT} = 400 mV, VCC = 12 V	60	80	135	Ω

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{ON_FLT}	$\overline{FLT}$ on-resistance	V_{FLT} = 400 mV, VCC = 3.3 V	90	145	200	Ω
I_{OL_FLT}	$\overline{FLT}$ low level sink current	V_{FLT} = 400 mV	3	5	7	mA
I_{FLTh}	$\overline{FLT}$ high level bias current (when off)	V_{FLT} = 3.3 V			1	µA
I_{FLTl}	$\overline{FLT}$ low level bias current (when off)	V_{FLT} = 0 V			1	µA
$V_{VCC\text{-}FLT}$	Min VCC voltage forcing low				3.3	V
t_{Don_L}	LIN to OUTL turn-on propagation delay	$\overline{SD}$/OD = $\overline{STBY}$ = 3.3 V; t_{PULSE} > 120 ns	30	45	60	ns
t_{Doff_L}	LIN to OUTL turn-off propagation delay		30	45	60	ns
t_{Don_H}	HIN to OUTH turn-on propagation delay		30	45	60	ns
t_{Doff_H}	HIN to OUTH turn-off propagation delay		30	45	60	ns
MT	LIN, HIN propagation delay matching time [2]	$\overline{SD}$/OD = $\overline{STBY}$ = 3.3 V; t_{PULSE} > 120 ns;		0	10	ns
t_{INmin}	LIN, HIN minimum input pulse width	LIN, HIN pulse low/high/low		15	35	ns
		T_J = -40 °C to +125 °C [1]			40	ns
t_r	GL / GH rise time	C_L= 2.2 nF [1]		22		ns
t_f	GL / GH fall time			11		ns
t_{SDon}	$\overline{SD}$/OD to OUTx turn-on propagation delay	LIN or HIN = $\overline{STBY}$ = 3.3 V; t_{PULSE} > 120 ns;	30	45	65	ns
t_{SDoff}	$\overline{SD}$/OD to OUTx turn-off propagation delay	LIN or HIN = $\overline{STBY}$ = 3.3 V; t_{PULSE} > 120 ns;	30	45	65	ns
$t_{STBYoff}$	Standby to OUTx turn-off propagation delay	$\overline{STBY}$ = 3.3 V to 0 V	30	45	65	ns
t_{STBY_FLT}	Standby enter signaling to $\overline{FLT}$	$\overline{STBY}$ = 3.3 V to 0 V, $\overline{FLT}$ 10 kΩ pull up to 5 V		0.9	2	µs
t_{WU}	Wake up time from standby	$\overline{STBY}$ = 0 V to 3.3 V, LIN = 3.3 V; *Time from $\overline{STBY}$ rising to OUTL = high*			5	µs
t_{WU_FLT}	Standby end signaling to $\overline{FLT}$	$\overline{STBY}$ = 0 V to 3.3 V, $\overline{FLT}$ = 10 kΩ pull up to 5 V; *Time from $\overline{STBY}$ rise to V_{FLT} = 0.5 V*			5	µs
Comparator protection						
CIN_{th}	Comparator threshold		350	400	450	mV
R_{PD_CIN}	CIN pull-down resistor	CIN = 1 V	75	100	125	kΩ
$t_{CIN\text{-}OUT}$	Comparator delay to half-bridge output	CIN 0 V to 0.8 V: OUTH, OUTL 90%		170	220	ns
$t_{CIN\text{-}OD}$	Comparator delay to $\overline{SD}$/OD	CIN 0 V to 0.8 V: $\overline{SD}$/OD 90% (10 kΩ to 5 V)		140	190	ns
$t_{CIN\text{-}FLT}$	Comparator delay to $\overline{FLT}$	CIN 0 V to 0.8 V: $\overline{FLT}$ 90% (10 kΩ to 5 V)		140	190	ns
$t_{CINfilter}$	Comparator input filter	CIN pulse 0 - 0.8 V	55	90	125	ns
Overtemperature protection						
T_{TSD}	Shutdown temperature	[1]	150	175	200	°C

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{HYS}	Temperature hysteresis	(1)	17	20	23	°C
t_{TSD}	OT protection enabling time after $\overline{STBY}$ = high	(1)			20	µs

1. *Not tested in production: value by characterization on a limited number of samples.*
2. *MT = max (| t_{Don_L} - t_{Doff_L} |, | t_{Don_H} - t_{Doff_H} |, | t_{Doff_L} - t_{Don_H} |, | t_{Doff_H} - t_{Don_L} |)*

5.1 Characterization figures

Figure 5. Timing definitions

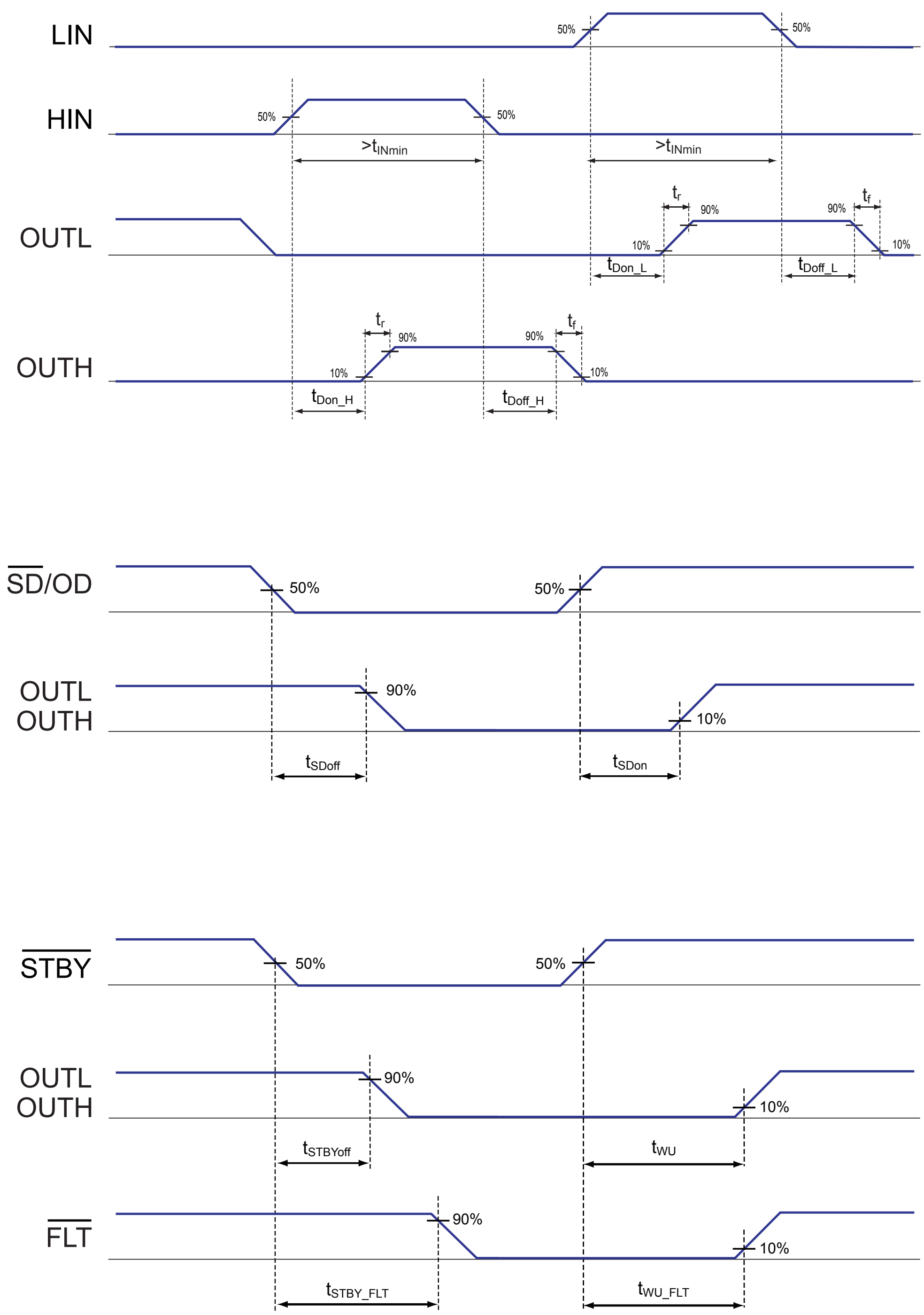


Figure 6. I_{SVCC} **vs frequency (high range)**

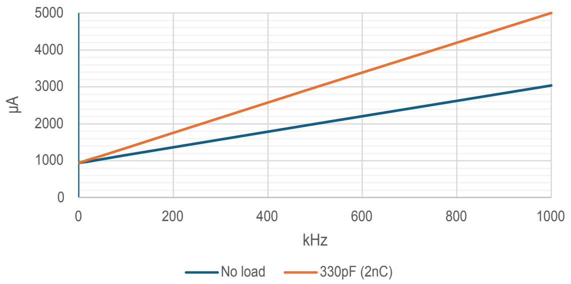


Figure 7. I_{SVCC} **vs frequency (low range)**

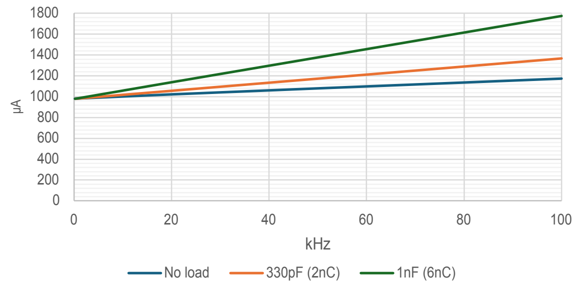


Figure 8. I_{SBO} **vs frequency (high range)**

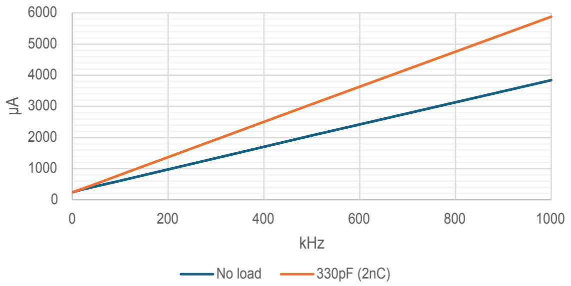
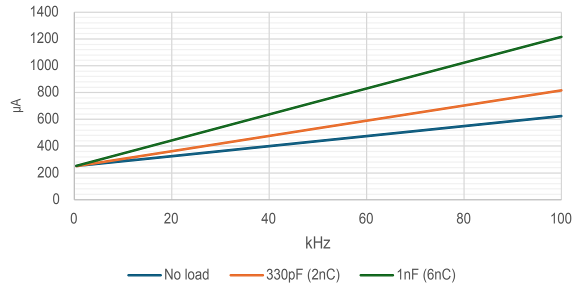


Figure 9. I_{SBO} **vs frequency (low range)**

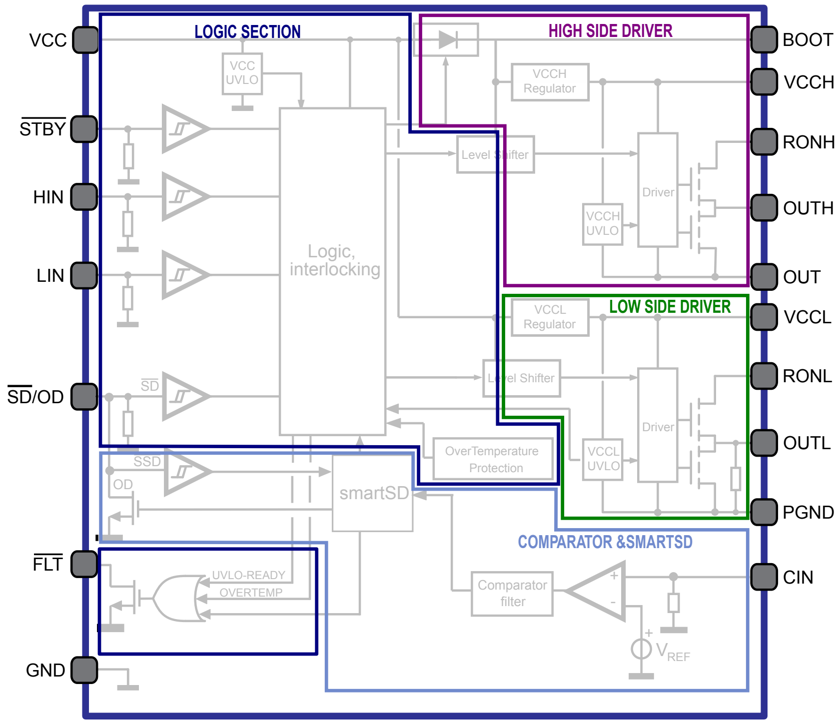


6 Device description

6.1 Device structure

Figure 10 is a simplified version of the block diagram of STDRIVEG611. It consists of basic structures described in the following sections.

Figure 10. STDRIVEG611 simplified block diagram



6.1.1 Logic section

This section receives the input signals, manages the system protections (UVLOs, comparator and overtemperature), and transfers the input pulses to relevant drivers through level shifters.

It is electrically referred to the GND pin and supplied by the VCC pin.

6.1.2 Low-side driver

This block receives input pulses from the logic section through the level shifter and provides driving action to the low-side GaN transistor.

It is electrically referred to PGND, that must be connected to the source (preferably Kelvin) of the low-side GaN transistor.

GaN V_{GS} sink current can be tuned with the R_{GATE} resistor placed between the OUTL and GaN gate. Source current can be tuned with the R_{ON} resistor between VCCL and RONL. Sink path impedance is the sum of R_{GATE} and driver R_{SI}, while source path impedance is the total of R_{ON}, R_{GATE}, and driver R_{SO}. Tuning R_{ON} is typically done to adjust hard turn-on dV/dt. Tuning R_{GATE} is typically done to eventually dump V_{GS} ringing at turn-off, to adjust hard turn-off dV/dt while avoiding induced turn-on at high-side hard turn-on.

Low-side driver circuitry is supplied by VCC, while an integrated voltage regulator tightly stabilizes the supply voltage of the output stage of the driver (V_{LS}). A UVLO comparator interrupts the half-bridge activity if the regulator's output voltage is insufficient for a proper GaN's driving. See Section 6.4.2 for a detailed LS UVLO protection description.

The low-side driver has been designed to allow the use of current sense resistors without affecting the applied V_{GS} voltage.

6.1.3 High-side driver

This block receives input pulses from the logic section through the level shifter and provides driving action to the high-side GaN transistor.

It is electrically referred to OUT, that must be connected to the source connection (preferably Kelvin) of the high-side GaN transistor.

GaN V_{GS} sink current can be tuned with the R_{GATE} resistor placed between the OUTH and GaN gate. Source current can be tuned with the R_{ON} resistor between VCCH and RONH. Sink path impedance is the sum of R_{GATE} and driver R_{SI}, while source path impedance is the total of R_{ON}, R_{GATE} and driver R_{SO}. Tuning R_{ON} is typically done to adjust hard turn-on dV/dt. Tuning R_{GATE} is typically done to eventually dump V_{GS} ringing at turn-off, to adjust hard turn-off dV/dt while avoiding induced turn-on at low-side hard turn-on.

High-side driver circuitry is supplied by the voltage present at the BOOT pin, while an integrated fast startup voltage regulator tightly stabilizes the supply voltage of the output stage of the driver (V_{HS}). A UVLO comparator interrupts the high-side GaN activity if the regulator's output voltage is insufficient for a proper GaN's driving. See Section 6.4.4 for detailed HS UVLO protection description.

This section includes an equivalent bootstrap diode, synchronous with low-side on-time, that generates floating supply voltage (V_{BO}), starting from VCC voltage.

6.1.4 Comparator and smart shutdown

The embedded comparator, typically used for overcurrent detection, immediately turns off both GaNs once CIN input exceeds the threshold. The event is signaled to $\overline{SD}$/OD and $\overline{FLT}$ pins.

The smart shutdown (SmartSD) feature allows to automatically keep the switches off for the desired time to cool down the GaN devices while the controller reacts to the overcurrent $\overline{FLT}$ signal.

6.2 Truth table and control inputs

The STDRIVEG611 has four logic inputs to control the high-side and low-side power transistors.

- LIN: low-side driver input, active high;
- HIN: high-side driver inputs, active high.
- $\overline{STBY}$: standby input, active low;
- $\overline{SD}$/OD: shutdown input, active low.

An open drain output is there ($\overline{FLT}$) to communicate externally the operating status of the device.

The $\overline{SD}$/OD pin is also used as an output for the comparator with SmartSD disable time function (see Section 6.6).

Table 6 summarizes the different IC operating modes depending on the Input pin configurations.

Output pin configuration and IC consumption is also reported.

Table 6. Truth table

Mode	INPUTS				OUTPUTS		
	$\overline{STBY}$	$\overline{SD}$/OD	LIN	HIN	OUTL	OUTH	$\overline{FLT}$
Standby	L	X	X	X	L	L	L
Shutdown	H	L	X	X	L	L	H
High-Z	H	H	L	L	L	L	H
Low-side on	H	H	H	L	H	L	H
High-side on	H	H	L	H	L	H	H
Interlocking	H	H	H	H	L	L	H
Overcurrent	H	L (1)	X	X	L	L	L

1. *Forced low from the internal open-drain when CIN > CIN_{th}.*

The logic inputs have internal pull-down resistors to set a defined logic level even in case of high-Z on signal lines. As a result, the transistors are set to off in the case of unconnected input pins.

The front-end of logic inputs consists of a comparator having a fixed threshold and defined hysteresis to guarantee precise and robust level detection. The input pins can accept an input voltage up to 20 V independently from VCC voltage level.

Propagation delays between LIN and HIN input pins to OUTL and OUTH are matched to obtain the best symmetry and minimum pulse width distortion.

The minimum duration of the pulse that can be transferred from LIN and HIN to OUTL and OUTH is t_{INmin}; shorter pulses may be blanked.

The $\overline{FLT}$ open drain pin signals standby, UVLO (VCC and VCCL), overcurrent, and overtemperature status. An external pull-up resistor or source current is required to raise the $\overline{FLT}$ pin signal. The maximum pull-up voltage is 20 V, independent from VCC. When unused, this pin must be connected to GND.

The $\overline{STBY}$ pin is intended to activate standby mode to reduce the IC consumption during long-lasting inactive times or between burst modes. The description of this mode is reported in Section 6.5.

6.3 Gate driving outputs and gate resistors

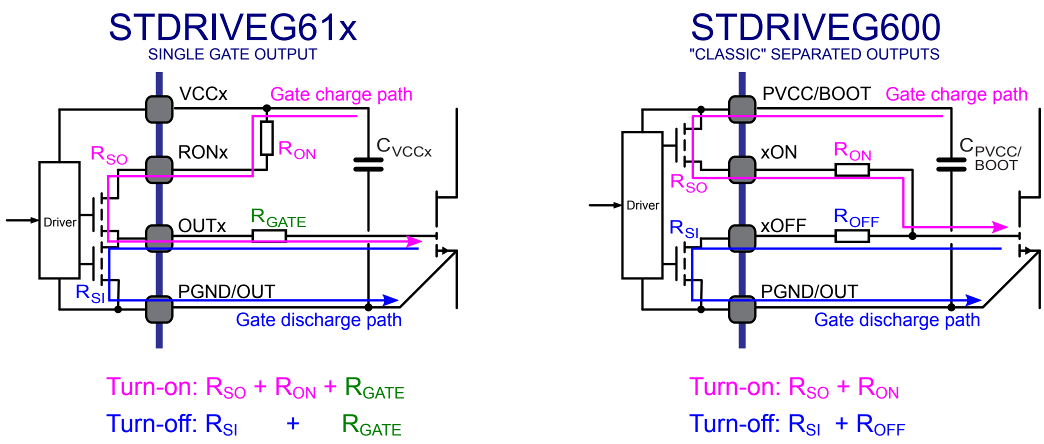
The STDRIVEG611 has a gate driver output architecture enabling turn-on and turn-off impedance differentiation to tune dV/dt and dI/dt avoiding turn-off diode usage. Diode avoidance for turn-on/off differentiation has several benefits:

- bill of material (BOM) reduction;
- gate loop inductance minimization due to smaller geometrical gate loop;
- more effective and faster turn-off with increased induced turn-on margin thanks to diode V_F drop removal.

Effective turn-off is crucial with GaN switches due to low V_{GSth} and turn-off diode is typically not recommended especially with unipolar gate driving (no negative V_{GS} while off).

Similarly to STDRIVEG600 (classic separated output architecture), with the STDRIVEG611 (single gate output architecture) the gate turn-on/off currents can be tuned by external resistors, but those resistors are arranged in different way.

Figure 11. Gate driver output and gate resistor tuning for differentiated turn-on/off



Turn-off path goes through R_{GATE}, so the user shall increase R_{GATE} to slow down turn-off speed.

Increasing R_{GATE} will slow down also turn-on speed since turn-on path goes through R_{GATE} and R_{ON}. The user shall increase R_{ON} to further slowdown turn-on speed.

Thus, turn-on impedance can be only equal or higher than turn-off, as typically found in all applications to avoid induced turn-on phenomenon.

As rule-of-thumb when migrating from “classic” separated output architectures:

- $R_{GATE} \approx R_{OFF(old)}$
- $R_{ON} \approx R_{ON(old)} - R_{GATE}$

In power conversion applications, depending on gate charge, turn-off resistor (R_{GATE}) is typically in the range of 1 to 5 Ω while turn-on resistance sum (R_{GATE} + R_{ON}) is typically in the range of 5 to 300 Ω.

6.3.1 Gate driving network for slow hard-off dV/dt (motor control applications)

While several applications, typically power conversion, tends to make desirable high dV/dt to minimize switching losses, some others, notably motor control ones, could require limiting dV/dt at the expense of higher switching losses.

The main reasons to limit dV/dt in motor control applications are:

- EMI control: to pass regulatory emission masks.
- Motor winding reliability: especially in high voltage applications with long cables, voltage overshoots on motor poles/winding could generate partial discharge phenomena reducing winding lifetime.
- Ball bearing reliability: winding parasitic capacitance to the rotor will generate current peaks during dV/dt toward chassis earth. If those currents flow through classic steel ball bearings, those current can flute bearing rollers and bearing races reducing lifetime.

Typically, the EMI point is the bottleneck to limit dV/dt even if the absence of diode recovery with GaN is now pushing higher the dV/dt limit; motor winding and ball bearing issues are seldom, typically found when pushing further dV/dt limit thanks to shorter cables or with specific motors.

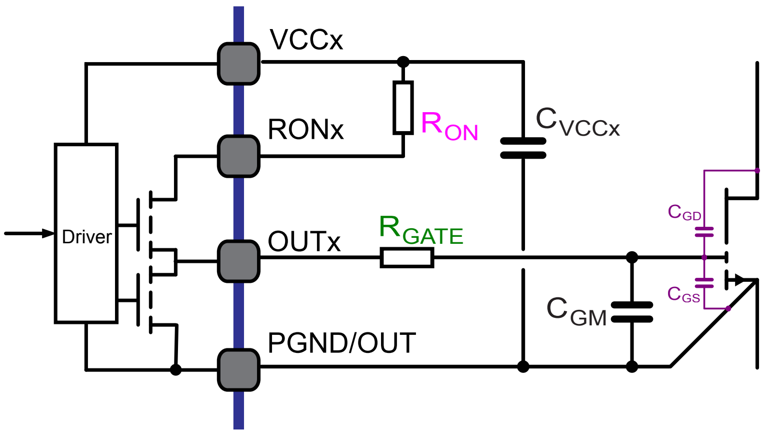
Hard turn-on dV/dt reduction is an easy task by simply increasing R_{ON} resistor.

Hard turn-off dV/dt is generally proportional to load parasitic capacitance (the higher the motor parasitic capacitance, the slower the dV/dt). Depending on motor parasitic capacitance and load current, could be required to slow down turn-off.

In resonant applications, hard-off dV/dt reduction is typically done by adding a discrete capacitor in parallel to GaN C_{DS}. However, adding this capacitor in hard switching applications leads to increase hard-on switching losses loosing some GaN benefits.

In motor control applications with MOSFETs, hard turn-off slow down is typically done by increasing the turn-off resistor. However with GaN this could easily lead to induced turn-on phenomenon unless a specific gate driving network is used as the following one.

Figure 12. Hard-off dV/dt limiting gate driving network



While the GaN is off and during dV/dt generated by the companion GaN, C_{GD} charges C_{GS}. If R_{GATE} has a high value, due to requirement to slow down hard-off dV/dt, V_{GS} could easily exceed V_{GSth} leading to induced turn-on phenomenon.

The higher the C_{GD}/C_{GS} ratio and the lower the V_{GSth}, the most likely the induced turn-on could occur.

Adding the C_{GM} capacitor, the overall C_{GD}/C_{GS} ratio decreases avoiding the induced turn-on phenomenon and enabling hard-off dV/dt reduction increasing R_{GATE}.

The C_{GM} capacitor required to use this technique depends on several factors like GaN characteristics, bus voltage and load current but, as a rule-of-thumb, it is in the range around 3-5 times Q_{GS}/V_{GSth}.

6.4 Supply rails, LDOs, UVLO protections, and bootstrap diode

The STDRIVEG611 is supplied by two rails: VCC, referred to GND, and BOOT referred to OUT.

Integrated LDOs generate supply voltages for low-side and high-side output stages (V_{LS} and V_{HS}). Undervoltage circuitries monitor VCC, V_{LS} and V_{HS}.

An integrated bootstrap diode is there to generate floating supply voltage for the high-side structure.

6.4.1 VCC supply structure and relevant UVLO protection

The VCC pin supplies the logic circuit, the input structure of the low-side driver and the integrated bootstrap structure (D_{BOOT}). Low-ESR ceramic capacitors must be connected as close as possible between VCC and GND (100 nF typ., X7R).

A bulk capacitor is recommended on VCC to deliver the impulsive bootstrap current to charge V_{BO}. A single VCC rail electrolytic capacitor is typically sufficient even with multiple drivers on board while using only the integrated bootstrap diode and the electrolytic capacitor is not too far.

Dedicated bigger low-ESR ceramic VCC capacitors are otherwise recommended, also in the case of an optional external bootstrap diode to minimize VCC dips. An external bootstrap diode could be required for those applications requiring a faster high-side startup time (such as burst mode).

Undervoltage protection is available on the VCC supply pin. A hysteresis sets the turn-off threshold.

When VCC voltage reaches the V_{CCthON} threshold, the device enters normal operation: if V_{LS} is above UVLO level and the $\overline{STBY}$ pin is high, the $\overline{FLT}$ pin is released and the device sets drivers output according to actual input pins; high-side driver supply state is not monitored, therefore the high-side driver generates driving levels when V_{HS} is above UVLO level.

When VCC voltage goes below the $V_{CCthOFF}$ threshold, both high-side and low-side gate driver outputs are forced low and the $\overline{FLT}$ pin is forced low to signal the state to remote controllers.

The minimum VCC voltage that the STDRIVEG611 requires to be able to force the $\overline{FLT}$ pin low is $V_{VCC\text{-}FLT}$.

In hard switching applications, during deadtime and load current flowing out from the OUT node, low-side GaN is in reverse conduction mode (as a freewheeling diode) and the OUT pin becomes negative with several volts below GND.

GaN transistors do not have an intrinsic body diode, which have the benefit of 0 nC recovery charge, but have worse reverse conduction characteristics in respect to MOSFETs. This could lead to two drawbacks if not properly addressed:

- higher GaN dissipation during deadtime, that should be minimized.
- deeper static below-GND voltage on OUT node during deadtime; this could bring BOOT lower than the recommended operating range (BOOT-GND min. 5 V), increasing high-side hard turn-on propagation delay.

To help ensure BOOT in the recommended operating range in hard switching applications (while current is freewheeling in low-side GaN), the VCC supply has a relatively high UVLO threshold. This helps charging and achieving the V_{BO} > (low-side GaN reverse conduction drop +5 V) recommended range in almost all conditions.

Operating with VCC higher than the typical value could be required only in very limited cases where extreme hard switching current transient with very high GaN reverse conduction voltage is foreseen.

6.4.2 V_{LS} supply structure and relevant UVLO protection

The integrated VCCL regulator reduces the input VCC voltage to a regulated V_{LS} (6 V typ.) to drive the gate with a stable and optimized V_{GS} voltage.

Low-side regulator input is VCC pin; regulator output is VCCL pin, referred to PGND. Low-ESR ceramic capacitors must be connected as close as possible between VCCL and PGND (C_{VCCL} min. 47 nF, X7R, 16 V) to obtain a clean supply voltage. A slightly higher C_{VCCL} could be required to minimize V_{LS} ripple when driving high GaN Q_G.

Under recommended operating conditions, VCCL regulator can provide an average current of 10 mA.

A UVLO on V_{LS} is there to prevent unsafe operations of low-side GaN.

When V_{LS} voltage reaches the V_{LSthON} threshold, the device enables the low-side driver normal operation: if no other protection is active, $\overline{FLT}$ pin is released, and the device sets low-side driver output according to actual input pins and high-side driver output according to actual input pins.

When V_{LS} voltage goes below the $V_{LDthOFF}$ threshold, both high-side and low-side gate driver outputs are forced low and the $\overline{FLT}$ pin is forced low to signal this condition to the remote controllers.

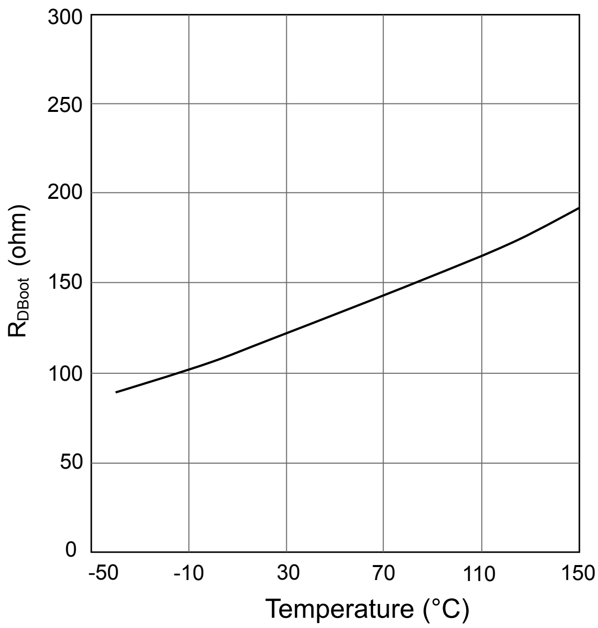
6.4.3 Bootstrap diode

The STDRIVEG611 integrates a bootstrap diode structure connected between VCC and BOOT pins, to supply the high-side floating supply voltage $V_{BOOT\text{-}OUT}$ (or shortly V_{BO}). A very low ESR ceramic capacitor (C_{BOOT} to be selected between 47 nF and 3.3 µF, X7R, 50 V) must be placed as close as possible between the BOOT and OUT pins.

The internal bootstrap structure is synchronous with the low-side to reduce the voltage drop between VCC and V_{BO} to almost zero volts. Its turn-on resistance is reported in the electrical characteristics table as R_{DBOOT}. This integrated structure is characterized by a very low recovery charge and current.

The bootstrap DC characteristics are detailed in Figure 13.

Figure 13. Typical bootstrap diode characteristics



The final voltage drop between VCC and V_{BO} depends on multiple factors like duty cycle, operating frequency, GaN gate charge, GaN leakage, temperature, etc. In case the voltage on V_{BO} is not sufficient for a proper VCCH regulator operation, either increasing the VCC value or using an external bootstrap diode can obtain a correct V_{BO} voltage.

Motor control applications typically do not require an external bootstrap diode but it is allowed in case of specific needs as fast high-side start-up or large bootstrap capacitor to allow very long high side turn-on time.

It is recommended to place a resistor $R_{BOOT} \geq 2.2\ \Omega$ in series with the above mentioned external bootstrap diode to limit the amount of peak charging current. In cases of high side not-zero-current hard switching applications (as motor control), the external bootstrap diode could be subject to high peak current during dead time and peak recovery current at high side turn-on, leading to strong emissions. A higher R_{BOOT} or using the internal bootstrap structure with no recovery current is preferable in these cases. Refer to Section 7.1.1 for further details.

Even if a low R_{BOOT} resistor is allowed, it is know that a low value resistor could increase radiated noise; so it is worth properly selecting the C_{BOOT} capacitor based on applicative requirements. With the same start-up time, the smaller C_{BOOT} capacitor the higher R_{BOOT} minimum resistance or even no external diode requirement. Moreover, the internal bootstrap diode has better dynamic characteristics compared to a discrete one.

6.4.4 V_{HS} supply structure and relevant UVLO protection

The energy stored in the C_{BOOT} capacitor supplies the input circuitry of the high-side driver.

The integrated fast startup VCCH regulator reduces the input V_{BO} voltage to a regulated V_{HS} (VCCH-OUT = 6 V typ.) to drive the gate with a stable and optimized V_{GS} voltage.

The fast startup features a minimized wake-up time especially during intermittent operation (burst mode).

High-side regulator input is the BOOT pin; regulator output is the VCCH pin, referred to OUT. Low-ESR ceramic capacitor must be connected as close as possible between VCCH and OUT (C_{VCCL} min. 47 nF, X7R, 16 V) to obtain a clean supply voltage. A slightly higher C_{VCCH} could be required to minimize V_{HS} ripple when driving high GaN Q_G, but the lower the C_{VCCH} the faster the startup time.

Under recommended operating conditions, VCCH regulator can provide an average current of 10 mA.

A UVLO on V_{HS} is there to prevent unsafe operations of low-side GaN.

When V_{HS} voltage reaches the V_{HSthON} threshold, the high-side driver is enabled to accept turn-on/off commands from the input logic block.

When V_{HS} voltage goes below the $V_{HSthOFF}$ threshold, high-side gate driver output is forced low.

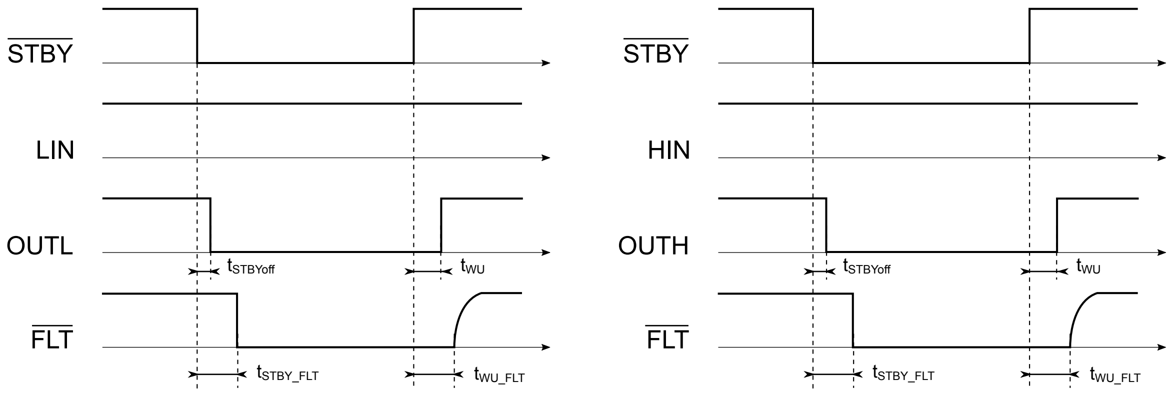
V_{HS} UVLO status is not signaled on the $\overline{\text{FLT}}$ pin and the low-side driver continues to operate according to inputs and other protections.

6.5 Standby

The STDRIVEG611 is designed to reduce the current consumption of both the logic portion and low-side driver when the $\overline{\text{STBY}}$ pin is pulled to GND. Low-side and high-side output are immediately set low to leave the half-bridge in a three-state, while the $\overline{\text{FLT}}$ pin is forced low, and consumption is reduced if the $\overline{\text{STBY}}$ pin is pulled to GND. The overtemperature and the comparator protections are disabled in this operating condition.

Setting the $\overline{\text{STBY}}$ pin high, the device wakes up and operation is restored: the $\overline{\text{FLT}}$ pin is released while driver's outputs are set according to inputs, providing that relevant UVLOs are not active, within t_{WU}.

Figure 14. Standby timings



6.6 Comparator with SmartSD

The STDRIVEG611 integrates a comparator committed to the fault sensing function.

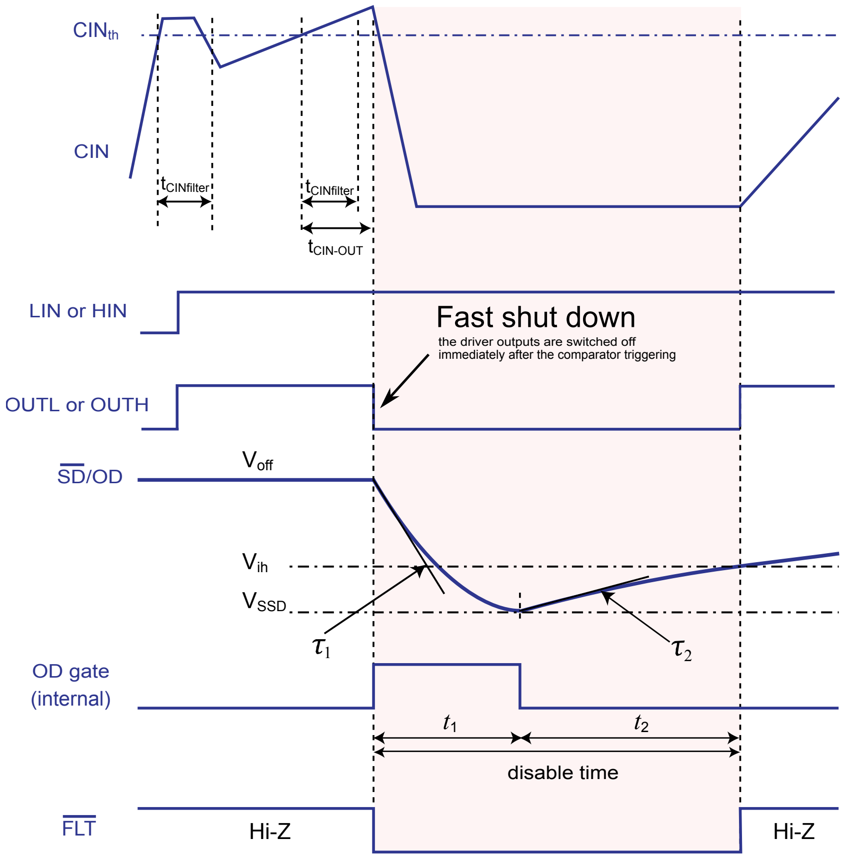
The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function with an automatic OFF-time mechanism (Smart Shutdown) providing the possibility to increase the disable time after the fault event up to an arbitrary value without increasing the delay time of the protection.

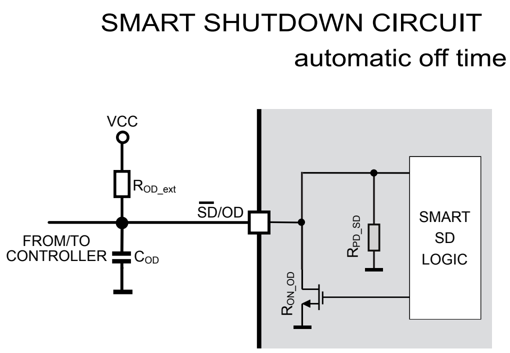
The comparator has an internal voltage reference CIN_{th} connected to the inverting input, while the non-inverting input is available on the CIN pin. The output signal of the comparator is filtered from glitches shorter than $t_{CINfilter}$ and then fed to the Smart Shutdown logic.

The $\overline{\text{SD}}$/OD is connected to a timing capacitor C_{OD} and a pull-up to determine the output disable time of the fault event.

When an overcurrent is detected, gates are immediately turned off, the $\overline{\text{FLT}}$ pin is forced low to signal the state to the controller, the $\overline{\text{SD}}$/OD pin discharges C_{OD} down to V_{SSD} and then the external pull-up charges it again. Once C_{OD} reaches V_{ih}, the gate driving restarts and $\overline{\text{FLT}}$ is released.

Figure 15. Smart Shutdown timing waveforms





An approximation of the disable time is given by:

$$t_1 \cong \tau_1 \cdot ln\left(\frac{V_{off} - V_{on}}{V_{SSD} - V_{on}}\right)$$

$$t_2 \cong \tau_2 \cdot ln\left(\frac{V_{SSD} - V_{off}}{V_{ih} - V_{off}}\right)$$

Where:

$$\tau_1 = (R_{ON\_OD} // R_{OD\_ext}) \cdot C_{OD}$$

$$\tau_2 = (R_{PD\_SD} // R_{OD\_ext}) \cdot C_{OD}$$

$$V_{on} = \frac{R_{ON\_OD}}{R_{ON\_OD} + R_{OD\_ext}} \cdot V_{BIAS}$$

$$V_{off} = \frac{R_{PD\_SD}}{R_{PD\_SD} + R_{OD\_ext}} \cdot V_{BIAS}$$

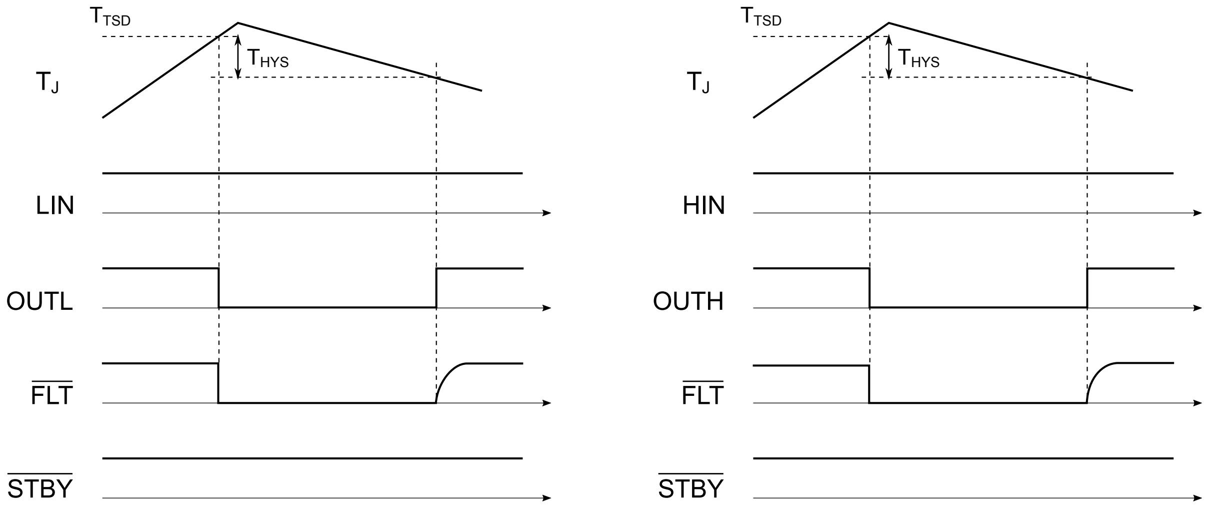
6.7 Thermal shutdown

The STDRIVEG611 provides a thermal shutdown protection feature.

When, during active mode, the junction temperature reaches the T_{TSD} temperature threshold, the device turns the driver outputs off to leaves the half-bridge in 3-state and signals this condition forcing the $\overline{FLT}$ pin low. The status of all the input pins is ignored.

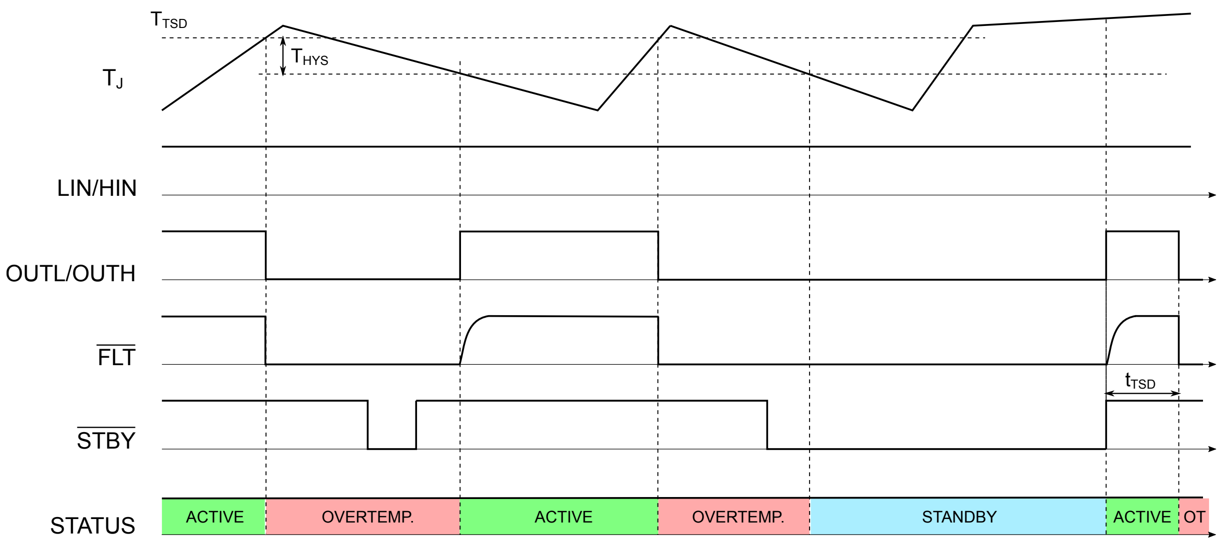
When the junction temperature is lower than T_{TSD}-T_{HYS}, the device operation is restored and the $\overline{FLT}$ pin is released.

Figure 16. **Thermal shutdown behavior**



The overtemperature detection is inactive when the device is operating in standby mode or in VCC UVLO to minimize consumption. On standby mode exit or VCC UVLO exit, overtemperature requires t_{TSD} to protect against overtemperature.

Figure 17. **Thermal shutdown vs. standby**



7 PCB, BOM, and layout recommendations

7.1 PCB suggestions

This section lists some tips to facilitate the PCB routing of the STDRIVEG611.

7.1.1 External BOM values selection and placement

A list of recommended value ranges for some key components are reported.

The bulk capacitors required for VCC, VCCL, VCCH, and BOOT must be placed as close as possible to relevant pins and relevant references. Such capacitors must be low ESR/ESL ceramic components having rated voltages that are almost twice the maximum operating voltages to overcome the well-known value modulation versus bias voltage.

The eventual external bootstrap diode is typically not required in motor control applications but is possible. In case of external diode use, a series resistor with a value of ≥ 2.2 Ω (10 Ω in case of large C_{BOOT}) is recommended to minimize the bootstrap diode peak current, EMI generation and supply rail spike generation. In case an external bootstrap diode is used, the C_{BOOT} capacitor must be placed on the PCB in such a way that the negative terminal is put as close as possible to the OUT pin: this arrangement ensures that the charging current flows in the shortest track possible. In the case of overcurrent comparator use, the user should consider the bootstrap current sums with the load current through the low-side: undesired overcurrent events could be generated especially with low R_{BOOT} values.

Turn-on resistors (RONx) need to be placed close to the IC to minimize the length of the track connected to the RONx pin.

Table 7. External BOM summary

Symbol	Function	Value (range)	Technology	Min. rating
C_{VCC}	VCC large bulk capacitor (it is normally used as bulk capacitor of controller too)	2.2 to 10 µF	EL-Cap (or X7R)	25 V
	VCC bypass capacitor	100 nF	X7R	50 V
C_{BOOT}	BOOT to OUT bypass capacitor	C_{VCCH} to 3300 nF	X7R	50 V
C_{VCCL}	VCCL to PGND bypass capacitor	47 nF to 470 nF	X7R	16 V
C_{VCCH}	VCCH to OUT bypass capacitor	47 nF to 470 nF	X7R	16 V
R_{BOOT}	Current limiting resistor of external D_{BOOT}	≥ 2.2 Ω		
D_{BOOT}	External Bootstrap diode (typically not required in motor control applications)	STTH1R06 or equivalent	Turbofast	600 V / 1 A

To speed-up start-up time, the user shall minimize C_{BOOT} and C_{VCCH} values. Most power conversion applications are optimized using C_{BOOT} = C_{VCCx} = 47 nF. Most motor control applications (depending on gate load) are optimized when using C_{VCCx} = 47 to 100 nF and C_{BOOT} = 100 to 470 nF.

A larger C_{BOOT} capacitor could be rarely required in specific applications if a very long high side on-time is required. On all other applications is recommended to keep C_{BOOT} small to avoid increasing start-up time, the potential need of the additional external bootstrap diode, the diode dissipation. In extreme cases, as in all gate driver applications, excessive C_{BOOT} and small C_{VCC} can lead to VCC drops due to charge sharing when low-side turns on, detected by the VCC UVLO.

PGND must be connected to the low-side GaN (Kelvin if available) source, which creates the path to GND through the optional current shunt resistor. So, PGND shall not be directly connected to GND to avoid shorting the Kelvin connection and reducing its benefits.

OUT must be connected to the high-side GaN (Kelvin if available) source. GaN main source and Kelvin source shall not be shorted together externally to best exploit the Kelvin benefits.

VCCL and VCCH are the output access to the internal voltage regulator: forcing these pins to external voltage regulators may result in unrecoverable damage of the IC.

7.1.2 Gate resistors

The most critical layout part in a GaN design is the gate driving loop: parasitic inductance must be minimized.

The path between OUTx → R_{GATE} resistor → GaN gate → GaN (Kelvin) source → PGND/OUT must be minimized. Using 0603 or smaller SMD resistors is recommended also as creating a small copper plane connected to PGND/OUT under the gate routing path to minimize loop inductance.

Turn-on gate resistors must be placed as close as possible to VCCH, RONH and VCCL, RONL pins.

7.1.3 Noise reduction

To minimize the noise generation during normal operation of typical applications, a few simple steps can be followed:

1. Connect signal GND to current shunt cold pole (or low-side source if shunt is not present) with a single star point. Signal ground consists of controller GND and signal GND of the STDRIVEG611.
2. If a shunt resistor is necessary, this component should have very small ELS and be placed as close as possible to the low-side source and the STDRIVEG611. A cheap alternative to a low ESL resistor consists of the parallel of multiple smaller resistors (for example, 3x 0603 SMD resistors have similar ESL of a 1020 package shunt resistor and is much lower than a 2010 standard package). On motor control applications, with low dV/dt and dI/dt, the requirement can be relaxed, but small SMD shunt resistors are still recommended to minimize ESL to remain in the recommended operating conditions range.
3. In the case of motor control (low dV/dt) applications requiring slowing down hard off dV/dt, a capacitor in parallel to GaN gate could be required. Place the capacitor as close as possible to the GaN pins. If ringing is observed, a resistor in series to these capacitors helps dumping ringing.
4. The OUT pin could be high frequency switching: it is preferable to be routed very closely to the load (in case of transformer or inductor) minimizing the overlap with any other nets. This avoids undesired parasitic capacitance and noise generation.
5. Components connected to BOOT, VCCH, RONH, and OUTH floats together with the OUT node. They must be placed as close as possible to the listed pins minimizing the overlap with other nets.
6. Keep current loops as small as possible. A high voltage ceramic capacitor connected between high voltage bus and power ground and placed as close as possible to GaN devices facilitates the reduction of such loops. In multiphase applications, a ceramic capacitor is recommended for each half-bridge. In high dV/dt hard switching applications, the high voltage ceramic capacitor ground return should be routed preferably just under, or at least beside, the low-side and high-side GaN to minimize loop inductance, ringing, and noise generation. The use of the first inner layer just under the GaN pads is the most effective. Proper dielectric thickness must be selected for the insulation between the two layers. A core foil, instead of prepreg, between the two layers is often used to ensure a more constant thickness in the PCB production process.

8 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 QFN 4 x 5 x 1 mm, 18 leads, 0.5 mm pitch, package information

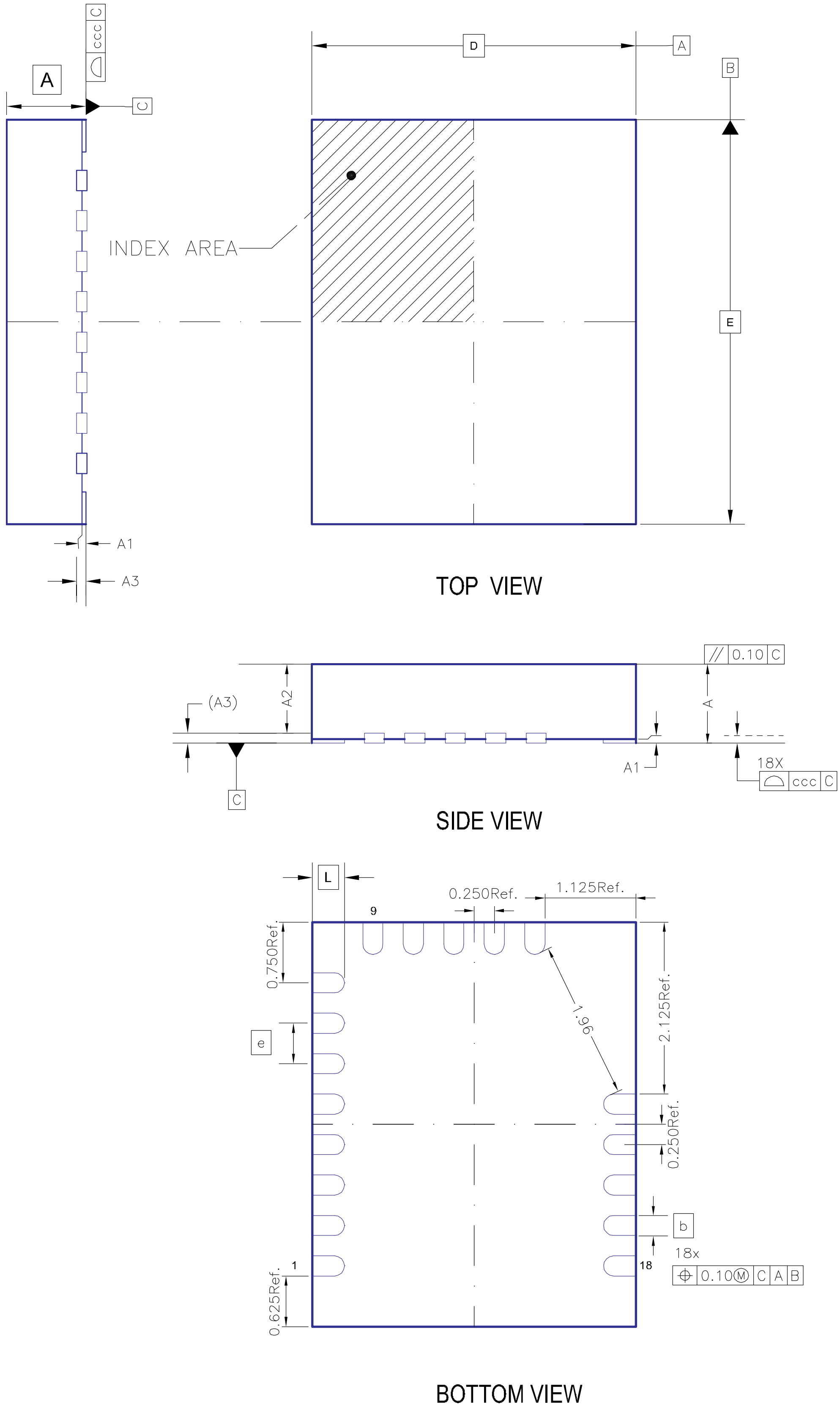
Table 8. QFN 4 x 5 x 1 mm, 18 leads, 0.5 mm pitch, package dimensions

Symbol	Dimensions [mm]		
	Min.	Typ.	Max
A	0.927	0.977	1.047
A1	0.0	-	0.05
A2	-	0.850	-
A3	0.03	0.13	0.23
b	0.20	0.25	0.30
D	4 BSC		
e	0.50 BSC		
E	5 BSC		
L	0.30	0.40	0.50
	TOLERANCE		
ccc	0.08		

Note: *Package outline exclusive of metal burr dimensions.*

Note: *Co-planarity applies to leads, corner leads and die attach pad.*

Figure 18. **QFN 4 x 5 x 1 mm, 18 leads, 0.5 mm pitch, package outline**



8.2 Suggested footprint

The STDRIVEG611 footprint for the PCB layout is usually defined based on several design factors such as assembly plant technology capabilities and board component density. For easy device usage and evaluation, STMicroelectronics provides the following footprint design, which is suitable for the largest variety of PCBs.

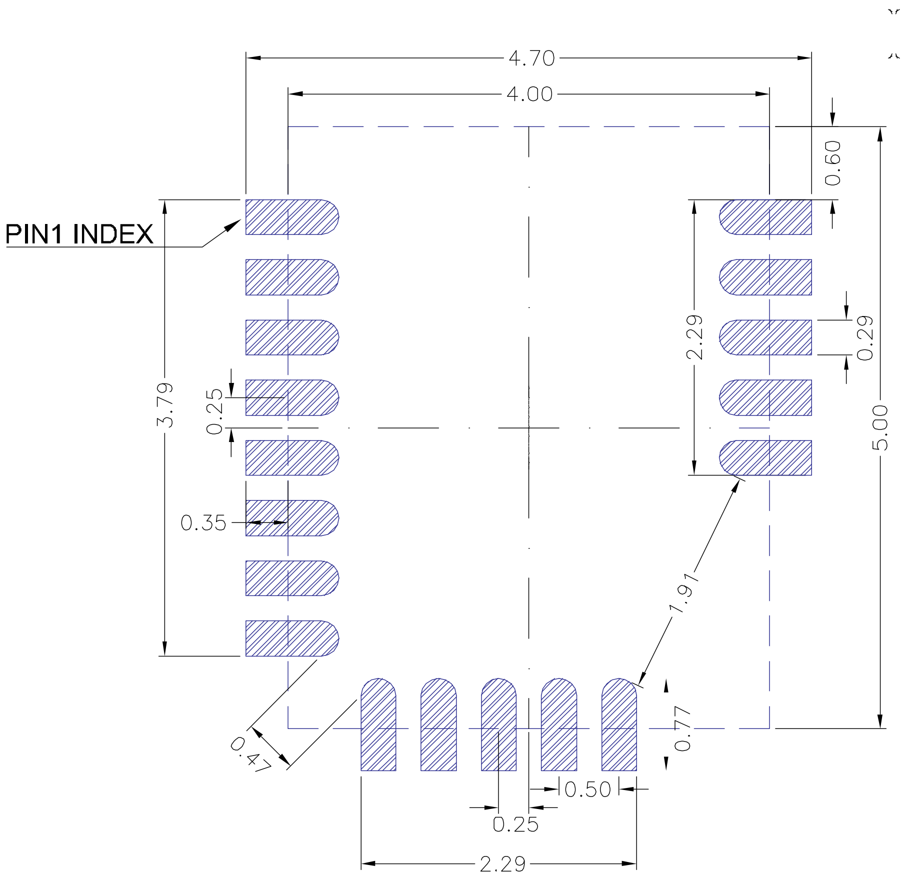
The following footprint indicates the copper area that should be free from the solder mask, while the copper area could extend beyond the indicated areas for device pins, especially GND, PGND, and OUT pins, which is beneficial for thermal and stray inductance minimization purposes.

A copper area connected to GND pins aids thermal dissipation, is useful to shield the input signal, and creates a low inductance, good return path for supplying capacitor currents.

A copper area connected to PGND and OUT pins running below the related components can minimize gate loop inductance for optimal gate driving and improves the return path for supply capacitor currents.

A PCB layout example is available with the STDRIVEG611 evaluation board.

Figure 19. QFN 4 x 5 x 1 mm, 18 leads, 0.5 mm pitch, suggested footprint



9 Ordering information

Table 9. Order code

Order Code	Package	Package marking	Packing
STDRIVEG611Q	QFN 4x5x1 mm	DRVG611	Tray
STDRIVEG611QTR	QFN 4x5x1 mm	DRVG611	Tape and Reel

Revision history

Table 10. Document revision history

Date	Version	Changes
31-Jul-2024	1	Initial release.
16-Dec-2024	2	Updated Table 2: I_{LS_OUT} and I_{HS_OUT} test condition; Table 3: VCC and V_{OUT} minimum values, removed note; Table 5 V_{HSthON}, V_{LSthON}, $V_{HSthOFF}$, $V_{LSthOFF}$, t_r, t_f values and added R_{PD_CIN} test condition; Table 9: added tray option. Updated Section Features, Section 7.1.1, and renamed Section 4.

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