EV5490-C-00A

ID Plus EML Bias for Optical Module Evaluation Board

DESCRIPTION

The EV5490-C-00A is an evaluation board designed to demonstrate the capabilities of the MP5490, which integrates four high-accuracy current sources (ID) for distributed feedback (DFB) laser diodes (LDs), as well as four negative voltage biases for EML bias. The MP5490 also provides 4-channel EML current measurement and MPD current measurement to simplify the design process.

The MP5490 integrates 6-channel high accuracy, low temperature coefficient external analog-to-digital converter (ADC) inputs. These ADCs can help to read the ROSA current and temperature information to conserve microcontroller (MCU) resources.

It is recommended to read the datasheet for the MP5490 prior to making any changes to the EV5490-C-00A.

PERFORMANCE SUMMARY

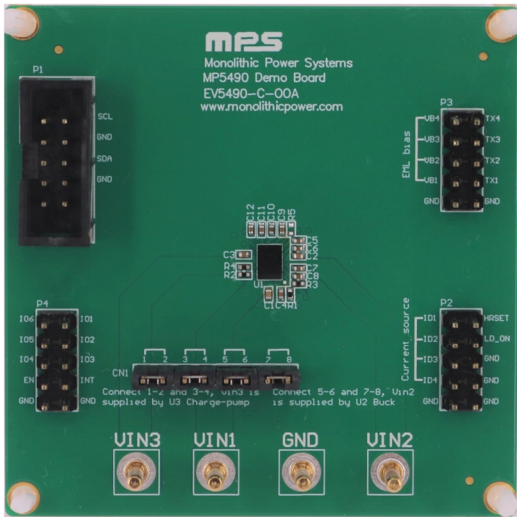
Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage for the circuitry range (V_{IN1})		2.7V to 5.5V
Input voltage for the current source range (V_{IN1}) (1)		1.2V to V_{IN1}
Input voltage for the EML bias range (V_{IN1}) (1)		-2V to -5V
Maximum ID current	R_{IMON} = 60.4kΩ, 0.1%	250mA
EML bias VBx pin range		-0.1V to -2.5V (2)
MPD current sensed range		0mA to 5mA

Notes:

1) V_{IN2} and V_{IN3} are powered by V_{IN1} by default, and there is no need for an external power supply. If external power is used, use the table above for V_{IN2} and V_{IN3} range.
2) The VBx pin minimum output is -2.5V by default. It can be set to -5V by writing CTL0 (0x00), bit[6] to 1.

EVALUATION BOARD



LxWxH (6.3cmx6.3cmx2cm)

Board Number	MPS IC Number
EV5490-C-00A	MP5490GC-0000

QUICK START GUIDE

The EV5490-C-00A evaluation board is easy to set up and use to evaluate the MP5490's performance. For proper measurement equipment set-up, refer to Figure 1 on page 3 and follow the steps below:

1. Preset the VIN1 power supply (V_{IN1}) between 2.7V and 5.5V, then turn off the power supply. (3) (4)
2. Connect power supply terminals to:
   a. Positive (+): VIN1
   b. Negative (-): GND
3. Connect the load terminals to:
   a. Positive (+): ID1, ID2, ID3, ID4, VB1, VB2, VB3, and VB4
   b. Negative (-): GND
4. After making the connections, turn on the power supply.
5. Configure the MP5490's ID or VB pins output using the microcontroller (MCU) I^2C interface or the MPS I^2C communication interface, then follow the steps below:
   a. Enable SYSEN by setting CTL0, bit D[7] to 1.
   b. Set the ID output current(s) via ID (0x07), bits D[7:0] and ID (0x08), bits D[1:0] (e.g. set ID1 = 100mA by setting register 0x07, bits D[7:0] to 0110 0100 and setting register 0x08, bits D[1:0] to 00).
   c. Set the VB output voltage(s) via VB (0x0F), bits D[7:0] and VB (0x10), bits D[1:0] (e.g. set VB1 = -1.2V by setting register 0x0F, bits D[7:0] to 0111 1000 and setting register 0x10, bits D[1:0] to 00).
   d. Enable ID_EN by setting CTL1, bit D[7] to 1. The ID pin should start to work.
   e. Enable VB_EN by setting CTL2, bit D[7] to 1. The VB pin should start to work.
6. To use the hardware enable function, apply a digital input to the EN pin. Drive EN above 0.8V to turn the evaluation board on; drive EN below 0.4V to turn it off.

Notes:

3) V_{IN2} and V_{IN3} are powered by V_{IN1} by default, and there is no need for an external power supply. V_{IN2} is 1.8V, and V_{IN3} is equal to $-V_{IN1}$ with a max 200mA I_{OUT}. If the sum of all load currents from the EML bias exceeds 200mA, remove jumpers 1, 2, 3, and 4 from CN1 (see Figure 1 on page 3), and use an external power supply to supply V_{IN3}.
4) There are two methods to change the V_{IN2} supply voltage. The first is to change the buck V_{OUT} via the MP5490's ADJ function, and the second is to remove jumpers 5, 6, 7, and 8 from CN1 (see Figure 1 on page 3), and use an external power supply to supply V_{IN2}.

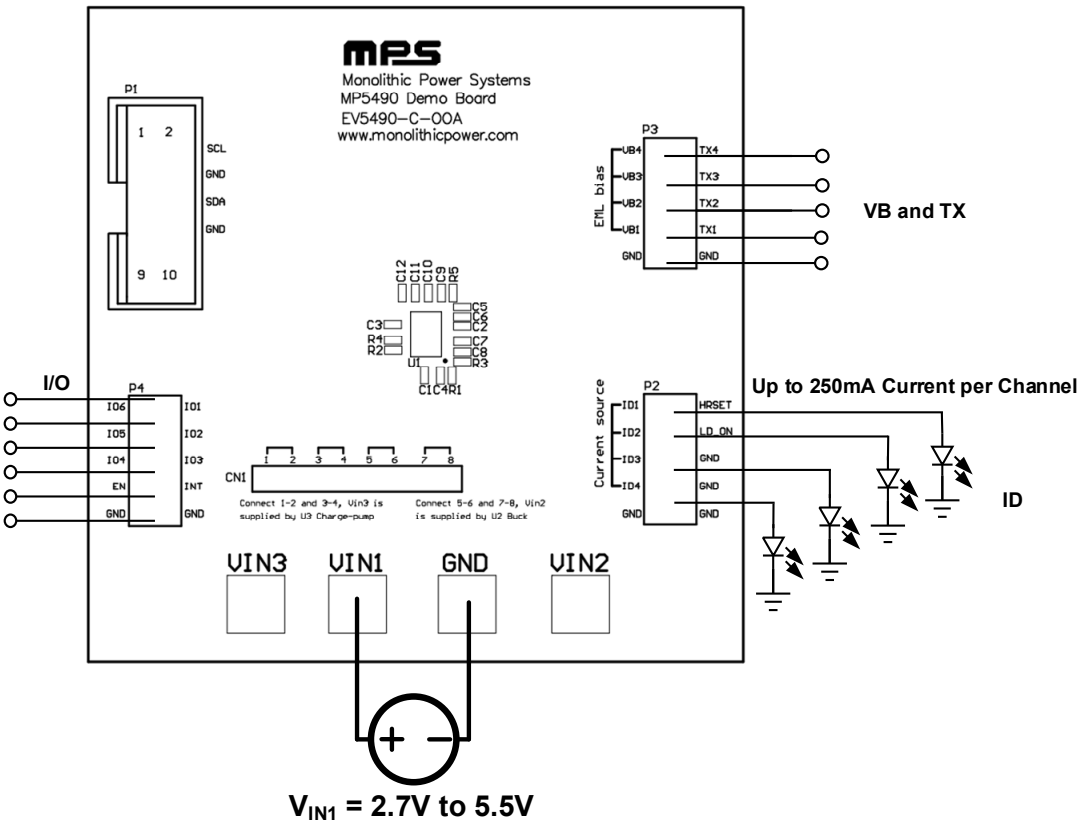


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

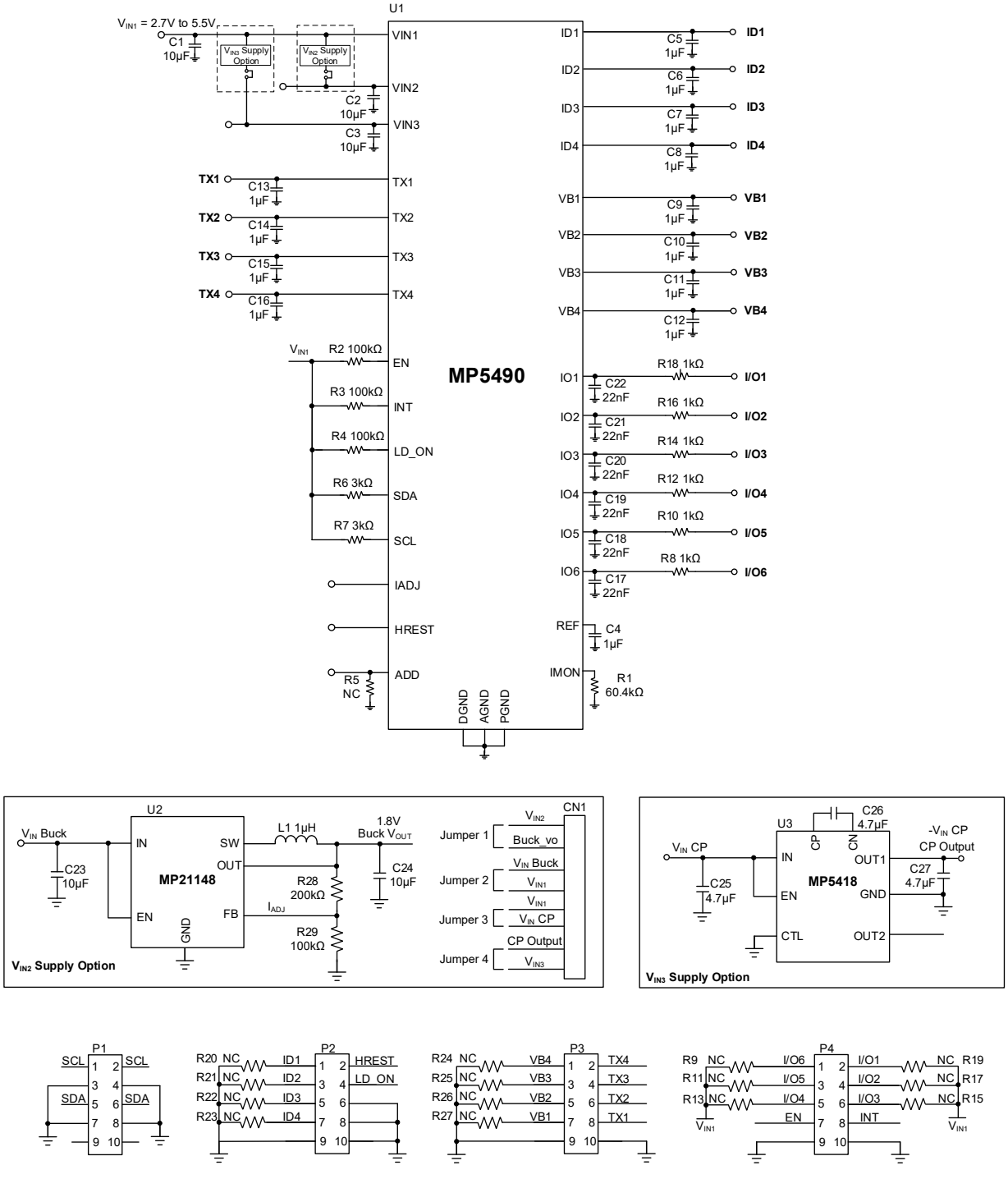


Figure 2: Evaluation Board Schematic

EV5490-C-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	C1, C2, C3	10µF	Ceramic capacitor, 6.3V, X5R	0402	Murata	GRM155R60J106ME44D
13	C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16	1µF	Ceramic capacitor, 25V, X5R	0402	Murata	GRM155R61E105KA12D
6	C17, C18, C19, C20, C21, C22	22nF	Ceramic capacitor, 25V, X7R	0402	Murata	GRM155R71E223KA61D
1	R1	60.4kΩ	Film resistor, 0.1%	0402	Panasonic	ERA-2AEB6042X
3	R2, R3, R4	100kΩ	Film resistor, 0.1%	0402	Yageo	RC0402FR-07100KL
0	R5, R9, R11, R13, R15, R17, R19, R20, R21, R22, R23, R24, R25, R26, R27	NC				
2	R6, R7	3kΩ	Film resistor, 0.1%	0402	Yageo	RC0402FR-073KL
6	R8, R10, R12, R14, R16, R18	1kΩ	Film resistor, 0.1%	0402	Yageo	RC0402FR-071KL
4	VIN1, VIN2, VIN3, GND	φ2.0	Φ2.0 copper pin	DIP	Custom	φ2.0 copper pin
1	P1		I^2C connector	DIP	Wurth	612010235121
3	P2, P3, P4	10 pins	10-pin, double-row straight header	DIP	Wurth	61301021121
1	CN1	8 pins	8-pin, single-row straight header	DIP	Wurth	61300811121
1	U1	MP5490	IDAC plus EML bias for QSFP optical module	CSP-36 (3mmx 4.25mm)	MPS	MP5490GC
V_{IN2} Buck Supply Option						
2	C23, C24	10µF	Ceramic capacitor, 10V, X5R	0603	Murata	GRM188R61A106KE69D
1	R28	200kΩ	Film resistor, 0.1%	0402	Yageo	RC0402FR-07200KL
1	R29	100kΩ	Film resistor, 0.1%	0402	Yageo	RC0402FR-07100KL
1	L1	1µH	Inductor, R_{DC} = 50mΩ, I_{SAT} = 4.2A	SMD	MPS	MPL-AT2010-1R0
1	U2	MP21148	Synchronous step-down converter	QFN-6	MPS	MP21148GQD
V_{IN3} Negative Voltage Supply Option						
3	C25, C26, C27	4.7µF	Ceramic capacitor, 16V, X6S	0603	Murata	GRM188C81C475KE11D
4	Jumper	2.54mm	Jumper, 1 x 2 pins	DIP	Wurth	60900213421
4	N/A (5)	5mm	White rivet, 5mmx10mm	Bulk	Wurth	709445100
1	U3	MP5418A	Negative charge pump and adjustable regulator	QFN-10	MPS	MP5418AGQG

Note:

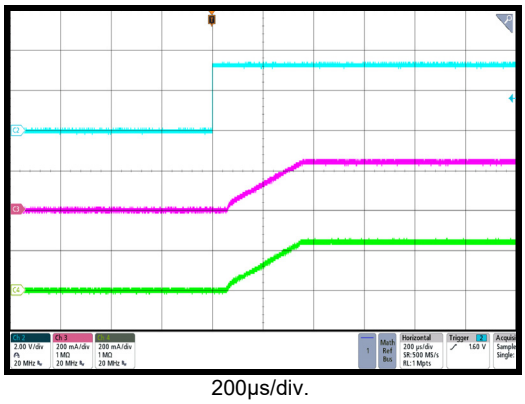
5) See the evaluation board image on page 1.

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN1} = 3.3V, V_{IN2} = 1.8V, V_{IN3} = -3.3V, T_A = 25°C, unless otherwise noted.

Start-Up through LD_ON

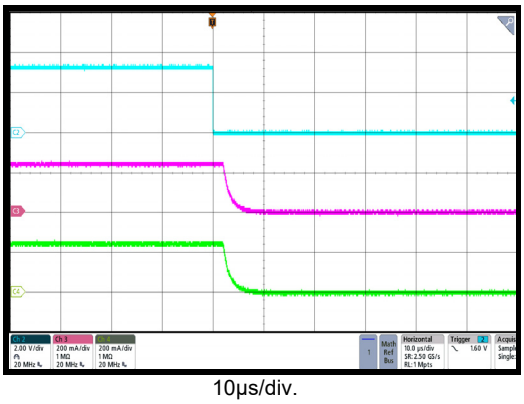
ID1 = ID3 = 250mA, SR bit = 01



200µs/div.

Shutdown through by LD_ON

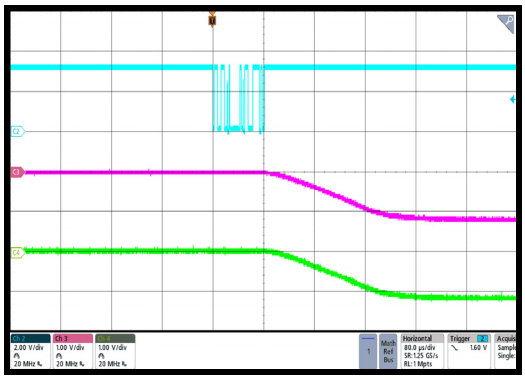
ID1 = ID3 = 250mA



10µs/div.

VB_EN Bit On

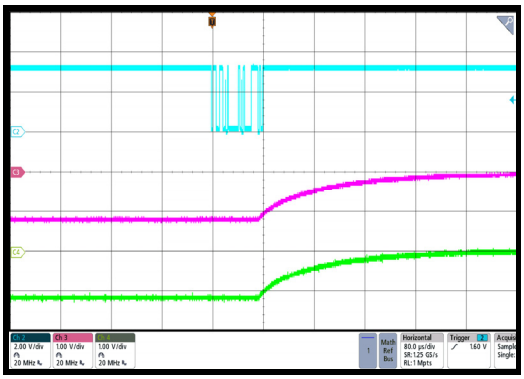
VB1 = VB3 = -1.2V



80µs/div.

VB_EN Bit Off

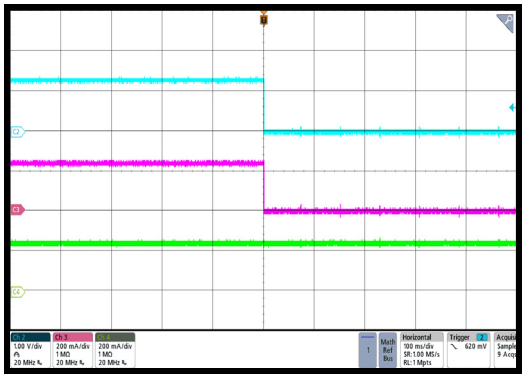
VB1 = VB3 = -1.2V



80µs/div.

ID SCP Entry

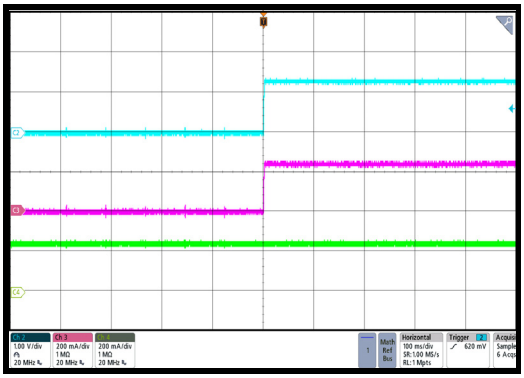
ID1 = ID3 = 250mA, auto-recovery mode



100ms/div.

ID SCP Recovery

ID1 = ID3 = 250mA, auto-recovery mode



100ms/div.

PCB LAYOUT

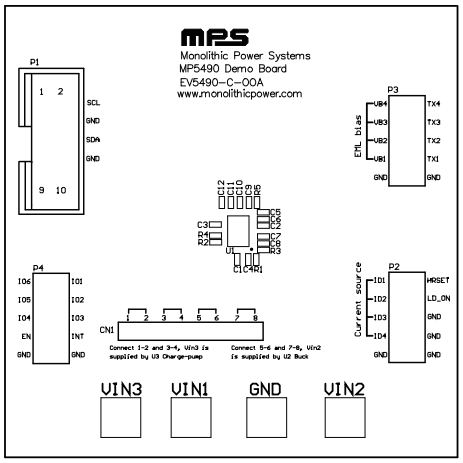


Figure 3: Top Silk

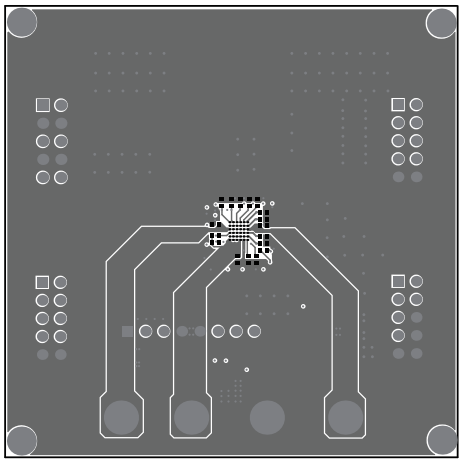


Figure 4: Top Layer

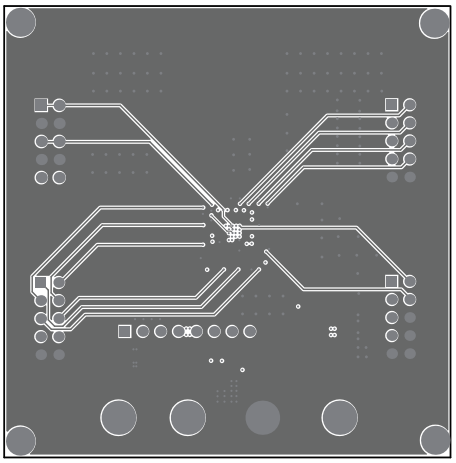


Figure 5: Mid-Layer 1

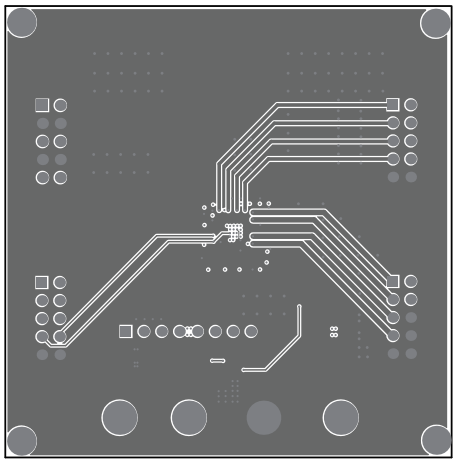


Figure 6: Mid-Layer 2

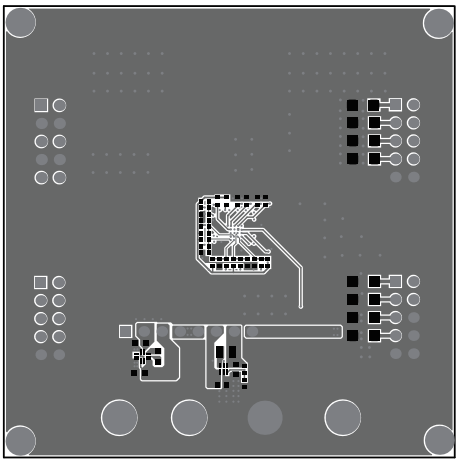


Figure 7: Bottom Layer

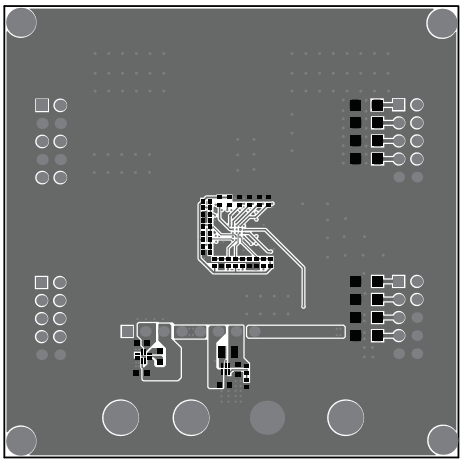


Figure 8: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/26/2023	Initial Release	-