EVQ79500FS-Q-00A

MPSafe™ ASIL-D 6-Channel Voltage Monitor Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ79500FS-Q-00A evaluation board is designed to demonstrate the capabilities of the MPQ79500FS, a 6-channel voltage monitor. The MPQ79500FS is engineered for automotive applications that require voltage rails to be monitored for safety.

Each voltage monitor input has configurable over-voltage (OV) and under-voltage (UV) thresholds. Highly accurate high-frequency (HF) and low-frequency (LF) voltage monitoring can detect when the voltage thresholds are reached. Two of the inputs are differential, remote voltage-sense input pairs. The MPQ79500FS can record the order in which voltage rails are sequenced, as well as their associated timestamps. The device also provides a sync I/O function to increase the number of the monitored voltage rails. The device is accessible through an I^2C interface.

With the integration of sophisticated functional safety features, this device is targeted to support applications with a high automotive safety integrity level up to ASIL-D.

The EVQ79500FS-Q-00A is fully assembled and tested. The MPQ79500FS is available in a QFN-16 (3mmx3mm) package with wettable flanks, and is AEC-Q100 qualified.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Power supply voltage (V_{DD}) range		2.7V to 5.5V
Pull-up voltage (V_{PU}) range		0.9V to 5.5V
Monitoring input voltage (V_{INx}) range	No scaling (Bank 1, VRANGE_MULT (0x1F), bits D[x - 1] = 0, where x = 1–6)	0.2V to 1.475V
	With x4 scaling (Bank 1, VRANGE_MULT (0x1F), bits D[x - 1] = 1, where x = 1–6)	0.8V to 5.5V
DC (<f_{LF}) voltage measurement accuracy (LF channel)	No scaling	±1LSB
DC (>f_{HF}) voltage measurement accuracy (HF channel)	No scaling, V_{INx} < 1V	±5mV
	No scaling, V_{INx} > 1V	±0.5%

EVQ79500FS-Q-00A EVALUATION BOARD

LxWxH (6.35cmx6.35cmx1cm)

Board Number	MPS IC Number
EVQ79500FS-Q-00A	MPQ79500FSGQE-0000-AEC1

QUICK START GUIDE

1. Preset the power supply (V_{DD}) between 3V and 5.5V, then turn off the power supply.
2. If longer cables (>0.5m total) are used between the source and the evaluation board, install a damping capacitor at the input terminals.
3. If the V_{DD} range is between 2.7V and 3V, turn on V_{DD} above its 3V maximum rising threshold, then decrease V_{DD} to the voltage value required for normal operation.
4. Connect the power supply terminals to:
   a. Positive (+): VDD
   b. Negative (-): GND
5. To connect jumpers on CN2, JP1, and JP2, follow the steps below:
   a. For CN2, if there is no remote voltage to monitor on the VINN pin, then connect VINN to GND.
   b. For JP1, connect the VPU pin on the evaluation board to VDD.
   c. For JP2, connect the SIN pin on the evaluation board to VDD.
6. Toggle SW1 to the low (L) side, and toggle SW2 to the high (H) side.
7. Connect the SDA, SCL, and GND pins to the I²C interface, then open Virtual Bench Pro 4.0, the MPQ79500FS's graphic user interface (GUI) (see Figure 1).

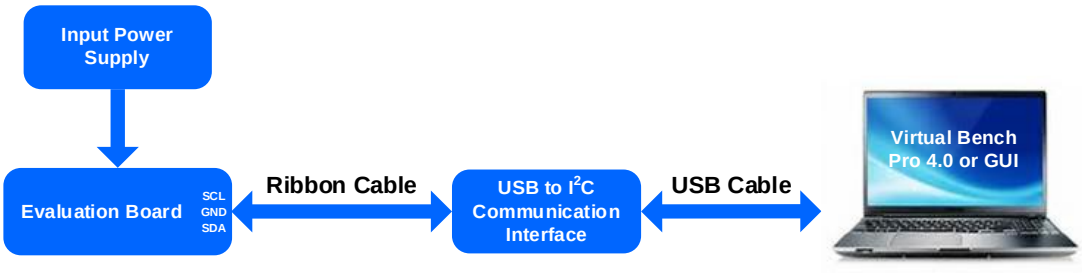


Figure 1: Connection to the I²C Interface

8. After making the connections, turn on the power supply. The board should automatically start up and then enter an idle state in high-power mode, where the NIRQ pin is pulled high.
9. The EVQ79500FS-Q-00A's address is 0x33. Table 1 shows the I²C addresses based on different R9 values. It is recommended to use a resistor with 1% accuracy.

Table 1: I²C Addresses

R9	Address (Bits)						
	6	5	4	3	2	1	0
0Ω to GND	Load from the OTP				0	0	0
8.06kΩ to GND	Load from the OTP				0	0	1
16kΩ to GND	Load from the OTP				0	1	0
24kΩ to GND	Load from the OTP				0	1	1
32.4kΩ to GND	Load from the OTP				1	0	0
40.2kΩ to GND	Load from the OTP				1	0	1
47.5kΩ to GND	Load from the OTP				1	1	0
0Ω to VDD	Load from the OTP				1	1	1

10. To set up V_{INx} on the evaluation board and in the registers, set the SIN voltage (V_{SIN}) to 5.5V. V_{IN1} is 0.95V, V_{IN2} is 1.2V, V_{IN3} is 1.8V, V_{IN4} is 3.3V, V_{IN5} is 5V, and V_{IN6} is 5.5V. Set VRANGE_MULT in Bank 1 as 3C, then read the corresponding voltage of VIN_LVL[x] in Bank 0. Table 2 shows V_{INx} divided by V_{SIN}.

Table 2: V_{INx} Divided by V_{SIN}

Channel	Pull-Up Resistor		Pull-Down Resistor		V_{INx} (V) (V_{SIN} = 5.5V)	Value Read in VIN_LVL[x] in Bank 0
	Ref	Value (kΩ)	Ref	Value (kΩ)		
CH1	R3	47.5	R4	10	0.95	96
CH2	R5	35.7	R6	10	1.2	C8
CH3	R11	20.5	R12	10	1.8	32
CH4	R13	6.65	R14	10	3.3	7D
CH5	R15	1	R16	10	5	D2
CH6	R17	0	R17	10	5.5	EB

11. To initiate the sequence transition, remove JP2 and then follow the steps below:
    a. Directly apply the monitored voltage to the VINx pin on CN2, then write the registers in Bank 1. See the SEQ Monitoring On waveform and Table 3 on page 7. The set-up in the registers must be written with the values corresponding to the rails on VINx.
    b. Toggle SW1 from low to high to transition the MPQ79500FS from an idle state to an active state, after which a 38ms timeout occurs. Read the sequence log and timestamp from the registers.
    c. Toggle SW2 from high to low to transition the MPQ79500FS from an active state to a sleep state, after which a 38ms timeout occurs. Read the sequence log and timestamp from the registers.
    d. Toggle SW2 from low to high to transition the MPQ79500FS from a sleep state to an active state, after which a 38ms timeout occurs. Read the sequence log and timestamp from the registers.
    e. Toggle SW1 from high to low to transition the MPQ79500FS from an active state to an idle state.
12. To use the NIRQ pin's interrupt output function, follow the steps below:
    a. If there is no fault, the NIRQ pin's output is high.
    b. If an interrupt is reported, the MPQ79500FS pulls the NIRQ pin low. Read the registers in Bank 0 to obtain the interrupt information. Some interrupts can be cleared by writing 1. Refer to the MPQ79500FS datasheet for more details.
13. If an external signal is used to control the ACT/SHDN pin or ACT/SLP pin, maintain SW1 or SW2 high, then add the signal input to ACT/SHDN or ACT/SLP. The ACT/SHDN and ACT/SLP rising threshold is 0.84V, and the ACT/SHDN and ACT/SLP falling threshold is 0.36V. ACT/SHDN and ACT/SLP are edge-triggered.
14. The recommended threshold range for a channel with 1x scaling is between 0.215V and 1.46V. The recommended threshold range for a channel with 4x scaling is between 0.86V and 5.5V.
15. If an independent pull-up voltage (V_{PU}) is applied, remove JP1, then connect the power source terminals to:
    a. Positive (+): VPU
    b. Negative (-): GND

16. Set V_{PU} between 0.9V and 5.5V.

17. Figure 2 shows the proper measurement equipment set-up.

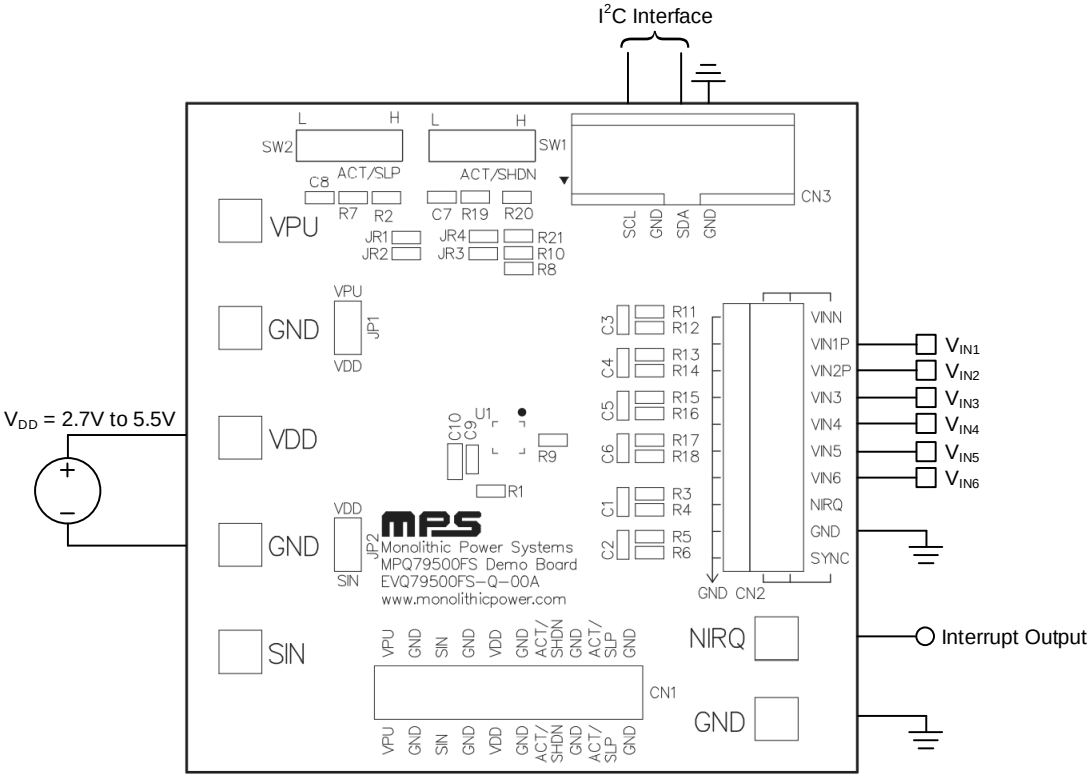
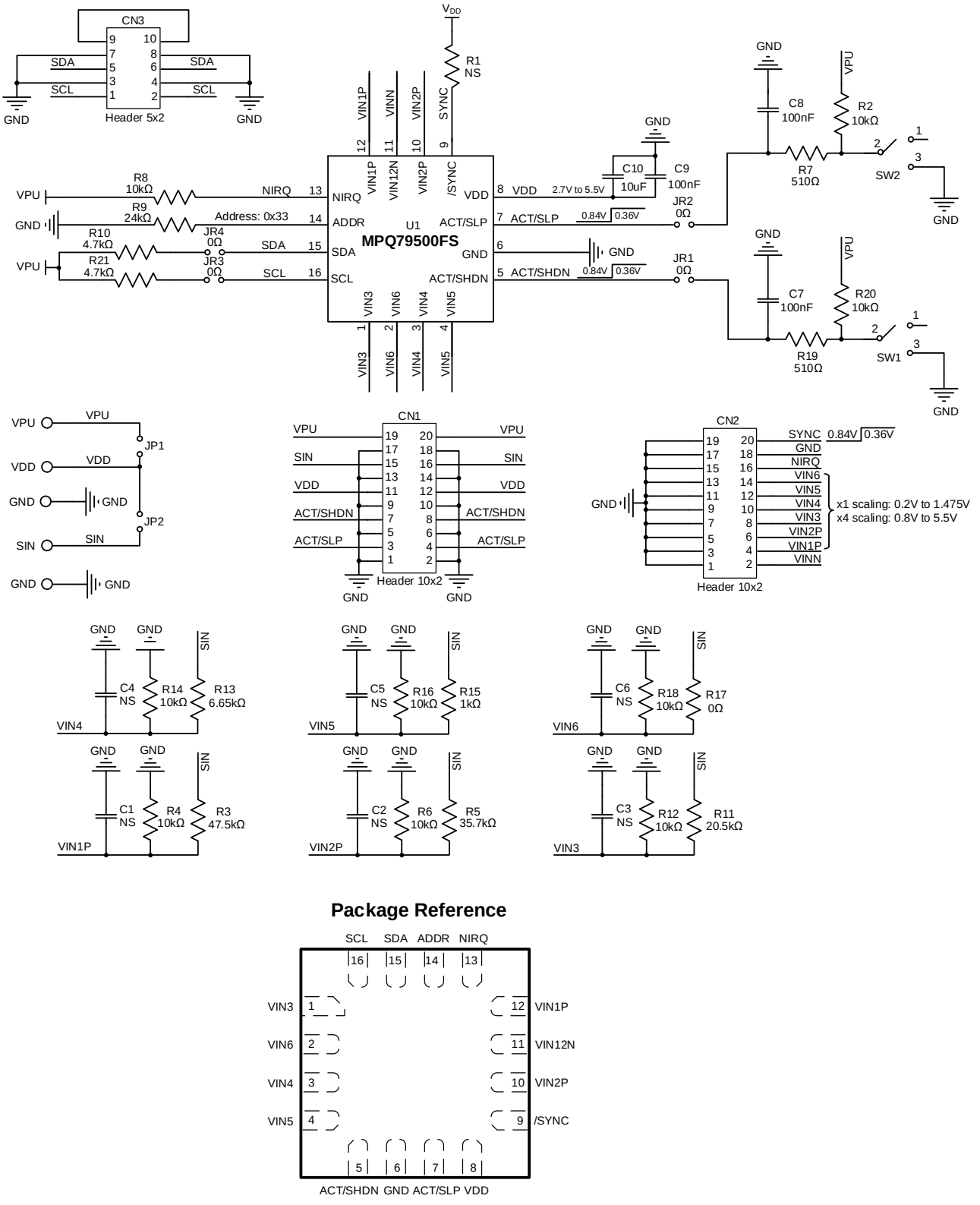


Figure 2: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC



Package Reference

Figure 3: Evaluation Board Schematic

EVQ79500FS-Q-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
6	C1, C2, C3, C4, C5, C6	NS				
3	C7, C8, C9	100nF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	C10	10µF	Ceramic capacitor, 10V, X7R	0805	Murata	GRM21BR71A106KE51L
1	CN1	2.54mm	180° pin header, 2 x 10-pin	DIP	Custom (1)	
1	CN2	2.54mm	180° pin header, 3 x 10-pin	DIP	Custom (1)	
1	CN3	2.54mm	Male box header, 2 x 5-pin	DIP	Wurth	61201021621
7	GND, SIN, VDD, VPU, GND, NIRQ, GND	1mm	Test point, golden pin	DIP	Custom (1)	
2	JP1, JP2	2.54mm	Header, 2-pin	DIP	Custom (1)	
2	JP1, JP2	2.54mm	Jumper, 2-pin	DIP	Custom (1)	
4	JR1, JR2, JR3, JR4	0Ω	Film resistor, 1%	0603	Royalohm	0603WAF0000T5E
1	R1	NS				
1	R9	24kΩ	Film resistor, 1%	0602	Yageo	RC0603FR-0724KL
9	R2, R4, R6, R8, R12, R14, R16, R18, R20	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R3	47.5kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0747K5L
1	R5	35.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0735K7L
1	R11	20.5kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0720K5L
1	R13	6.65kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-076K65L
1	R15	1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071KL
1	R17	0Ω	Film resistor, 1%	0603	RoyalOhm	0603WAF0000T5E
2	R19, R7	510Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07510RL
2	R10, R21	4.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-074K7L
2	SW1, SW2	10mmx2.5mm	Slide switch, opposite side connection	DIP	Wurth	450301014042
1	U1	MPQ79500FS	ASIL-D 6-channel voltage monitor, AEC-Q100 qualified	QFN16 (3mmx 3mm)	MPS	MPQ79500FSGQE-0000-AEC1

Note:

1) Contact an MPS FAE for more information regarding custom pins.

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{DD} = 3.3V, V_{PU} = 3.3V, T_A = 25°C, unless otherwise noted.

SEQ Monitoring On

Single MPQ79500FS device, ACT/SHDN = low to high, ACT/SLP = high

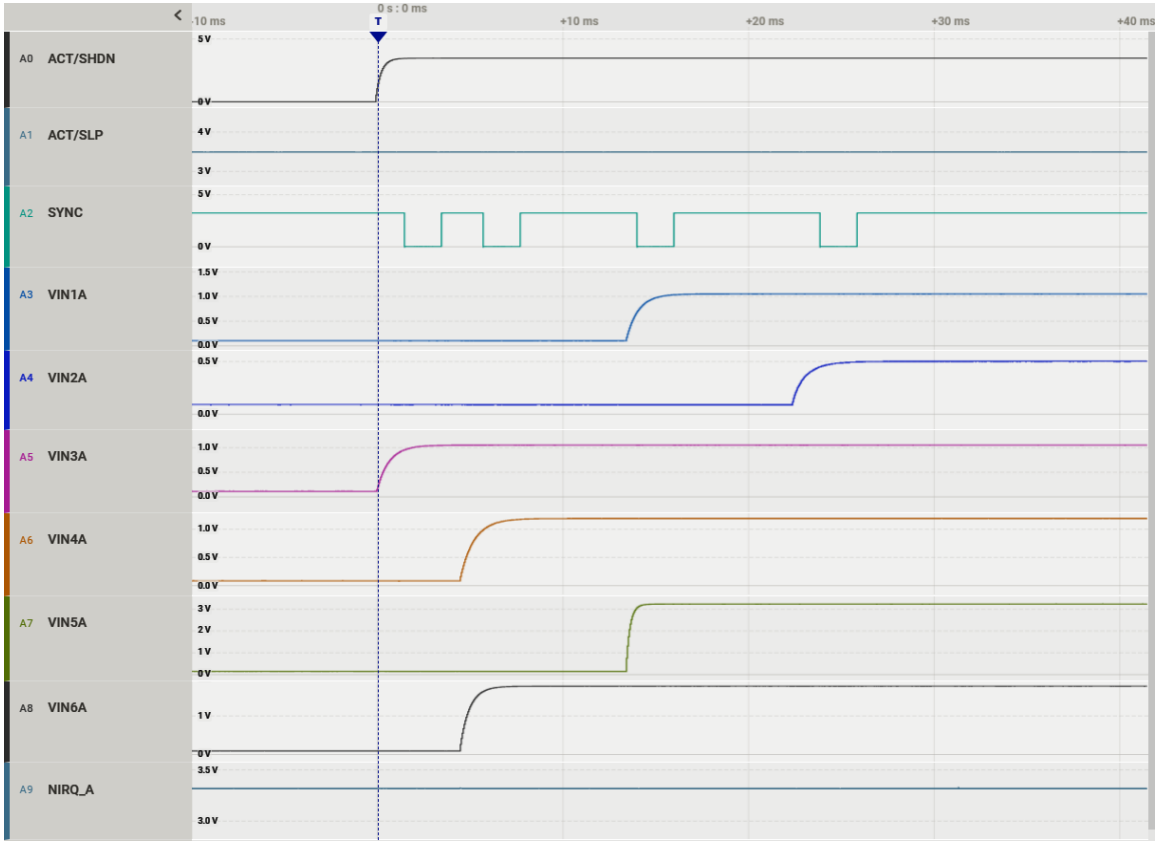


Table 3: Read Register after Timeout

Bank 0 of Part A				Bank 1 of Part A			
Address	**Register Name**	**Read Result**	**Description**	**Address**	**Register Name**	**Read Result**	**Description**
0x10	INT_SRC	00	No interrupt after SEQ is on.	0x13	IEN_UVHF	3F	UVHF monitoring for channels 1–6 is enabled.
0x11	INT_MONITOR	00	No interrupt after SEQ is on.	0x14	IEN_UVLF	3F	UVLF monitoring for channels 1–6 is enabled.
0x12	INT_UVHF	00	No UVHF fault has occurred.	0x15	IEN_OVHF	3F	OVHF monitoring for channels 1–6 is enabled.
0x14	INT_UVLF	00	No UVLF fault has occurred.	0x16	IEN_OVLF	3F	OVLF monitoring for channels 1–6 is enabled.
0x16	INT_OVHF	00	No OVHF fault has occurred.	0x17	IEN_SEQ_ON	3F	SEQ_ON monitoring for channels 1–6 is enabled.
0x18	INT_OVLF	00	No OVLF fault has occurred.	0x18	IEN_SEQ_OFF	3F	SEQ_OFF for channels 1–6 is enabled.
0x1A	INT_SEQ_ON	00	No power-up sequence fault has occurred.	0x19	IEN_SEQ_EXS	3F	SEQ_EXS for channels 1–6 is enabled.
0x1C	INT_SEQ_OFF	00	No power-off sequence fault has occurred.	0x20	UV_HF[1]	80	The channel 1 UVHF threshold is 0.84V.

0x1E	INT_SEQ_EXS	00	No sleep exit sequence fault has occurred.	0x21	OV_HF[1]	D4	The channel 1 OVHF threshold is 1.26V.
0x20	INT_SEQ_ENS	00	No sleep entry sequence fault has occurred.	0x22	UV_LF[1]	94	The channel 1 UVLF threshold is 0.94V.
0x22	NT_CONTROL	00	No interrupt after SEQ is on.	0x23	OV_LF[1]	C0	The channel 1 OVLF threshold is 1.16V.
0x23	INT_TEST	00	No interrupt after SEQ is on.	0x24	FLT_HF[1]	22	The OV/UV debouncing time for the high-frequency threshold comparator for channel 1 is 0.4µs.
0x24	INT_VENDOR	00	No interrupt after SEQ is on.	0x25	FC_LF[1]	04	The low-frequency path cutoff frequency for channel 1 is 1kHz.
0x30	VMON_STAT	4E	The monitoring status is as expected.	0x32	UV_LF[2]	30	The channel 2 UVLF threshold is 0.44V.
0x31	TEST_INFO	00	No error for the internal self-testing and ECC.	0x35	FC_LF[2]	04	The low-frequency path cutoff frequency for channel 2 is 1kHz.
0x32	OFF_STAT	00	Channels 1–6 are in the on state.	0x42	UV_LF[3]	94	The channel 3 UVLF threshold is 0.94V.
0x36	SEQ_ORD_STAT	04	4 sync pulse count.	0x45	FC_LF[3]	04	The low-frequency path cutoff frequency for channel 3 is 1kHz.
0x40	VIN_LVL[1]	AC	VIN1A is 1.06V in the active state after SEQ on.	0x52	UV_LF[4]	B0	The channel 4 UVLF threshold is 1.08V.
0x41	VIN_LVL[2]	3D	VIN2A is 0.505V in the active state after SEQ on.	0x55	FC_LF[4]	04	The low-frequency path cutoff frequency for channel 4 is 1kHz.
0x42	VIN_LVL[3]	AA	VIN3A is 1.05V in the active state after SEQ on.	0x62	UV_LF[5]	6C	The channel 5 UVLF threshold is 2.96V.
0x43	VIN_LVL[4]	C8	VIN4A is 1.2V in the active state after SEQ on.	0x65	FC_LF[5]	04	The low-frequency path cutoff frequency for channel 5 is 1kHz.
0x44	VIN_LVL[5]	7B	VIN5A is 3.26V in the active state after SEQ on.	0x72	UV_LF[6]	29	The channel 6 UVLF threshold is 1.62V.
0x45	VIN_LVL[6]	32	VIN6A is 1.8V in the active state after SEQ is on.	0x75	FC_LF[6]	04	The low-frequency path cutoff frequency for channel 6 is 1kHz.
0x50	SEQ_ON_LOG[1]	03	The rail on VIN1A is up in the first SYNC pulse recording as first sequence log.	0x1A	IEN_SEQ_ENS	3F	SEQ_ENS monitoring for channels 1–6 is enabled.
0x51	SEQ_ON_LOG[2]	04	The rail on VIN2A is up in the fourth SYNC pulse record as fourth sequence log.	0x1E	VIN_CH_EN	3F	Channels 1–6 are enabled.
0x52	SEQ_ON_LOG[3]	01	The rail on VIN3A is up in the first SYNC pulse record as first sequence log.	0x1F	VRANGE_MULT	30	VIN1–VIN4 are 1x scaling, VIN5 and VIN6 are 4x scaling.

0x53	SEQ_ON_LOG[4]	02	The rail on VIN4A is up in the second SYNC pulse record as second sequence log.	0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.
0x54	SEQ_ON_LOG[5]	03	The rail on VIN5A is up in the third SYNC pulse record as third sequence log.	0xA2	AMSK_OFF	3F	AMSK_OFF for VIN1–VIN6 is enabled.
0x55	SEQ_ON_LOG[6]	02	The rail on VIN6A is up in the second SYNC pulse record as the second sequence log.	0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.
0x90	SEQ_TIME_MSB[1]	01	The VIN1A up time is 14.75ms.	0xA4	AMSK_ENS	06	AMSK_ENS for VIN1, VIN4, VIN5, and VIN6 is enabled.
0x91	SEQ_TIME_LSB[1]	27		0xA5	SEQ_TOUT_MSB	00	The timeout set is to 38ms.
0x92	SEQ_TIME_MSB[2]	01	The VIN2A up time is 23.8ms.	0xA6	SEQ_TOUT_LSB	25	
0x93	SEQ_TIME_LSB[2]	DC		0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.
0x94	SEQ_TIME_MSB[3]	00	The VIN3A up time is 1.45ms.	0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.
0x95	SEQ_TIME_LSB[3]	1D		0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.
0x96	SEQ_TIME_MSB[4]	00	The VIN4A up time is 6.15ms.	0xB0	SEQ_ON_EXP[1]	03	The expected sequence log for VIN1A is 3.
0x97	SEQ_TIME_LSB[4]	7B		0xB1	SEQ_ON_EXP[2]	04	The expected sequence log for VIN2A is 4.
0x98	SEQ_TIME_MSB[5]	01	The VIN5A up time is 13.95ms.	0xB2	SEQ_ON_EXP[3]	01	The expected sequence log for VIN3A is 1.
0x99	SEQ_TIME_LSB[5]	17		0xB3	SEQ_ON_EXP[4]	02	The expected sequence log for VIN4A is 2.
0x9A	SEQ_TIME_MSB[6]	00	The VIN6A up time is 5.7ms.	0xB4	SEQ_ON_EXP[5]	03	The expected sequence log for VIN5A is 3.
0x9B	SEQ_TIME_MSB[6]	72		0xB5	SEQ_ON_EXP[6]	02	The expected sequence log for VIN6A is 2.

SEQ Monitoring On with Multiple MPQ79500FS Devices

Three MPQ79500FS devices, ACT/SHDN = low to high, ACT/SLP = high

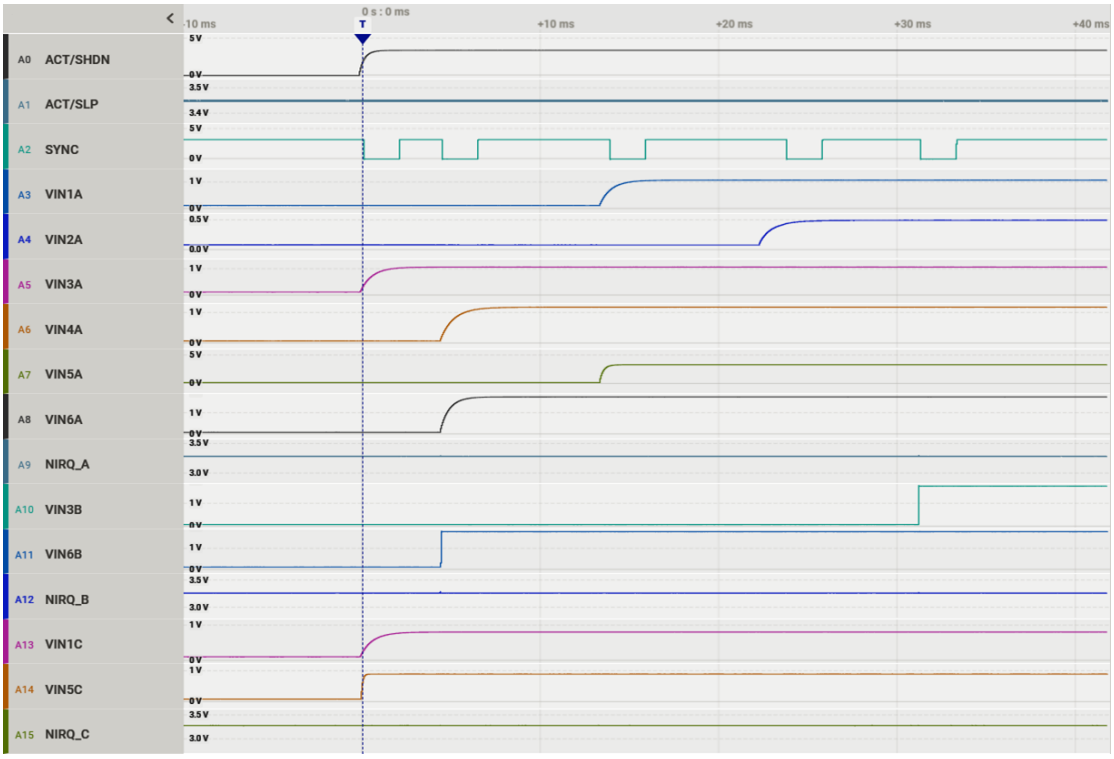


Table 4: Read Register after Timeout

		Part A		Part B		Part C	
Add.	**Register Name**	**Read Result**	**Description**	**Read Result**	**Description**	**Read Result**	**Description**
Bank 0							
0x10 ~10x 24	Interrupt Information Registers	00	No interrupt after SEQ_ON.	00	No interrupt after SEQ is on.	00	No interrupt after SEQ_ON.
0x32	OFF_ STAT	00	Channels 1–6 are in the on state.	1B	Channel 3 and channel 6 are in the on state.	2E	Channel 1 and channel 5 are in the on state.
0x36	SEQ_ ORD_ STAT	05	5 sync pulse count.	05	5 sync pulse count.	05	5 sync pulse count.
0x40	VIN_ LVL[1]	AC	VIN1A is 1.06V in the active state after SEQ_ON.	00	VIN1B is not on.	78	VIN1A is 0.8V at active state after SEQ_ON.
0x41	VIN_ LVL[2]	3D	VIN2A is 0.505V in active state after SEQ_ON.	00	VIN2B is not on.	00	VIN2C is not on.
0x42	VIN_LVL[3]	AA	VIN3A is 1.05V in the active state after SEQ_ON.	32	VIN3B is 1.8V at active state after SEQ is on.	00	VIN3C is not on.
0x43	VIN_LVL[4]	C8	VIN4A is 1.2V in the active state after SEQ_ON.	00	VIN4B is not on.	00	VIN4C is not on.
0x44	VIN_LVL[5]	7B	VIN5A is 3.26V in the active state after SEQ_ON.	00	VIN5B is not on.	8C	VIN5C is 0.9V at active state after SEQ_ON.
0x45	VIN_LVL[6]	32	VIN6A is 1.8V in the active state after SEQ_ON.	32	VIN6B is 1.8V at active state after SEQ_ON.	00	VIN6C is not on.
0x50	SEQ_ON_L OG[1]	03	The rail on VIN1A is up in the first SYNC pulse record as the first sequence log.	00	VIN1B does not have a sequence when SEQ is on.	01	The rail on VIN1C is up in the first SYNC pulse record as the first sequence log.

0x51	SEQ_ON_LOG[2]	04	The rail on VIN2A is up in the fourth SYNC pulse record as the fourth sequence log.	00	VIN2B does not have a sequence when SEQ is on.	00	VIN2C does not have a sequence when SEQ is on.
0x52	SEQ_ON_LOG[3]	01	The rail on VIN3A is up in the first SYNC pulse record as the first sequence log.	05	The rail on VIN3B is up in the fifth SYNC pulse record as the fifth sequence log.	00	VIN3C does not have a sequence when SEQ is on.
0x53	SEQ_ON_LOG[4]	02	The rail on VIN4A is up in the second SYNC pulse record as the second sequence log.	00	VIN4B does not have a sequence when SEQ is on.	00	VIN4C does not have a sequence when SEQ is on.
0x54	SEQ_ON_LOG[5]	03	The rail on VIN5A is up in the third SYNC pulse record as the third sequence log.	00	VIN5B does not have a sequence when SEQ is on.	01	The rail on VIN5C is up in the first SYNC pulse record as the first sequence log.
0x55	SEQ_ON_LOG[6]	02	The rail on VIN6A is up in the second SYNC pulse record as the second sequence log.	02	The rail on VIN6B is up in the second SYNC pulse record as the second sequence log.	00	VIN6C does not have a sequence when SEQ is on.
0x90	SEQ_TIME_MSB[1]	01	The VIN1A up time is 14.8ms.	00	VIN1B does not have a sequence when SEQ is on.	00	The VIN1C up time is 1.55ms.
0x91	SEQ_TIME_LSB[1]	28		00		1F	
0x92	SEQ_TIME_MSB[2]	01	The VIN2A up time is 23.85ms.	00	VIN2B does not have a sequence when SEQ is on.	00	VIN2C does not have a sequence when SEQ is on.
0x93	SEQ_TIME_LSB[2]	DD		00		00	
0x94	SEQ_TIME_MSB[3]	00	The VIN3A up time is 1.45ms.	02	The VIN3B up time is 31.25ms.	00	VIN3C does not have a sequence when SEQ is on.
0x95	SEQ_TIME_LSB[3]	1D		71		00	
0x96	SEQ_TIME_MSB[4]	00	The VIN4A up time is 6.15ms.	00	VIN4B does not have a sequence when SEQ is on.	00	VIN4C does not have a sequence when SEQ is on.
0x97	SEQ_TIME_LSB[4]	7B		00		00	
0x98	SEQ_TIME_MSB[5]	01	The VIN5A up time is 13.95ms.	00	VIN5B does not have a sequence when SEQ is on.	00	The VIN5C up time is 0.15ms.
0x99	SEQ_TIME_LSB[5]	17		00		03	
0x9A	SEQ_TIME_MSB[6]	00	The VIN6A up time is 5.7ms.	00	The VIN6B up time is 4.55ms.	00	VIN6C does not have a sequence when SEQ is on.
0x9B	SEQ_TIME_MSB[6]	72		5B		00	
Bank 1							
0x1E	VIN_CH_EN	3F	Channels 1–6 are enabled.	24	Channel 3 and channel 6 are enabled.	11	Channel 1 and channel 5 are all enabled.
0x1F	VRANGE_MULT	30	VIN1–VIN4 are 1x scaling, VIN5 and VIN6 are 4x scaling.	37	VIN3 and VIN6 are 4x scaling.	37	VIN1 and VIN5 are 1x scaling.
0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.	3C	AMSK_ON for VIN3 and VIN6 is enabled.	3C	AMSK_ON for VIN1 and VIN5 is enabled.
0xA2	AMSK_OFF	3F	AMSK_OFF for VIN1–VIN6 are all enabled.	3C	AMSK_OFF for VIN3 and VIN6 is enabled.	3C	AMSK_OFF for VIN1 and VIN5 is enabled.
0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_EXS for VIN6 is enabled, AMSK_EXS of VIN3 is disabled.	20	AMSK_EXS for VIN1 and VIN5 is enabled.
0xA4	AMSK_ENS	06	AMSK_ENS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_ENS for VIN6 is enabled, AMSK_ENS of VIN3 is disabled.	20	AMSK_ENS for VIN1 and VIN5 is enabled.

0xA5	SEQ_TOUT_MSB	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.
0xA6	SEQ_TOUT_LSB	25		25		25	
0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.
0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.
0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.
0xB0	SEQ_ON_EXP[1]	03	The expected sequence log for VIN1A is 3.	00	The expected sequence log for VIN1B is 0.	01	Expected sequence log for VIN1C is 1.
0xB1	SEQ_ON_EXP[2]	04	The expected sequence log for VIN2A is 4.	00	The expected sequence log for VIN2B is 0.	00	The expected sequence log for VIN2C is 0.
0xB2	SEQ_ON_EXP[3]	01	The expected sequence log for VIN3A is 1.	05	The expected sequence log for VIN3B is 5.	00	The expected sequence log for VIN3C is 0.
0xB3	SEQ_ON_EXP[4]	02	The expected sequence log for VIN4A is 2.	00	The expected sequence log for VIN4B is 0.	00	The expected sequence log for VIN4C is 0.
0xB4	SEQ_ON_EXP[5]	03	The expected sequence log for VIN5A is 3.	00	The expected sequence log for VIN5B is 0.	01	The expected sequence log for VIN5C is 1.
0xB5	SEQ_ON_EXP[6]	02	The expected sequence log for VIN6A is 2.	02	The expected sequence log for VIN6B is 2.	00	The expected sequence log for VIN6C is 0.

SEQ Monitoring Off with Multiple MPQ79500FS Devices

Three MPQ79500FS devices, ACT/SHDN = high to low, ACT/SLP = high

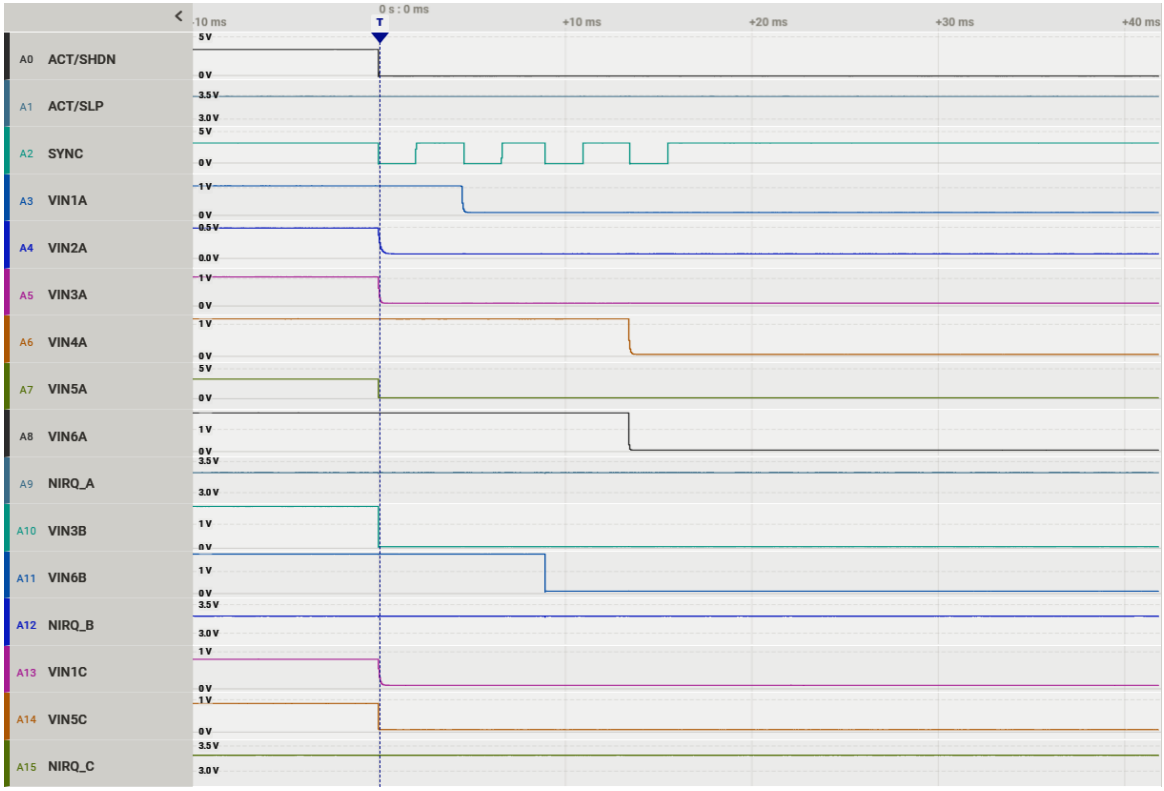


Table 5: Read Register after Timeout

		Part A		Part B		Part C	
Add.	**Register Name**	**Read Result**	**Description**	**Read Result**	**Description**	**Read Result**	**Description**
Bank 0							
0x10~ 0x24	Interrupt Information Registers	00	No interrupt after SEQ_OFF.	00	No interrupt after SEQ_OFF.	00	No interrupt after SEQ_OFF.
0x32	OFF_STAT	3F	Channels 1–6 are in an off state.	3F	Channel 3 and channel 6 are in an off state.	2E	Channel 1 and channel 5 are in an on state.
0x36	SEQ_ORD _STAT	04	4 sync pulse count.	04	4 sync pulse count.	04	4 sync pulse count.
0x40	VIN_LVL[1]	00	VIN1A < 0.2V after SEQ_OFF.	00	VIN1B < 0.8V after SEQ_OFF.	00	VIN1C < 0.2V after SEQ_OFF.
0x41	VIN_LVL[2]	00	VIN2A < 0.2V after SEQ_OFF.	00	VIN2B < 0.8V after SEQ_OFF.	00	VIN2C < 0.8V after SEQ_OFF.
0x42	VIN_LVL[3]	00	VIN3A < 0.2V after SEQ_OFF.	00	VIN3B < 0.8V after SEQ_OFF.	00	VIN3C < 0.8V after SEQ_OFF.
0x43	VIN_LVL[4]	00	VIN4A < 0.2V after SEQ_OFF.	00	VIN4B < 0.2V after SEQ_OFF.	00	VIN4C < 0.8V after SEQ_OFF.
0x44	VIN_LVL[5]	00	VIN5A < 0.8V after SEQ_OFF.	00	VIN5B < 0.8V after SEQ_OFF.	00	VIN5C < 0.2V after SEQ_OFF.
0x45	VIN_LVL[6]	00	VIN6A < 0.8V after SEQ_OFF.	00	VIN6B < 0.8V after SEQ_OFF.	00	VIN6C < 0.2V after SEQ_OFF.
0x60	SEQ_OFF_ LOG[1]	02	The rail on VIN1A Is down in the second SYNC pulse record as the first sequence log.	00	VIN1B does not have a sequence when SEQ is off.	01	The rail on VIN1C is down in the first SYNC pulse record as the first sequence log.
0x61	SEQ_OFF_ LOG[2]	01	The rail on VIN2A is down in the first SYNC pulse record as the first sequence log.	00	VIN2B does not have a sequence when SEQ is off.	00	VIN2C does not have a sequence when SEQ is off.
0x62	SEQ_OFF_ LOG[3]	01	The rail on VIN3A is down in the first SYNC pulse record as the first sequence log.	01	The rail on VIN3B is down in the first SYNC pulse record as the first sequence log.	00	VIN3C does not have a sequence when SEQ is off.
0x63	SEQ_OFF_ LOG[4]	04	The rail on VIN4A is down in the fourth SYNC pulse record as the fourth sequence log.	00	VIN4B does not have a sequence when SEQ is off.	00	VIN4C does not have a sequence when SEQ is off.
0x64	SEQ_OFF_ LOG[5]	01	The rail on VIN5A is down in the first SYNC pulse record as the first sequence log.	00	VIN5B does not have a sequence when SEQ is off.	01	The rail on VIN5C is down in the first SYNC pulse record as the first sequence log.
0x65	SEQ_OFF_ LOG[6]	04	The rail on VIN6A Is Down in the fourth SYNC pulse record as the fourth sequence log.	03	The rail on VIN6B is down in the third SYNC pulse record as the third sequence log.	00	VIN6C does not have a sequence when SEQ is off.
0x90	SEQ_TIME _MSB[1]	00	The VIN1A off time is 4.6ms.	00	VIN1B does not have a sequence when SEQ is off.	00	The VIN1C off time is 0.15ms.
0x91	SEQ_TIME _LSB[1]	5C		00		03	

0x92	SEQ_TIME_MSB[2]	00	The VIN2A off time is 0.15ms.	00	VIN2B does not have a sequence when SEQ is off.	00	VIN2C does not have a sequence when SEQ is off.
0x93	SEQ_TIME_LSB[2]	03		00		00	
0x94	SEQ_TIME_MSB[3]	00	The VIN3A off time is 0.1ms.	00	The VIN3B off time is 0ms.	00	VIN3C does not have a sequence when SEQ is off.
0x95	SEQ_TIME_LSB[3]	02		00		00	
0x96	SEQ_TIME_MSB[4]	01	The VIN4A off time is 13.5ms.	00	VIN4B does not have a sequence when SEQ is off.	00	VIN4C does not have a sequence when SEQ is off.
0x97	SEQ_TIME_LSB[4]	0E		00		00	
0x98	SEQ_TIME_MSB[5]	00	The VIN5A off time is 0ms.	00	VIN5B does not have a sequence when SEQ is off.	00	The VIN5C off time is 0ms.
0x99	SEQ_TIME_LSB[5]	00		00		00	
0x9A	SEQ_TIME_MSB[6]	01	The VIN6A off time is 13.45ms.	00	The VIN6B off time is 8.9ms.	00	VIN6C does not have a sequence when SEQ is off.
0x9B	SEQ_TIME_MSB[6]	0D		B2		00	
Bank 1							
0x1E	VIN_CH_EN	3F	Channels 1–6 are all enabled.	24	Channel 3 and channel 6 are all enabled.	11	Channel 1 and channel 5 are all enabled.
0x1F	VRANGE_MULT	30	VIN1–VIN4 are 1x scaling, VIN5 and VIN6 are 4x scaling.	37	VIN3 and VIN6 are 4x scaling.	37	VIN1 and VIN5 are 1x scaling.
0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.	3C	AMSK_ON for VIN3 and VIN6 is enabled.	3C	AMSK_ON for VIN1 and VIN5 is enabled.
0xA2	AMSK_OFF	3F	AMSK_OFF for VIN1–VIN6 is enabled.	3C	AMSK_OFF for VIN3 and VIN6 is enabled.	3C	AMSK_OFF for VIN1 and VIN5 is enabled.
0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 re enabled.	20	AMSK_EXS for VIN6 is enabled, AMSK_EXS for VIN3 is disabled.	20	AMSK_EXS for VIN1 and VIN5 is enabled.
0xA4	AMSK_ENS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_ENS for VIN6 is enabled, AMSK_ENS for VIN3 is disabled.	20	AMSK_ENS for VIN1 and VIN5 is enabled.
0xA5	SEQ_TOUT_MSB	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.
0xA6	SEQ_TOUT_LSB	25		25		25	
0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.
0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.
0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.
0xC0	SEQ_OFF_EXP[1]	02	The expected sequence log for VIN1A is 2.	00	The expected sequence log for VIN1B is 0.	01	The expected sequence log for VIN1C is 1.
0xC1	SEQ_OFF_EXP[2]	01	The expected sequence log for VIN2A is 1.	00	The expected sequence log for VIN2B is 0.	00	The expected sequence log for VIN2C is 0.

0xC2	SEQ_OFF_EXP[3]	01	The expected sequence log for VIN3A is 1.	01	The expected sequence log for VIN3B is 1.	00	The expected sequence log for VIN3C is 0.
0xC3	SEQ_OFF_EXP[4]	04	The expected sequence log for VIN4A is 4.	00	The expected sequence log for VIN4B is 0.	00	The expected sequence log for VIN4C is 0.
0xC4	SEQ_OFF_EXP[5]	01	The expected sequence log for VIN5A is 1.	00	The expected sequence log for VIN5B is 0.	01	The expected sequence log for VIN5C is 1.
0xC5	SEQ_OFF_EXP[6]	04	The expected sequence log for VIN6A is 4.	03	The expected sequence log for VIN6B is 3.	00	The expected sequence log for VIN6C is 0.

SEQ Sleep Entry Monitoring with Multiple MPQ79500FS Devices

Three MPQ79500FS devices, ACT/SHDN = high, ACT/SLP = high to low

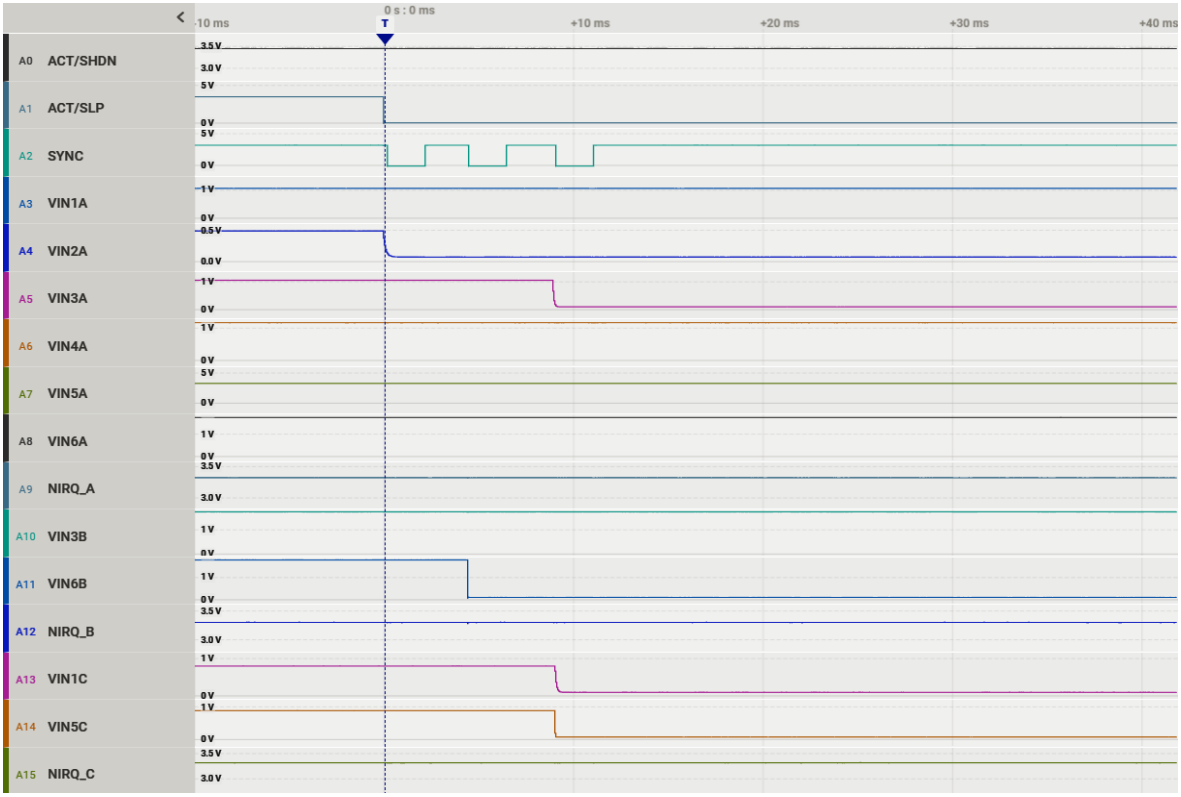


Table 6: Read Register after Timeout

		Part A		Part B		Part C	
Add.	**Register Name**	**Read Result**	**Description**	**Read Result**	**Description**	**Read Result**	**Description**
Bank 0							
0x10~0x24	Interrupt Information Registers	00	No interrupt after SEQ_ENS.	00	No interrupt after SEQ_ENS.	00	No interrupt after SEQ_ENS.
0x32	OFF_STAT	00	Channels 1–6 are in the on state.	3B	Channel 3 is in the on state; the other channels are off.	3F	Channels 1–6 are in the off state.
0x36	SEQ_ORD_STAT	03	3 sync pulse count.	03	3 sync pulse count.	03	3 sync pulse count.
0x40	VIN_LVL[1]	AA	1.05V.	00	VIN1B < 0.8V after SEQ_ENS.	00	VIN1C < 0.2V after SEQ_ENS.
0x41	VIN_LVL[2]	3D	VIN2A < 0.2V after SEQ_ENS.	00	VIN2B < 0.8V after SEQ_ENS.	00	VIN2C < 0.8V after SEQ_ENS.
0x42	VIN_LVL[3]	00	VIN3A < 0.2V after SEQ_ENS.	32	1.8V.	00	VIN3C < 0.8V after SEQ_ENS.
0x43	VIN_LVL[4]	C8	1.2V.	00	VIN4B < 0.2V after SEQ_ENS.	00	VIN4C < 0.8V after SEQ_ENS.
0x44	VIN_LVL[5]	7B	3.26V.	00	VIN5B < 0.8V after SEQ_ENS.	00	VIN5C < 0.2V after SEQ_ENS.
0x45	VIN_LVL[6]	32	1.8V.	00	VIN6B < 0.8V after SEQ_ENS.	00	VIN6C < 0.2V after SEQ_ENS.
0x80	SEQ_ENS_LOG[1]	00	VIN1A does not have a sequence during SEQ_ENS.	00	VIN1B does not have a sequence during SEQ_ENS.	03	The rail on VIN1C is down in the third SYNC pulse record as the third sequence log.
0x81	SEQ_ENS_LOG[2]	01	The rail on VIN2A is down in the first SYNC pulse record as the first sequence log.	00	VIN2B does not have a sequence during SEQ_ENS.	00	VIN2C does not have a sequence during SEQ_ENS.
0x82	SEQ_ENS_LOG[3]	03	The rail on VIN3A is down in the third SYNC pulse record as the third sequence log.	00	VIN3B does not have a sequence during SEQ_ENS.	00	VIN3C does not have a sequence during SEQ_ENS.
0x83	SEQ_ENS_LOG[4]	00	VIN4A does not have a sequence during SEQ_ENS.	00	VIN4B does not have a sequence during SEQ_ENS.	00	VIN4C does not have a sequence during SEQ_ENS.
0x84	SEQ_ENS_LOG[5]	00	VIN5A does not have a sequence during SEQ_ENS.	00	VIN5B does not have a sequence during SEQ_ENS.	03	The rail on VIN5C is down in the third SYNC pulse record as the third sequence log.
0x85	SEQ_ENS_LOG[6]	00	VIN6A does not have a sequence during SEQ_ENS.	02	The rail on VIN6B is down in the second SYNC pulse record as the second sequence log.	00	VIN6C does not have a sequence during SEQ_ENS.
0x90	SEQ_TIME_MSB[1]	00	VIN1A does not have a sequence during SEQ_ENS.	00	VIN1B does not have a sequence during SEQ_ENS.	00	The VIN1C off time is 9.15ms.
0x91	SEQ_TIME_LSB[1]	00		00		B7	
0x92	SEQ_TIME_MSB[2]	00	The VIN2A off time is 0.15ms.	00	VIN2B does not have a sequence during SEQ_ENS.	00	VIN2C does not have a sequence during SEQ_ENS.
0x93	SEQ_TIME_LSB[2]	03		00		00	

0x94	SEQ_TIME_MSB[3]	00	The VIN3A off time is 9.05ms.	00	VIN3B does not have a sequence during SEQ_ENS.	00	VIN3C does not have a sequence during SEQ_ENS.
0x95	SEQ_TIME_LSB[3]	B5		00		00	
0x96	SEQ_TIME_MSB[4]	00	VIN4A does not have a sequence during SEQ_ENS, but VIN5 does.	00	VIN4B does not have a sequence during SEQ_ENS.	00	VIN4C does not have a sequence during SEQ_ENS.
0x97	SEQ_TIME_LSB[4]	00		00		00	
0x98	SEQ_TIME_MSB[5]	00	VIN6A and VIN4A do not have a sequence during SEQ_ENS.	00	VIN5B does not have a sequence during SEQ_ENS.	00	The VIN5C off time is 9.05ms.
0x99	SEQ_TIME_LSB[5]	00		00		B5	
0x9A	SEQ_TIME_MSB[6]	00	VIN5A does not have a sequence during SEQ_ENS.	00	The VIN6B off of is 4.45ms.	00	VIN6C does not have a sequence during SEQ_ENS.
0x9B	SEQ_TIME_MSB[6]	00		59		00	
Bank 1							
0x1E	VIN_CH_EN	3F	Channels 1–6 are all enabled.	24	Channel 3 and channel 6 are enabled.	11	Channel 1 and channel 5 are enabled.
0x1F	VRANGE_MULT	30	VIN1–VIN4 are 1x scaling, VIN and VIN6 are 4x scaling.	37	VIN3 and VIN6 are 4x scaling.	37	VIN1 and VIN5 are 1x scaling.
0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.	3C	AMSK_ON for VIN3 and VIN6 is enabled.	3C	AMSK_ON for VIN1 and VIN5 is enabled.
0xA2	AMSK_OFF	3F	AMSK_OFF for VIN1–VIN6 is enabled.	3C	AMSK_OFF for VIN3 and VIN6 is enabled.	3C	AMSK_OFF for VIN1 and VIN5 is enabled.
0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_EXS for VIN6 is enabled, AMSK_EXS for VIN3 is disabled.	20	AMSK_EXS for VIN1 and VIN5 is enabled.
0xA4	AMSK_ENS	06	AMSK ENS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_ENS for VIN6 is enabled, AMSK_ENS for VIN3 is disabled.	20	AMSK_ENS for VIN1 and VIN5 is enabled.
0xA5	SEQ_TOUT_MSB	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.
0xA6	SEQ_TOUT_LSB	25		25		25	
0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.
0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.
0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.
0xE0	SEQ_ENS_EXP[1]	00	The expected sequence log for VIN1A is 0.	00	The expected sequence log for VIN1B is 0.	03	The expected sequence log for VIN1C is 3.
0xE1	SEQ_ENS_EXP[2]	01	The expected sequence log for VIN2A is 1.	00	The expected sequence log for VIN2B is 0.	00	The expected sequence log for VIN2C is 0.
0xE2	SEQ_ENS_EXP[3]	03	The expected sequence log for VIN3A is 3.	00	The expected sequence log for VIN3B is 0.	00	The expected sequence log for VIN3C is 0.
0xE3	SEQ_ENS_EXP[4]	00	The expected sequence log for VIN4A is 0.	00	The expected sequence log for VIN4B is 0.	00	The expected sequence log for VIN4C is 0.
0xE4	SEQ_ENS_EXP[5]	00	The expected sequence log for VIN5A is 0.	00	The expected sequence log for VIN5B is 0.	03	The expected sequence log for VIN5C is 3.
0xE5	SEQ_ENS_EXP[6]	00	The expected sequence log for VIN6A is 0.	02	The expected sequence log for VIN6B is 2.	00	The expected sequence log for VIN6C is 0.

SEQ Sleep Exit Monitoring with Multiple MPQ79500FS Devices

Three MPQ79500FS devices, ACT/SHDN = high, ACT/SLP = low to high

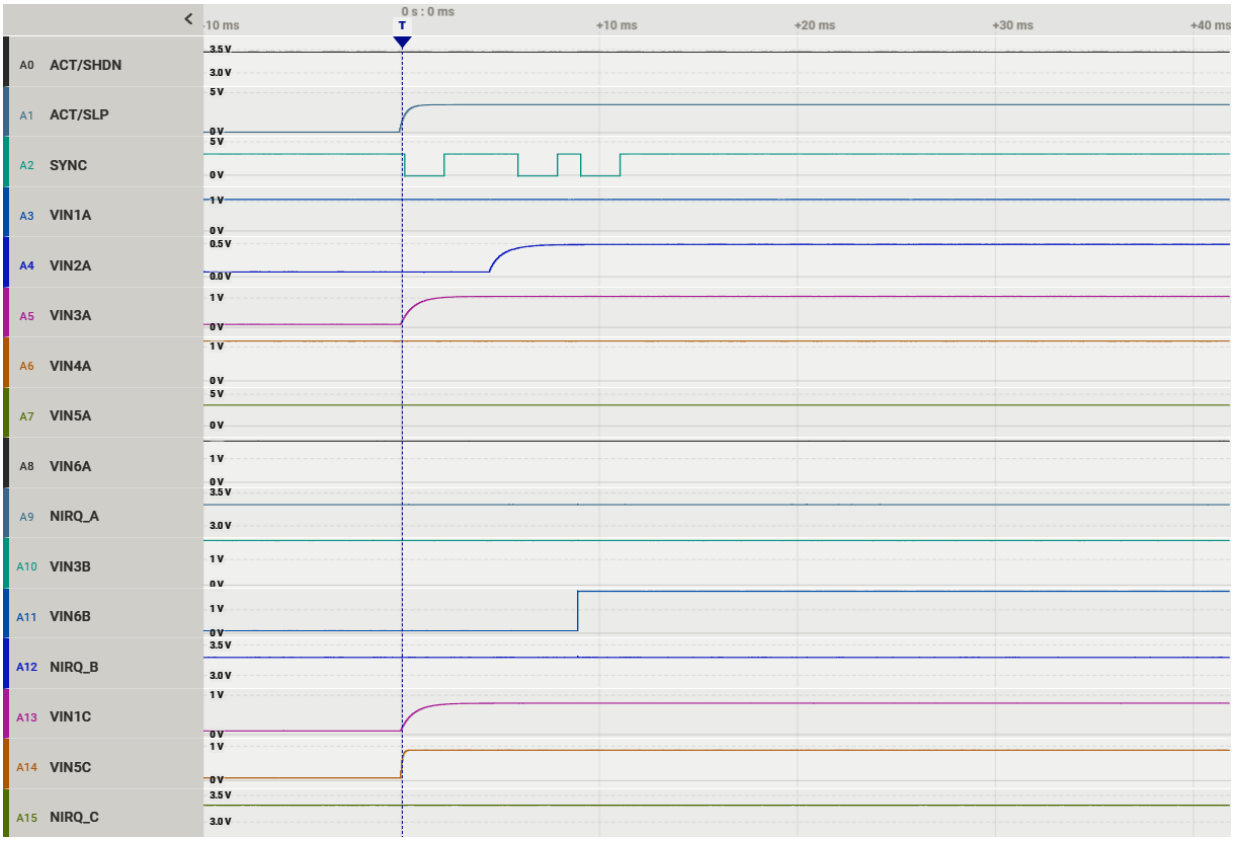


Table 7: Read Register after Timeout

		Part A		Part B		Part C	
Add.	**Register Name**	**Read Result**	**Description**	**Read Result**	**Description**	**Read Result**	**Description**
Bank 0							
0x10 - 0x24	Interrupt Information Registers	00	No interrupt after SEQ_EXS.	00	No interrupt after SEQ_EXS.	00	No interrupt after SEQ_EXS.
0x32	OFF_STAT	06	Channels 1, 4, 5, and 6 are in the on state; channel 2 and channel 3 are in the off state.	1B	Channels 3 and 6 are in the on state; channels 1, 2, 4, and 5 are in the off state.	2E	Channels 1 and 5 are in the on state; channels 2, 3, 4, and 6 are in the off state.
0x36	SEQ_ORD_STAT	03	3 sync pulse count.	03	3 sync pulse count.	03	3 sync pulse count.
0x40	VIN_LVL[1]	AC	VIN1A is 1.06V in the active state after SEQ_EXS.	00	VIN1B < 0.8V.	78	0.8V.
0x41	VIN_LVL[2]	3D	VIN2A is 0.505V in the active state after SEQ_EXS.	00	VIN2B < 0.8V.	00	VIN2C < 0.8V.
0x42	VIN_LVL[3]	AA	VIN3A is 1.05V in the active state after SEQ_EXS.	32	1.8V.	00	VIN3C < 0.8V.
0x43	VIN_LVL[4]	C8	VIN4A is 1.2V in the active state after SEQ_EXS.	00	VIN4B < 0.2V.	00	VIN4C < 0.8V.

0x44	VIN_LVL[5]	7B	VIN5A is 3.26V in the active state after SEQ_EXS.	00	VIN5B < 0.8V.	8C	0.9V.
0x45	VIN_LVL[6]	32	VIN6A is 1.8V in the active state after SEQ_EXS.	32	1.8V.	00	VIN6C < 0.2V.
0x70	SEQ_EXS_LOG[1]	00	VIN1A does not have a sequence during SEQ_EXS.	00	VIN1B does not have a sequence during SEQ_EXS.	01	The rail on VIN1C is up in the first SYNC pulse record as the first sequence log.
0x71	SEQ_EXS_LOG[2]	02	The rail on VIN2A is up in the second SYNC pulse record as the second sequence log.	00	VIN2B does not have a sequence during SEQ_EXS.	00	VIN2C does not have a sequence during SEQ_EXS.
0x72	SEQ_EXS_LOG[3]	01	The rail on VIN3A is up in the first SYNC pulse record as the first sequence log.	00	VIN3B does not have a sequence during SEQ_EXS.	00	VIN3C does not have a sequence during SEQ_EXS.
0x73	SEQ_EXS_LOG[4]	00	VIN4A does not have a sequence during SEQ_EXS.	00	VIN4B does not have a sequence during SEQ_EXS.	00	VIN4C does not have a sequence during SEQ_EXS.
0x74	SEQ_EXS_LOG[5]	00	VIN5A does not have a sequence during SEQ_EXS.	00	VIN5B does not have a sequence during SEQ_EXS.	01	The rail on VIN5C is up in the first SYNC pulse record as the first sequence log.
0x75	SEQ_EXS_LOG[6]	00	VIN6A does not have a sequence during SEQ_EXS.	03	The rail on VIN6B is up in the third SYNC pulse record as the third sequence log.	00	VIN6C does not have a sequence during SEQ_EXS.
0x90	SEQ_TIME_MSB[1]	00	VIN1A does not have a sequence during SEQ_EXS.	00	VIN1B does not have a sequence during SEQ_EXS.	00	The VIN1C up time is 1.5ms.
0x91	SEQ_TIME_LSB[1]	00		00		1E	
0x92	SEQ_TIME_MSB[2]	00	The VIN2A up time is 0.15ms.	00	VIN2B does not have a sequence during SEQ_EXS.	00	VIN2C does not have a sequence during SEQ_EXS.
0x93	SEQ_TIME_LSB[2]	75		00		00	
0x94	SEQ_TIME_MSB[3]	00	The VIN3A up time is 9.05ms.	00	VIN3B does not have a sequence during SEQ_EXS.	00	VIN3C does not have a sequence during SEQ_EXS.
0x95	SEQ_TIME_LSB[3]	1D		00		00	
0x96	SEQ_TIME_MSB[4]	00	VIN4A does not have a sequence during SEQ_EXS.	00	VIN4B does not have a sequence during SEQ_EXS.	00	VIN4C does not have a sequence during SEQ_EXS.
0x97	SEQ_TIME_LSB[4]	00		00		00	
0x98	SEQ_TIME_MSB[5]	00	VIN5A does not have a sequence during SEQ_EXS.	00	VIN5B does not have a sequence during SEQ_EXS.	00	The VIN5C up time is 0.15ms.
0x9A	SEQ_TIME_MSB[6]	00	VIN6A does not have sequence when SEQ_EXS.	00	The VIN6B up time is 9.05ms.	00	VIN6C do not have sequence when SEQ_EXS.
0x9B	SEQ_TIME_MSB[6]	00		B5		00	
Bank 1							
0x1E	VIN_CH_EN	3F	Channels 1–6 are all enabled.	24	Channels 3 and 6 are enabled.	11	Channels 1 and 5 are enabled.
0x1F	VRANGE_MULT	30	VIN1–4 are 1x scaling, VIN5 and VIN6 are 4x scaling.	37	VIN3 and VIN6 are 4x scaling.	37	VIN1 and VIN5 are 1x scaling.
0xA1	AMSK_ON	3F	AMSK_ON for VIN1–VIN6 is enabled.	3C	AMSK_ON for VIN3 and VIN6 is enabled.	3C	AMSK_ON for VIN1 and VIN5 is enabled.

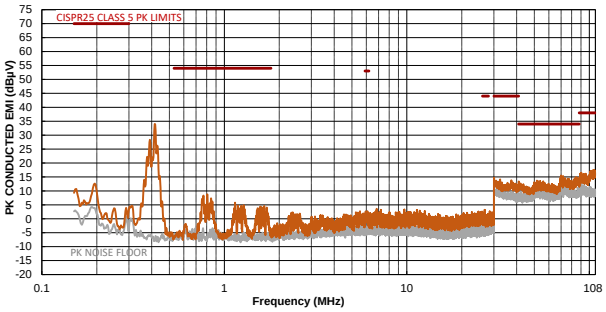
0xA2	AMSK_OFF	3F	AMSK_OFF for VIN1–VIN6 is enabled.	3C	AMSK_OFF for VIN3 and VIN6 is enabled.	3C	AMSK_OFF for VIN1 and VIN5 is enabled.
0xA3	AMSK_EXS	06	AMSK_EXS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_EXS for VIN6 is enabled, AMSK_EXS for VIN3 is disabled.	20	AMSK EXS for VIN1 and VIN5 is enabled.
0xA4	AMSK_ENS	06	AMSK_ENS for VIN1, VIN4, VIN5, and VIN6 is enabled.	20	AMSK_ENS for VIN6 is enabled, AMSK_ENS for VIN3 is disabled.	20	AMSK ENS for VIN1 and VIN5 is enabled.
0xA5	SEQ_TOUT_MSB	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.	00	The timeout is set to 38ms.
0xA6	SEQ_TOUT_LSB	25		25		25	
0xA7	SEQ_SYNC	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.	C3	PULSE_WIDTH is set to 2000µs.
0xA8	SEQ_UP_THLD	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.	3F	The UP rail threshold is the UV threshold.
0xA9	SEQ_DN_THLD	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.	00	The OFF rail threshold is the OFF threshold.
0xD0	SEQ_EXS_EXP[1]	00	The expected sequence log for VIN1A is 0.	00	The expected sequence log for VIN1B is 0.	01	The expected sequence log for VIN1C is 1.
0xD1	SEQ_EXS_EXP[2]	02	The expected sequence log for VIN2A is 2.	00	The expected sequence log for VIN2B is 0.	00	The expected sequence log for VIN2C is 0.
0xD2	SEQ_EXS_EXP[3]	01	The expected sequence log for VIN3A is 1.	00	The expected sequence log for VIN3B is 0.	00	The expected sequence log for VIN3C is 0.
0xD3	SEQ_EXS_EXP[4]	00	The expected sequence log for VIN4A is 0.	00	The expected sequence log for VIN4B is 0.	00	The expected sequence log for VIN4C is 0.
0xD4	SEQ_EXS_EXP[5]	00	The expected sequence log for VIN5A is 0.	00	The expected sequence log for VIN5B is 0.	01	The expected sequence log for VIN5C is 1.
0xD5	SEQ_EXS_EXP[6]	00	The expected sequence log for VIN6A is 0.	03	The expected sequence log for VIN6B is 3.	00	The expected sequence log for VIN6C is 0.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. Circuit includes first-stage power supply from 12V battery to second-stage EVB. (2) V_{DD} = 5V, V_{PU} = 5V, T_A = 25°C, unless otherwise noted.

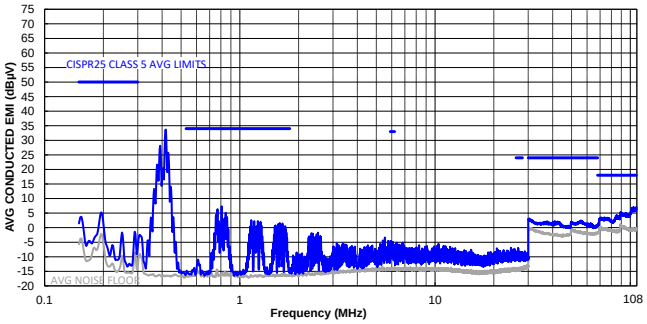
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



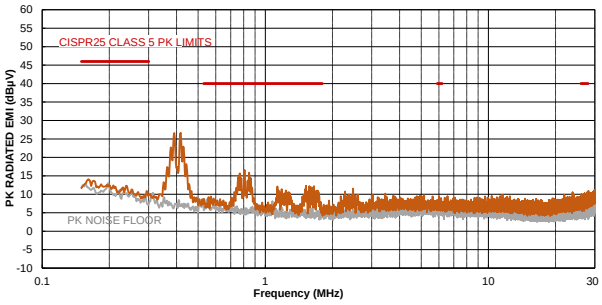
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



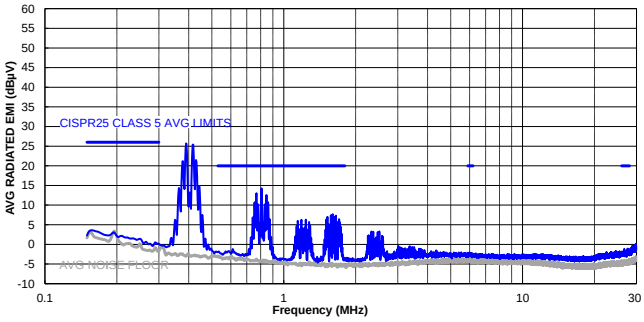
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



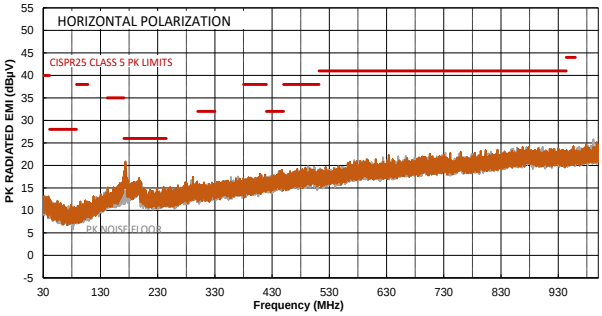
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



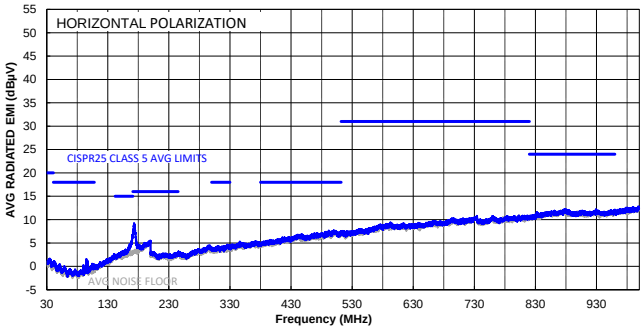
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

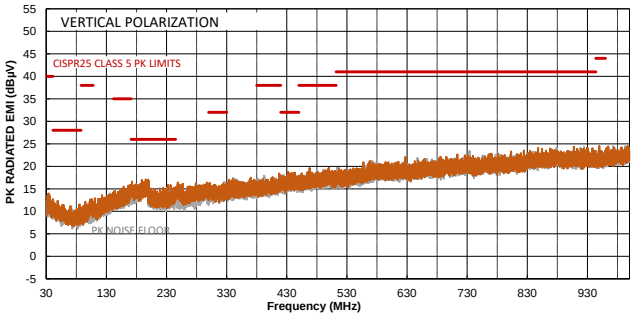


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. Circuit includes first-stage power supply from 12V battery to the second-stage EVB. (2) V_{DD} = 5V, V_{PU} = 5V, T_A = 25°C, unless otherwise noted.

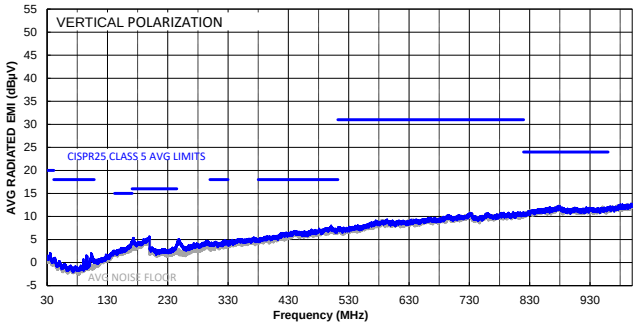
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

2) Contact MPS for more details.

PCB LAYOUT (3)

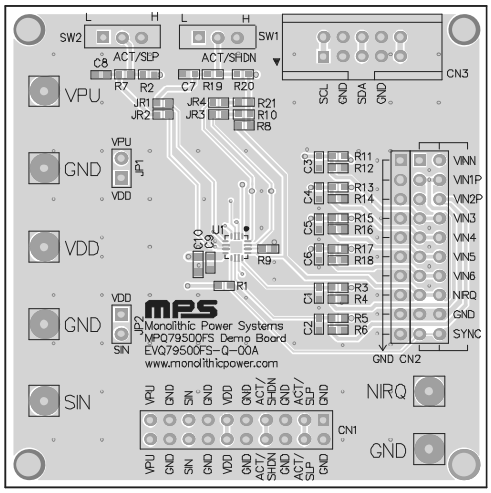


Figure: 4 Top Silk and Top Layer

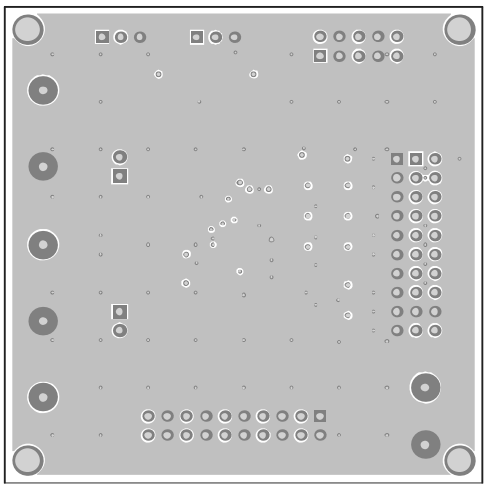


Figure 5: Mid-Layer 1

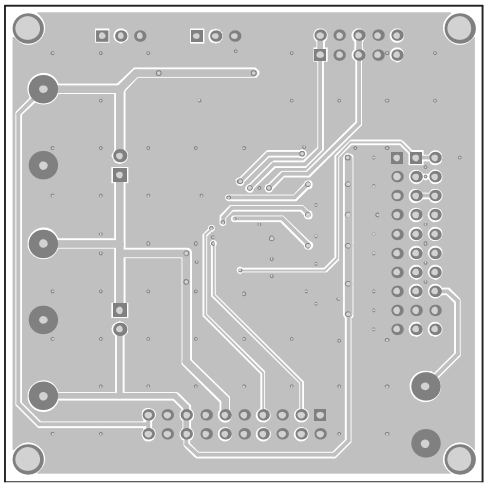


Figure 6: Mid-Layer 2

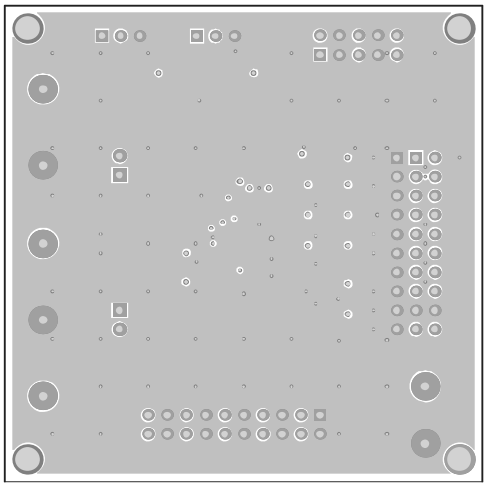


Figure 7: Bottom Layer and Bottom Silk

Note:

3) The EVQ79500FS-Q-00A is a 4-layer, 2oz copper thickness PCB.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/3/2022	Initial Release	-