# Product Change Notification: SYST-05CFNU141

## Date:

07-Feb-2025

## Product Category:

Wireless IC, Wireless Modules

## Notification Subject:

PIC32CX-BZ2 Family Silicon Errata Sheet

## Affected CPNs:

**SYST-05CFNU141_Affected_CPN_02072025.pdf**
**SYST-05CFNU141_Affected_CPN_02072025.csv**

## Notification Text:

| SYST-05CFNU141 |
| --- |
| Microchip has released a new Document for the PIC32CX-BZ2 Family Silicon Errata Sheet of devices. If you are using one of these devices please read the document located at **PIC32CX-BZ2 Family Silicon Errata Sheet**.<br><br>**Notification Status:** Final<br><br>**Description of Change:**<br><br>Overview, Silicon Errata<br><br>Summary, Silicon Errata<br><br>Issues<br><br>Added errata information that are applicable for the WBZ451PE-E device |

Data Sheet Clarifications • Added information on Wake-up Timing Specification for Low Power Modes

• Updated information on ADC Single-Ended Mode

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity.

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 07 Feb 2025

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

**PIC32CX-BZ2 Family Silicon Errata Sheet**

Please contact your local **Microchip sales office** with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC32CX1012BZ25048-E/MYX
PIC32CX1012BZ25048-I/MYX
PIC32CX1012BZ25048T-IA0/MYX
PIC32CX1012BZ25048T-IA2/MYX
PIC32CX1012BZ25048T-I/MYX
PIC32CX1012BZ25048T-E/MYX
PIC32CX1012BZ24032-E/S8B
PIC32CX1012BZ24032-I/S8B
PIC32CX1012BZ24032T-I/S8B
PIC32CX1012BZ24032T-E/S8B
WBZ451PE-E
WBZ451HPE-I
WBZ451HUE-I
WBZ451PE-I
WBZ451UE-I
WBZ451PE-IA2
WBZ451UE-IA2
WBZ450PE-I
WBZ450UE-I

# PIC32CX-BZ2 Family Silicon Errata Sheet

## PIC32CX-BZ2 Family

www.microchip.com Product Pages: PIC32CX1012BZ24032, PIC32CX1012BZ25048, WBZ450PE, WBZ450UE, WBZ451HPE, WBZ451HUE, WBZ451PE, WBZ451PE-E, WBZ451UE

## Overview

The PIC32CX-BZ2 family of devices that you received conform functionally to the current device data sheet, except for the anomalies described in this document.

The silicon issues discussed and summarized in the following pages are for silicon revisions with the device and revision IDs listed in the following table.

The errata described in this document will be addressed in future revisions of the PIC32CX-BZ2 family silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

**Table 1.** PIC32CX-BZ2 Family Silicon Device Identification

| Revision | Part Number | Device Identification (DID[31:0]) | Revision ID (DID.REVISION[3:0]) |
|---|---|---|---|
| A0 | PIC32CX1012BZ25048/WBZ451 | 0x0FBF9B8F | 0x00 |
| A2 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | 0x2FBF9B8F | 0x02 |
| A2 | PIC32CX1012BZ24032/WBZ450 | 0x2FBF9B0B | 0x02 |

**Note:** Refer to the *Device Service Unit* chapter in the current device data sheet for detailed information on device identification and revision IDs for your specific device.

# Table of Contents

# 1. Silicon Errata Summary

**Table 1-1.** Errata Summary

| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| Supply Voltage and Power Mode | GPIO Output Configuration in Deep Sleep and Extreme Deep Sleep | In Deep Sleep and Extreme Deep Sleep modes, GPIO must not be set to the output state of pin HIGH.<br>Configuring the GPIO state to pin High during Deep Sleep and Extreme Deep Sleep modes will cause leakage current and potential reliability issues on the Silicon.<br>This issue is only applicable when the system is in Deep Sleep/Extreme Deep Sleep mode and when GPIO is configured as output state pin HIGH. | X | | |
| | POR Rearm Event | The POR event is not getting triggered even when the voltage is going below 1.45V. | X | X | X |
| Analog-to-Digital Converter (ADC) | Level Trigger | The ADC level trigger does not perform burst conversions in Debug mode. | X | X | X |
| | Scan | The Scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and do not generate an EOSRDY bit (ADCCON2[29]) end of scan interrupt status if a new trigger event from the STRGSRC[4:0] bits (ADCCON1[20:16]) trigger source occurs before the scan list completion on the shared ADC2 core. | X | X | X |
| | Incorrect VDD33/2 for ADC Internal Input Channel AN11 | The ADC internal input channel, AN11, is connected with VDD33/2, but the observed input voltage is<br>not equal to VDD/2. | X | | |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| Analog Comparator (AC) | Disabling Analog Comparator | Analog Comparator output (AC_CMPx) will not be disabled by setting either COMPCTRLx.ENABLE = 0 or PMD1.ACMD = 1. | X | X | X |
| | Incorrect VDD Scaler Reference for AC_CMP0 | AC_CMP0 is supposed to use a fixed VDD/2 reference when VDD scaler option is used. But the observed reference voltage is not equal to VDD/2. | X | | |
| | Incorrect VDD Scaler Reference with CMP0 and CMP1 Enabled Concurrently | Incorrect VDD scaler reference voltage is observed when AC_CMP0 and AC_CMP1 are enabled concurrently with the VDD scaler as a reference for both the comparators. Both the comparators will see the same VDD scaler reference. | X | | |
| Clock Reset Unit (CRU) | Peripheral Bus Clocks | The Power-on Reset (POR) value of the PB3 clock is not correct. | X | X | X |
| Configurable Custom Logic (CCL) | Enable Protected Registers | The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit; however, they should be enable-protected by the LUTCTRLx.ENABLE bits. | X | X | X |
| | Output Logic is Stuck when Enabling a LUT with Sequential Logic after the CCL is Enabled | When the LUT is disabled (LUTCTRL0.ENABLE=0 or LUTCTRL2.ENABLE=0) to clear the flip-flop/latch output and enabled again, the sequential logic is kept under Reset. | X | X | X |
| | PAC Error when Writing CCL.CTRL.SWRST Bit | Writing the Software Reset bit in the Control A register (CTRLA.SWRST) will trigger a PAC protection error. | X | X | X |
| | Sequential Logic | LUT output is corrupted after enabling CCL when sequential logic is used. | X | X | X |
| Device | VIL Input Low Voltage | There is degraded VIL/VIH performance when the GPIO pull-up/pull-down resistors are enabled on PB0, PB1, PB2, PB3,PB4, PB5, PB6, PB8 or PB9. These pins may not be able to recognize a logic low level if the pull-up on that pad is enabled. | X | | |
| | VDD min for A0 device is 2.1V | Some A0 devices may not operate below 2.1V. | X | | |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| Device Service Unit (DSU) | Programming or Debugging | Device debugging and programming is not supported when the device's supply voltage is greater than 3.0V and the device is operating outside of room temperature. | X | | |
| | CRC32 | DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled. | X | X | X |
| Direct Memory Access Controller (DMAC) | DMAC in Debug Mode | In debug mode, DMAC does not restart after a debug halt when DBGCTRL.DBGRUN = 0. | X | X | X |
| | DMA Writeback Descriptor Corruption Issue | Aborting or disabling a DMA channel could lead to a corruption issue in the writeback descriptor of an active channel where there are ongoing transfers. | X | X | X |
| | Occurrence of Fetch Error | When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) may occur on enabling a channel with no linked descriptor or when one of the already active channels using linked descriptors may fetch the enabled second descriptor (index 1) of the channel.<br>These errors can occur when a channel is enabled during the link request of another channel and if the channel number of the enabled channel is lower than the already active channel. | X | X | X |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| External Interrupt Controller (EIC) | Edge Detection | When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K). | X | X | X |
| | Asynchronous Edge Detection | When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up. | X | X | X |
| | Asynchronous Edge Detection | When the asynchronous edge detection is enabled (without debouncer) and the system is in the Standby Sleep mode, only the first edge will generate an event. The edges following the first edge of the waveform do not generate events until the system wakes up. | X | X | X |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| Event System (EVSYS) | Software Event | BUSYCH flag never resets upon software events in synchronous/ resynchronized path modes with event detection on falling edges.<br>If a software event occurs when the EVSYS is set in synchronous/ resynchronized path modes (CHANNELn.PATH=0x0/0x1) with event detection set on falling edges (CHANNELn.EDGSEL=0x2), the CHSTATUS.BUSYCHn flag will be set but will never come back to 0. It is, then, impossible to know if the event user for this channel is ready to accept new events or not. | X | X | X |
| | Spurious Overrun | Overrun interrupt flag may be incorrectly set upon software events in synchronous/ resynchronized path modes with event detection on both rising and falling edges.<br>If a software event occurs when the EVSYS is set in synchronous/ resynchronized path modes (CHANNELn.PATH=0x0/0x1) with event detection set on both rising and falling edges (CHANNELn.EDGSEL=0x3), spurious overrun interrupts may occur (INTFLAG.OVRn). | X | X | X |
| | Spurious Overrun | In the Synchronous mode, spurious overrun interrupts can happen when the generic clock for a channel is always CHANNEL.ONDEMAND=0. | X | X | X |
| Flash Controller Module | SYS Reset Not Getting Released when Asserted Post-Erase Retry | After the Erase Retry operation (using NVMCON2.VREAD1=1), all the operations work as expected until a SYS Reset is asserted. When the SYS Reset is asserted post-Erase Retry, the Reset is stuck and not getting released. | X | X | X |
| | DMA in Sleep Mode | Flash read/write by DMA not working in Standby Sleep mode if Flash power down is enabled. | X | | |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| Frequency Meter (FREQM) | Measurement Clock Stalls | During a measurement slot, the measurement clock stalls (or is very slow), the STATUS.BUSY will never de-assert and the DONE interrupt will not be raised. | X | X | X |
| I²C | SCL/SDA Transition Time | SCL/SDA minimum transition time is not met in Fast-mode plus (1 MHz). | X | X | X |
| Peripheral Access Controller (PAC) | PAC Protection Error in FREQM | FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error. | X | X | X |
| | PAC Protection Error in CCL | Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error. | X | X | X |
| Prefetch Cache | CPU Hang Configuration Switch | CHECON.ADRWS is not hard wired to '0' and is configurable to 1 or 0, with reset/default value as 1. CPU hangs when CHECON.ADRWS configuration switches from 1 to 0 and a Flash read access. While CHECON.ADRWS is switching to '0' (default is '1'), the ADRWS will be latched at next clock, and if a Flash read access happens at the same clock, the system hangs waiting for an internal ack due to the PFM cache miss. | X | | |
| Quad I/O Serial Peripheral Interface (QSPI) | QSPI Status Register Bits Not Updated when PB-Bridge-B (PB2_CLK) is Not Equal to System Clock (SYS_CLK) | If PB2_CLK is not equal to System Clock (sys_clk), the QSPI Status register bits are not updated. | X | X | X |
| RAM Error Correction Code (ECC) | ERRADDR Register may Read as '0' when PB-Bridge-B (PB2_CLK) is Not Equal to System Clock (SYS_CLK) | If PB2_CLK is not equal to System Clock (sys_clk), ERRADDR register read will not return the failing address (caused by Single Bit Error/Dual Bit Error), instead it may return '0'. | X | X | X |
| Real-Time Counter (RTC) | False Tamper Detection | False tamper detections may occur when configuring the RTC INn and OUTn pins. | X | X | X |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| | Incorrect Periodic Daily Event at 23:59:58 | Periodic Delay Event must be asserted at the end of the prescaler period to be generated on the last second of the day. As the prescaler overflow does not qualify the Periodic Delay Event, the event is generated at the beginning of the prescaler period, hence, one second earlier than specified. | X | X | X |
| | Reset of General Purpose Registers on Tamper Detection | General Purpose Registers n (GPn) are Reset on tamper detection even if GPTRST = 0. | X | X | X |
| | Reset of INTFLAG.TAMPER Bit Fails | When DMA is enabled (CTRLB.DMAEN=1), the INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register. | X | X | X |
| | RTC SYNCBUSY Register Bits Not Cleared | Entering the Deep Sleep mode without waiting for SYNCBUSY.ENABLE and SYNCBUSY.COUNTSYNC synchronization completion may freeze these bits statuses. | X | X | X |
| | Timestamp is Updated Even Tamper Flag is Not Cleared | When the tamper happens, DMA is triggered and DMA captures TIMESTAMP and TAMPID. INTFLAG.TAMPER flag is not cleared after reading TIMESTAMP. | X | X | X |
| | Timestamp Register is Cleared After Debug Read | The read of the RTC timestamp register in Debug mode will clear the DMA request flag and unlock the TIMESTAMP register, although a debug read does not alter the TIMESTAMP value. Further read of timestamp register by DMA or CPU will return 0x00 because the TIMESTAMP is an RTC core register and can be read only when locked after a capture. | X | X | X |
| | Write Corruption | An 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register, can fail for the following registers:<br>• The COUNT register in COUNT32 mode<br>• The COUNT register in COUNT16 mode<br>• The CLOCK register in CLOCK mode | X | X | X |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| | COUNTSYNC | When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and, therefore, it is a wrong value. | X | X | X |
| | Tamper Input Filter | Majority debouncing, as part of RTC tamper detection, does not work when enabled by setting the Debouncer Majority Enable bit CTRLB.DEBMAJ. | X | X | X |
| | Tamper Detection | Upon enabling the RTC, a false tamper detection could be reported by the RTC. | X | X | X |
| | Tamper Detection Timestamp | If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when the next tamper detection is triggered. | X | X | X |
| | Unwanted Event and Interrupt Generation | When CTRLA.PRESCALER is set to OFF and either CTRLB.RTCOUT is set or one of the TAMCTRL.DEBNCn bits is set, the RTC prescaler behaves like CTRLA.PRESCALER = DIV1. The periodic events and periodic interrupts will be generated. | X | X | X |
| Serial Communication Interface (SERCOM) | Two Stop Bits Mode is Not Supported in SERCOM USART LIN Host Mode | Two stop bits mode (CTRLB.SBMODE=0x1) is not supported in SERCOM USART LIN Host mode (CTRLA.FORM=0x2) in the case where break, sync and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD=0x2). Only one stop bit mode is supported. | X | X | X |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/ WBZ451H/ WBZ451PE-E | PIC32CX1012BZ24032/ WBZ450 |
| | | | A0 | A2 | A2 |
| | SERCOM LIN Adding Additional Delay Between Break and Sync Bits | In SERCOM USART LIN Host mode (CTRLA.FORM=0x2), in the case where break, sync and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD=0x2), the LIN Host Header delay between the sync and the ID transmission fields is not correct for the following cases:<br>CTRLC.HDRDLY=0x2, where the delay between sync and ID transmission fields is 8-bit time instead of 4-bit time.<br>CTRLC.HDRDLY=0x3, where the delay between sync and ID transmission fields is 14-bit time instead of 4-bit time. | X | X | X |
| | SERCOM-USART: INTFLAG.TXC being Set Incorrectly | When the USART is used in the 32-bit mode with hardware handshaking (CTS/RTS), the TXC flag may be set before transmission has completed. TXC may incorrectly be set regardless of whether Data Length Enable (LENGTH.LENEN) is set to '0' or '1'. | X | X | X |
| | SERCOM-USART: Overconsumption in Standby Mode | When the SERCOM USART configured as CTRLA.RUNSTDBY = 0 and the receiver is disabled (CTRLB.RXEN = 0), the clock request to the SERCOM generic clock generator feeding the SERCOM will stay asserted during the Standby Sleep mode, leading to unexpected over consumption. | X | X | X |
| | SERCOM-USART: Flow Control in 32-bit Extension Mode | When the USART is used in the 32-bit mode with hardware handshaking (CTS/RTS), the TXC flag may be set before transmission has completed. TXC may incorrectly be set regardless of whether Data Length Enable (LENGTH.LENEN) is set to '0' or '1'. | X | X | X |
| | SERCOM-USART: Auto-Baud Mode | In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors. | X | X | X |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| | SERCOM-USART: Collision Detection | In USART operating mode with Collision Detection enabled (CTRLB.COLDEN=1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock. | X | X | X |
| | SERCOM-USART: SERCOM USART in TX Mode Only | When the SERCOM USART is configured as CTRLA.RUNSTDBY=0 and the Receiver is disabled (CTRLB.RXEN=0), the clock request to the SERCOM generic clock generator feeding the SERCOM will stay asserted during the Standby Sleep mode, leading to unexpected overconsumption. | X | X | X |
| | SERCOM-USART: Debug Mode | In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode. | X | X | X |
| | SERCOM-USART: Error Interrupts | The SERCOM USART does not wake from the Standby Sleep mode for ERROR interrupts FERR and PERR. | X | X | X |
| | SERCOM-USART: 32-bit Extension Mode | When 32-bit Extension mode is enabled and data to be sent are not in multiples of 4 bytes (which means the length counter must be enabled), additional bytes will be sent over the line. | X | X | X |
| | SERCOM-UART: TXINV and RXINV Bits | The TXINV and RXINV bits in the CTRLA register have inverted functionality. | X | X | X |
| | STATUS.CLKHOLD Bit in Host and Client Modes | The STATUS.CLKHOLD bit in host and client modes can be written; however, it is a read-only status bit. | X | X | X |
| | SERCOM-I2C: Automatic Acknowledge Feature Not Usable | The I²C client AACKEN feature is not usable when doing a repeated start. | X | X | X |
| | SERCOM-I2C: Error Interrupt after Unexpected STOP | When an unexpected STOP occurs on the I²C bus, the STATUS.BUSERR and INTFLAG.ERROR bits are set but may not wake the system from the Standby Sleep mode. An unexpected START will not produce this issue. | X | X | X |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| | SERCOM-I2C: Repeated Start Not Issued Correctly | For the Host Write operations (excluding the High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue a Repeated Start command correctly. | X | X | X |
| | SERCOM-I2C: I2C in Client Mode | In I²C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared. | X | X | X |
| | SERCOM-I2C: Client Mode with DMA | In I²C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. | X | X | X |
| | SERCOM-I2C: I2C Client in DATA32B Mode | When SERCOM is configured as an I²C client in 32-bit Data Mode (DATA32B=1) and the I²C host reads from the I²C client (client transmitter) and outputs its NACK (indicating no more data is needed), the I²C client still receives a DRDY interrupt. | X | X | X |
| | SERCOM-I2C: 10-Bit Addressing Mode | The 10-bit addressing in I²C Client mode is not functional. | X | X | X |
| | SERCOM-I2C: Repeated Start | When the quick command is enabled (CTRLB.QCEN=1), the software can issue a repeated start by writing either CTRLB.CMD or ADDR.ADDR bit fields. If, in these conditions, SCL Stretch mode is CTRLA.SCLSM=1, a bus error will be generated. | X | X | X |
| | SERCOM-SPI: Data Preload | In SPI Client mode and with Client Data Preload Enabled (CTRLB.PLOADEN=1), the first data sent from the client will be a dummy byte if the host cannot keep the Client Select (SS) line low until the end of transmission. | X | X | X |

**.....continued**

| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| | SERCOM-SPI: Client Data Preload | Preloading a new SPI data (CTRLB.PLOADEN=1) before going into Standby Sleep mode may lead to extra power consumption. | X | X | X |
| | SERCOM-SPI: Hardware Client Select Control | When Hardware Client Select Control is enabled (CTRLB.MSSEN=1), the Client Select (SS) pin goes high after. | X | X | X |
| System Bus | Bus Error Address Checks | When accessing peripherals on the PB-PIC® bus, an access beyond the implemented memory region 0x4401_FFFF will cause the CPU to hang, waiting for a bus error signal. | X | | |
| System Configuration Registers | CFGCON0 Registers | CFGCON0.SWOEN is non-functional, which makes the PB7 function SWO during debugging only. | X | | |
| | System Bus QoS | The Power-on Reset values of the CFGPGQOS register sets all bus host QoS values to zero (Background) instead of the required Power-on Reset values. | X | X | X |
| Timer/Counter for Control Applications (TCC) | Counting-down Mode Not Supported in RAMP2 | The Timer/Counter counting-down mode (CTRLBCLR.DIR = CTRLBSET.DIR = 1) is not supported in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS). | X | X | X |
| | ALOCK Feature | The ALOCK feature is not functional. | X | X | X |
| | Hi-resolution in 2RAMP Mode | In 2RAMP mode with Hi-resolution, multiple restarts can be observed when a fault occurs. | X | X | X |
| | LUPD in Descendent Mode | When the TCC is used in the Down-Counting mode, transfer of the PERBUF register value to the PER register is delayed by one counter cycle, and, therefore, the LUPD feature must not be used with the PER register. | X | X | X |

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| Module | Feature | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| | Re-trigger in RAMP2 Operations | Re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C) is not supported if a prescaler is used (CTRLA.PRESCALER != 0) and the re-trig of the counter is done on the next GCLK (CTRLA.PRESCSYNC = GCLK or CTRLA.PRESCSYNC = RESYNC). | X | X | X |
| | Re-trigger | If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted. | X | X | X |
| | TCC in Dithering Mode | Using the TCC in the Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses or shrink of left-aligned pulses. | X | X | X |
| | TCC in SYNC or RESYNC Mode | The TCC peripheral is not compatible with an EVSYS channel in the SYNC or RESYNC mode. | X | X | X |
| | TCC Outputs | TCC0/TCC1 output not working as expected with PPS, output signals not visible on output pins via PPS even though the TCC is working correctly. TCC2 cannot be used to drive external pins. | X | | |
| | MCx Interrupt Status Flag is Not Cleared Automatically | In the capture operation, MC0/MC1 interrupt status flags (INTFLAG.MC0/INTFLAG.MC1) are not automatically cleared when the CC0/CC1 registers are read. | X | X | X |
| | DMA Request is Not Set on Overflow Condition in One-shot DMA Trigger Mode of RAMP2C Operation | TCC Overflow (OVF) will not trigger a DMA request in One-shot DMA trigger (DMAOS) mode of RAMP2C operation. | X | X | X |
| Timer/Counter (TC) | Issues After Clearing STATUS.PERBUFV/STATUS.CCBUFx flag | When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value. | X | X | X |

| .....continued | | | | | |
|---|---|---|---|---|---|
| Module | Feature | Issue Summary | Affected Revisions | | |
| | | | PIC32CX1012BZ25048/WBZ451 | PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E | PIC32CX1012BZ24032/WBZ450 |
| | | | A0 | A2 | A2 |
| | Re-trigger | If a Re-trigger event (EVCTRL.EVACTn=0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted. | X | X | X |
| | MCx Interrupt Status Flag is Not Cleared Automatically | In a capture operation, MC0/MC1 interrupt status flags (INTFLAG.MC0/INTFLAG.MC1) are not automatically cleared when CC0/CC1 registers are read. | X | X | X |
| | TC.PER not updated properly | In the 8-bit mode, the PER register updates using the DMA are not possible in the Standby mode. | X | X | X |
| | TC Outputs | TC0/1/2/3 output not working as expected with PPS, output signals are not visible on output pins via PPS even though the TC is working correctly. | X | | |
| | ALOCK Feature | ALOCK feature is not functional. | X | X | X |
| Watchdog Timer (WDT) | Watchdog Counter | When the interval between clearing the watchdog timer (in other words, clearing the Run mode watchdog counter) and the sleep instruction is less than 1 WDT clock cycle, the “Run Mode” watchdog counter is not cleared. | X | X | X |

**Notes:**

- Cells with ‘X’ indicate the issue is present in this revision of the silicon.
- Cells with ‘—’ indicate this silicon revision does not exist for this issue.
- The blank cell indicates the issue was corrected or does not exist in this revision of the silicon.

# 2. Silicon Errata Issues

The following errata issues apply to the PIC32CX-BZ2 family of devices.

**Notes:**

- Cells with an 'X' indicate the issue is present in this revision of the silicon.
- Cells with a dash ('—') indicate this silicon revision does not exist for this issue.
- Blank cells indicate the issue was corrected or does not exist in this revision of the silicon.
- Traditional Inter-Integrated Circuit ($I^2C$) and Serial Peripheral Interface (SPI) documentation use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client", respectively.

## 2.1 Supply Voltage and Power Mode

### 2.1.1 GPIO Output Configuration in Deep Sleep and Extreme Deep Sleep

In the Deep Sleep and Extreme Deep Sleep modes, GPIO must not be set to the output state of pin HIGH.

Configuring the GPIO state to pin High during the Deep Sleep and Extreme Deep Sleep modes will cause leakage current and potential reliability issues on the silicon.

This issue is only applicable when the CPU is in the Deep Sleep/Extreme Deep Sleep mode and when GPIO is configured as the output state pin HIGH.

**Work Around:**

Set the state of GPIOs to low before entering DS/XDS for the least current consumption, either by output state or by pull-down.

**Note:**

The work around is working in A2 and newer versions.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

### 2.1.2 POR Rearm Event

The POR event is not getting triggered even when the voltage is going below 1.45V.

**Work Around**

Discharge VDD to Zero.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.2 Analog-to-Digital Converter (ADC)

### 2.2.1 Level Trigger

The ADC level trigger does not perform burst conversions in Debug mode.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.2.2 Scan

The scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and does not generate an EOSRDY bit (ADCCON2[29]) end of scan interrupt status if a new trigger event from the STRGSRC[4:0] bits (ADCCON1[20:16]) trigger source occurs before the scan list completion on the shared ADC core.

**Work Around:**

Ensure that the STRGSRC[4:0] bits trigger source repetition rate.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.2.3 Incorrect VDD33/2 for ADC Internal Input Channel AN11

The ADC internal input channel, AN11, is connected with VDD33/2, but the observed input voltage is not equal to VDD/2.

**Work Around**

Get the expected input using the below formula:

VDD33/2 = VDD x (598.5/900)

For example, VDD = 3.3V

VDD33/2 = 3.3 x (598.5/900) = 2.1945V

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

## 2.3 Analog Comparator (AC)

### 2.3.1 Disabling Analog Comparator

AC_CMPx output is not gated either by COMPCTRLx.ENABLE or PMD1.ACMD.

**Work Around:**
Write the CFGCON1.CMPx_OE register bit to '0' to disable the AC_CMPx output.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.3.2 Incorrect VDD Scaler Reference for AC_CMP0

AC_CMP0 is supposed to use a fixed VDD/2 reference when the VDD scaler option is used. But the observed reference voltage is not equal to VDD/2.

**Work Around:**
For A0, use the following equation to get the VScale for AC_CMP0.

VScale = VDDx(598.5/900)

If VDD is 3.3, then:

VScale = 3.3x598.5/900 = 2.1945V

**Note:**
This workaround is only applicable to A0 revision and does not work in A2 revision.

For A2, AC_CMP0 uses VDD/2.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

### 2.3.3 Incorrect VDD Scaler Reference with CMP0 and CMP1 Enabled Concurrently

The wrong VDD scaler reference voltage is observed when AC_CMP0 and AC_CMP1 are enabled concurrently with VDD scaler as the reference for both the comparators. Both the comparators will see the same VDD scaler reference.

**Work Around:**
For A0, use the following equation to get the VScale for AC_CMP0 and AC_CMP1.

R_Bottom = R_Bottom of configured SCALER1.VALUE[3:0]

R_Total = 900 – abs([598.5 – R_Bottom])

VScale = VDD. (598.5)/R_Total if R_bottom >= 598.5

VScale = VDD.(R_Bottom/R_Total) if R_bottom < 598.5

**Note:**
This workaround is only applicable to A0 revision and does not work in A2 revision. In A2, CMP0 and CMP1 uses independent scaler references as per the data sheet.

CMP0 uses a fixed reference VDD/2. CMP1 uses a variable reference configured using SCALER1.VALUE[3:0].

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

## 2.4 Clock Reset Unit (CRU)

### 2.4.1 Peripheral Bus Clocks

The Power-on Reset value of the PB3 clock is not correct.

**Work Around:**
Use Microchip-provided SDK and bootloader. This software will initialize the CRU.PB3DIV register to the data sheet-specified default value. If using third-party tools and other custom developed software, set this register to the data sheet default value of 0x0000_8809.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.5 Configurable Custom Logic (CCL)

### 2.5.1 Enable Protected Registers

The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit; however, they must be enable-protected by the LUTCTRLx.ENABLE bits.

**Work Around:**
None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.5.2 Output Logic is Stuck when Enabling a LUT with Sequential Logic after the CCL is Enabled

When the LUT is disabled (LUTCTRL0.ENABLE=0 or LUTCTRL2.ENABLE=0) to clear the flip-flop/latch output, then enabled again, the sequential logic is kept under Reset.

**Work Around:**

Write CTRL.ENABLE again after LUT is enabled (LUTCTRL0.ENABLE=1 / LUTCTRL2.ENABLE=1) back.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.5.3 PAC Error when Writing CCL.CTRL.SWRST Bit

Writing the Software Reset bit in the Control A register (CTRLA.SWRST) will trigger a PAC protection error.

**Work Around:**

Clear the CCL PAC error each time a CCL software Reset is executed.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.5.4 Sequential Logic

LUT output is corrupted after enabling CCL when sequential logic is used.

**Work Around:**

Write the CTRL register twice when enabling the CCL.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.6 Device

### 2.6.1 VIL Input Low Voltage

There is degraded VIL/VIH performance when the GPIO pull-up/pull-down resistors are enabled on PB0, PB1, PB2, PB3,PB4, PB5, PB6, PB8 or PB9. These pins may not be able to recognize a logic low level if the pull-up on that pad is enabled.

**Work Around:**

If using PB0, PB1, PB2, PB3,PB4, PB5, PB6, PB8 or PB9 for GPIO, do not enable pull-up or pull-down; use external resistors.

**Note:**

The work around is working in A2 and newer versions.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

### 2.6.2 VDD min for A0 device is 2.1V

Some A0 devices may not operate below 2.1V.

**Work Around:**

Ensure the VDD is 2.1V.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

## 2.7 Device Service Unit (DSU)

### 2.7.1 Programming or Debugging

Device debugging or programming can only be supported using ICD4 at room temperature. When programming or debugging, the device's supply voltage can only range between 1.9 (min) and 3.0 (max) V, including the min and max voltages.

**Work Around:**

Use A2 silicon.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

### 2.7.2 CRC32

The DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled.

**Work Around:**

Be sure to always enable the NVM cache when performing a DSU CRC32 request targeting the NVM memory space.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.8 Direct Memory Access Controller (DMAC)

### 2.8.1 DMAC in Debug Mode

In Debug mode, DMAC does not restart after a debug halt when DBGCTRL.DBGRUN=0.

**Work Around:**

Set DBGCTRL.DBGRUN to '1' so that the DMAC continues normal operation when the CPU is halted by an external debugger.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.8.2 DMA Writeback Descriptor Corruption Issue

Aborting or disabling a DMA channel could lead to a corruption issue in the writeback descriptor of an active channel where there are ongoing transfers.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.8.3 Occurrence of Fetch Error

When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) may occur on enabling a channel with no linked descriptor or when one of the already active channels using linked descriptors may fetch the enabled second descriptor (index 1) of the channel. These errors can occur when a channel is enabled during the link request of another channel and if the channel number of the enabled channel is lower than the already active channel.

**Work Around:**

When enabling a channel while other channels using linked descriptors are already active, the channel number of the new channel to enable must be greater than the other channel numbers.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.9 External Interrupt Controller (EIC)

### 2.9.1 Edge Detection

When enabling EIC, the SYNCBUSY.ENABLE bit resets before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.9.2 Asynchronous Edge Detection

When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.

**Work Around:**

Use the asynchronous edge detection with debouncer enabled. It is recommended to set the DPRESCALER.PRESCALER and DPRESCALER.TICKON to have the lowest frequency possible. To reduce the power consumption, set the EIC GCLK frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL set).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.9.3 Asynchronous Edge Detection

When the asynchronous edge detection is enabled (without debouncer) and the system is in the Standby Sleep mode, only the first edge will generate an event. The edges following the first edge of the waveform do not generate events until the system wakes up.

**Work Around**

Asynchronous edge detection does not work; instead use the synchronous edge detection (ASYNCH.ASYNCH[x]=0). To reduce power consumption when using synchronous edge detection, either set the GCLK_EIC frequency as low as possible or select the 32KHz_LPCLK clock (EIC CTRLA.CKSEL=1).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.10 Event System (EVSYS)

### 2.10.1 Software Event

BUSYCH flag never resets upon software events in synchronous/resynchronized path modes with event detection on falling edges.

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH=0x0/0x1) with event detection set on falling edges (CHANNELn.EDGSEL=0x2), the CHSTATUS.BUSYCHn flag will be set but will never come back to '0'. It is, then, impossible to know if the event user for this channel is ready to accept new events or not.

**Work Around:**

Generate software events for this user through a dedicated channel configured with event detection set on rising edges (CHANNELn.EDGSEL=0x1).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.10.2 Spurious Overrun

The overrun interrupt flag may be incorrectly set upon software events in synchronous/ resynchronized path modes with event detection on both rising and falling edges.

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH=0x0/0x1) with event detection set on both rising and falling edges (CHANNELn.EDGSEL=0x3), spurious overrun interrupts may occur (INTFLAG.OVRn).

**Work Around:**

Generate software events for the event user through a dedicated channel configured with event detection set on rising edges (CHANNELn.EDGSEL=0x1).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.10.3 Spurious Overrun

In the Synchronous mode, spurious overrun interrupts can happen when the generic clock for a channel is always CHANNEL.ONDEMAND=0.

**Work Around**

Set Generic Clock on Demand feature by setting CHANNEL.ONDEMAND=1.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.11 Flash Controller Module

### 2.11.1 SYS Reset Not Getting Released when Asserted Post-Erase Retry

After the Erase Retry operation (using NVMCON2.VREAD1=1), all the operations work as expected until a SYS Reset is asserted. When the SYS Reset is asserted post-Erase Retry, the Reset is stuck and not getting released.

**Work Around**

To eliminate the risk of getting stuck in Reset, execute one of the below mentioned options after the VREAD operation:

1. Power-on Reset
2. Configure the CFGCON1.SMCLR bit to 0 to make MLCR create Faux-POR. Assert MCLR.
3. Enter and Exit Deep Sleep mode

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.11.2 DMA in Sleep Mode

Flash read/write by DMA not working in Standby Sleep mode if Flash power down is enabled.

**Work Around**

If DMA is used in Standby Sleep mode, do not enable the Flash power down (NVMCON2.SLEEP=0).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

## 2.12 Frequency Meter (FREQM)

### 2.12.1 Measurement Clock Stalls

During a measurement slot, the measurement clock stalls (or is very slow), the STATUS.BUSY will never de-assert and the DONE interrupt will not be raised.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.13 $I^2C$

### 2.13.1 SCL/SDA Transition Time

SCL/SDA minimum transition time is not met in Fast-mode plus (1 MHz).

**Work Around:**

- If desired, external series resistors can slow the fall transition.
- Recommend REXT*CLOAD>13 ns. REXT must not exceed 1 Kohms.

| Product/Interface | Voltage Range |
|---|---|
| $I^2C$ | 2.97<VDDIO<3.63 |
| | 1.9<VDDIO<2.97 |

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.14 Peripheral Access Controller (PAC)

### 2.14.1 PAC Protection Error in FREQM

FREQM reads on the Control B register (FREQM.CTRLB), then generates a PAC protection error.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.14.2 PAC Protection Error in CCL

Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.

**Work Around:**

Clear the CCL PAC error each time a CCL software Reset is executed.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.15 Prefetch Cache

### 2.15.1 CPU Hang Configuration Switch

CHECON.ADRWS is not hardwired to '0' and is configurable to '1' or '0', with the reset/default value being '1'. The CPU hangs when the CHECON.ADRWS configuration switches from '1' to '0' and a Flash read access occurs. While CHECON.ADRWS is switching to '0' (default is '1'), the ADRWS will be latched at the next clock, and, if a Flash read access happens at the same clock, the system hangs waiting for an internal ack due to the PFM cache miss.

**Work Around:**

To configure ADRWS from '1' to '0', execute the CHECON configuration from SRAM until the configuration is done, then resume the execution from Flash after the configuration is set. The Microchip-generated initialization code already takes care of this with the above scheme.

**Notes:**

- The work around is working in A2 and newer versions.
- The ADRWS bit behavior is modified in the *PIC32CX-BZ2 and WBZ45 Family Data Sheet* (DS70005504).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

## 2.16 Quad I/O Serial Peripheral Interface (QSPI)

### 2.16.1 QSPI Status Register Bits Not Updated when PB-Bridge-B (PB2_CLK) is Not Equal to System Clock (SYS_CLK)

If PB2_CLK is not equal to System Clock (sys_clk), the QSPI Status register bits are not updated.

**Work Around**

When using the QSPI Status register bits in the application, configure PB2_CLK to be equal to SYS_CLK without any divisions.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.17 RAM Error Correction Code (ECC)

### 2.17.1 ERRADDR Register may Read as '0' when PB-Bridge-B (PB2_CLK) is Not Equal to System Clock (SYS_CLK)

If PB2_CLK is not equal to System Clock (sys_clk), ERRADDR register read will not return the failing address (caused by Single Bit Error/Dual Bit Error); instead it may return '0'.

**Work Around:**

When using RAM ECC in the application, configure PB2_CLK to be equal to SYS_CLK without any divisions.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.18 Real-Time Counter (RTC)

### 2.18.1 False Tamper Detection

False tamper detections may occur when configuring the RTC INn and OUTn pins.

**Work Around:**

First, configure the different RTC registers. Then, select the RTC INn and OUTn peripheral function(s) on the PORT peripheral (PMUX registers).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.2 Incorrect Periodic Daily Event at 23:59:58

Periodic Delay Event needs to be asserted at the end of the prescaler period to be generated on the last second of the day. As the prescaler overflow does not qualify the Periodic Delay Event, the event is generated at the beginning of the prescaler period, hence, one second earlier than specified.

**Work Around:**

The user application may wait 1 sec to process the periodic daily event.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.3 Reset of General Purpose Registers on Tamper Detection

General Purpose Registers n (GPn) are reset on tamper detection even if GPTRST=0.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.4 Reset of INTFLAG.TAMPER Bit Fails

When DMA is enabled (CTRLB.DMAEN=1), the INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register.

**Work Around:**

Clear the INTFLAG.TAMPER bit by writing a '1' to this bit when the Timestamp value is read by the DMA.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.5 RTC SYNCBUSY Register Bits Not Cleared

Entering the Deep Sleep mode without waiting for SYNCBUSY.ENABLE and SYNCBUSY.COUNTSYNC synchronization completion may freeze these bits' statuses.

**Work Around:**

The RTC must always be configured and enabled before enabling the Battery Backup mode.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.6 Timestamp is Updated Even Tamper Flag is Not Cleared

When the tamper happens, the DMA is triggered and the DMA captures TIMESTAMP and TAMPID. INTFLAG.TAMPER flag is not cleared after reading TIMESTAMP.

**Work Around:**

Clear the INTFLAG.TAMPER bit by writing a '1' to this bit when the timestamp value was read by the DMA.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.7 Timestamp Register is Cleared After Debug Read

The read of the RTC timestamp register in debug mode will clear the DMA request flag and unlock the TIMESTAMP register, although a debug read does not alter the TIMESTAMP value. Further read of TIMESTAMP register by DMA or CPU will return 0x00 because the TIMESTAMP is an RTC core register and can be read only when locked after a capture.

**Work Around:**

Do not read the RTC timestamp during debugging.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.8 Write Corruption

An 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:

- COUNT register in COUNT32 mode
- COUNT register in COUNT16 mode
- CLOCK register in CLOCK mode

**Work Around:**

Write the registers with:

- A 32-bit write access for COUNT register in COUNT32 mode, CLOCK register in CLOCK mode
- A 16-bit write access for the COUNT register in COUNT16 mode

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.9 COUNTSYNC

When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and, thus, it is an incorrect value.

**Work Around:**

After enabling COUNTSYNC, read the COUNT register until its value is changed when compared to its first value read. After this, all subsequent values read from the COUNT register are valid.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.10 Tamper Input Filter

Majority debouncing, as part of RTC tamper detection, does not work when enabled by setting the Debouncer Majority Enable bit, CTRLB.DEBMA J.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.11 Tamper Detection

Upon enabling the RTC tamper detection feature, a false tamper detection can be reported by the RTC.

**Work Around:**

Use any one of the following work arounds:

1. Configure tamper detection to only falling edge.
2. If the user software has to use tamper detection as rising edge, it must ignore the first tamper interrupt generated after enabling the RTC tamper detection.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.12 Tamper Detection Timestamp

If an external Reset occurs during a tamper detection, the timestamp register will not be updated when the next tamper detection is triggered.

**Work Around:**

Enable RTC tamper interrupt and copy the timestamp from the RTC CLOCK COUNT register to one of the following destinations:

- SRAM
- GPx register in RTC
- BKUPx register in RTC

**Note:** This work around does not apply for Battery Backup mode. In Battery Backup mode, the RTC Timestamp capture feature is not functional.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.18.13 Unwanted Event and Interrupt Generation

When CTRLA.PRESCALER is set to OFF and either CTRLB.RTCOUT is set or one of the TAMCTRL.DEBNCn bits is set, the RTC prescaler behaves like CTRLA.PRESCALER=DIV1. The periodic events and periodic interrupts will be generated.

**Work Around:**

When the above conditions are met, clear the EVTCTRL.PEROEn bits to avoid unwanted event generation and clear the INTENCLR.PERn bits to avoid unwanted interrupt generation.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.19 Serial Communication Interface (SERCOM)

### 2.19.1 Two Stop Bits Mode is Not Supported in SERCOM USART LIN Host Mode

Two stop bits mode (CTRLB.SBMODE=0x1) is not supported in SERCOM USART LIN Host Mode (CTRLA.FORM=0x2) in the case where break, sync and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD=0x2). Only one stop bit mode is supported.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.2 SERCOM LIN Adding Additional Delay Between Break and Sync Bits

In SERCOM USART LIN Host Mode (CTRLA.FORM=0x2), in the case where break, sync and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD=0x2), the LIN Host Header delay between the sync and the ID transmission fields is not correct for the following cases:

- CTRLC.HDRDLY=0x2, where the delay between sync and ID transmission fields is 8-bit time instead of 4-bit time.
- CTRLC.HDRDLY=0x3, where the delay between sync and ID transmission fields is 14-bit time instead of 4-bit time.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.3 SERCOM-USART: INTFLAG.TXC being Set Incorrectly

When the USART is used in the 32-bit mode with hardware handshaking (CTS/RTS), the TXC flag may be set before transmission completes. TXC may incorrectly be set regardless of whether Data Length Enable (LENGTH.LENEN) is set to '0' or '1'.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.4 SERCOM-USART: Overconsumption in Standby Mode

When the SERCOM USART configured as CTRLA.RUNSTDBY=0 and the Receiver is disabled (CTRLB.RXEN=0), the clock request to the SERCOM generic clock generator feeding the SERCOM will stay asserted during the Standby Sleep mode, leading to unexpected overconsumption.

**Work Around:**

Configure CTRLA.RXPO and CTRLA.TXPO to use the same SERCOM PAD for RX and TX or add an external pull-up on the RX pin.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.5 SERCOM-USART: Flow Control in 32-bit Extension Mode

When the USART is used in the 32-bit mode with hardware handshaking (CTS/RTS), the TXC flag may be set before transmission has completed. TXC may incorrectly be set regardless of whether Data Length Enable (LENGTH.LENEN) is set to '0' or '1'.

**Work Around**

Use the 8-bit mode if using Hardware Flow control.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.6 SERCOM-USART: Auto-Baud Mode

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.7 SERCOM-USART: Collision Detection

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN=1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.

**Work Around:**

The SERCOM APB clock must always be higher than the SERCOM Generic Clock to support collision detection.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.8 SERCOM-USART: SERCOM USART in TX Mode Only

When the SERCOM USART is configured as CTRLA.RUNSTDBY=0 and the Receiver is disabled (CTRLB.RXEN=0), the clock request to the SERCOM generic clock generator feeding the SERCOM will stay asserted during the Standby Sleep mode, leading to unexpected overconsumption.

**Work Around**

Configure CTRLA.RXPO and CTRLA.TXPO to use the same SERCOM PAD for RX and TX or add an external pull-up on the RX pin.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.9 SERCOM-USART: Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.10 SERCOM-USART: Error Interrupts

The SERCOM USART does not wake from the Standby Sleep mode for ERROR interrupts FERR and PERR.

**Work Around:**

Configure the SERCOM-USART to wake up on RX complete and check any PERR/FERR interrupt flag on wake-up.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.11 SERCOM-USART: 32-bit Extension Mode

When the 32-bit Extension mode is enabled and data to be sent are not in multiples of 4 bytes, which means the length counter must be enabled, additional bytes will be sent over the line.

**Work Around:**

Use any one of the following work arounds:

1. Write the Inter-Character Spacing bits (CTRLC.ICSPACE) to a non-zero-value.
2. Do not use the length counter in firmware by keeping the data to be sent in multiples of 4 bytes.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.12 SERCOM-UART: TXINV and RXINV Bits

The TXINV and RXINV bits in CTRLA are interchanged. TXINV controls the RX signal inversion and RXINV controls the TX signal inversion.

**Work Around:**

In software, interpret the TXINV bit as a functionality of RXINV, and, conversely, interpret the RXINV bit as a functionality of TXINV.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.13 STATUS.CLKHOLD Bit in Host and Client Modes

The STATUS.CLKHOLD bit in host and client modes can be written even though it is specified as a read-only status bit.

**Work Around:**

Do not clear the STATUS.CLKHOLD bit to preserve the current clock hold state.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.14 SERCOM-I$^2$C: Automatic Acknowledge Feature Not Usable

The I$^2$C client AACKEN feature is not usable when doing a repeated start.

**Work Around:**

Do not use the AACKEN feature; implement an AMATCH handler instead.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.15 SERCOM-I$^2$C: Error Interrupt after Unexpected STOP

When an unexpected STOP occurs on the I$^2$C bus, the STATUS.BUSERR and INTFLAG.ERROR bits are set but may not wake the system from the Standby Sleep mode. An unexpected START will not produce this issue.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.16 SERCOM-I²C: Repeated Start Not Issued Correctly

For the Host Write operations (excluding the High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD=0x1 does not issue a Repeated Start command correctly.

**Work Around:**

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate a Repeated Start.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.17 SERCOM-I²C: I²C in Client Mode

In I²C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.

**Work Around:**

Manually clear status bits LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR by writing these bits to '1' when set.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.18 SERCOM-I²C: Client Mode with DMA

If there are still data to be sent in the DMA buffer at the reception of a NACK in the I²C Client Transmitter mode, the DMA will push data to the DATA register. The NACK being received prevents the transfer on the I²C bus from occurring, causing the loss of this data.

**Work Around:**

Configure the DMA transfer size to the number of data to be received by the I²C host. DMA cannot be used if the number of data to be received by the host is not known.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.19 SERCOM-I²C: I²C Client in DATA32B Mode

When SERCOM is configured as an I²C client in 32-bit Data mode (DATA32B=1) and the I²C host reads from the I²C client (client transmitter) and outputs its NACK (indicating no more data are needed), the I²C client still receives a DRDY interrupt.

If the CPU does not write new data to the I²C client DATA register, the I²C client will pull the SDA line, which results in stalling the bus permanently.

**Work Around:**

1. Write dummy data to the data register when a NACK is received from the host.
2. Use command #2 (SERCOMx->I2CS.CTRLB.bit.CMD=2) when a NACK is received from the host.

**Important:** STATUS.RXNACK always indicates the last received ACK; therefore, to determine when a NACK is received from the I²C host, the I²C client software needs to consider I2CS.STATUS.RXNACK only on the second DRDY interrupt after receiving the AMATCH interrupt.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.20 SERCOM-I²C: 10-Bit Addressing Mode

The 10-bit addressing in I²C Client mode is not functional.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.21 SERCOM-I²C: Repeated Start

When the quick command is enabled (CTRLB.QCEN=1), software can issue a repeated start by writing either CTRLB.CMD or ADDR.ADDR bit fields. If, in these conditions, SCL Stretch mode is CTRLA.SCLSM=1, a bus error will be generated.

**Work Around:**

Use Quick Command mode (CTRLB.QCEN=1) only if SCL Stretch mode is CTRLA.SCLSM=0.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.22 SERCOM-SPI: Data Preload

In SPI Client mode and with Client Data Preload Enabled (CTRLB.PLOADEN=1), the first data sent from the client will be a dummy byte if the host cannot keep the client select (SS) line low until the end of transmission.

**Work Around:**

In SPI Client mode, the client select (SS) pin must be kept low by the host until the end of the transmission if the client data preload feature is used (CTRLB.PLOADEN=1).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.23 SERCOM-SPI: Client Data Preload

Preloading new SPI data (CTRLB.PLOADEN=1) before going into Standby Sleep mode may lead to extra power consumption.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.19.24 SERCOM-SPI: Hardware Client Select Control

When the hardware client select control is enabled (CTRLB.MSSEN=1), the client select (SS) pin goes high after each byte transfer even if new data is ready to be sent.

**Work Around:**

Set CTRLB.MSSEN=0, and handle the client select (SS) pin by software.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.20 System Bus

### 2.20.1 Bus Error Address Checks

When accessing peripherals on the PB-PIC® bus, an access beyond the implemented memory region 0x4401_FFFF causes the CPU to hang, waiting for a bus error signal.

**Work Around:**
Use the Microchip-provided peripheral drivers from Harmony 3 and the Microchip-provided SDK. This software will not generate addresses outside the implemented regions. If using third-party tools and other custom developed software, do not create accesses outside this region or an MCU Reset will be required to recover.

**Note:**
The work around is working in A2 and newer versions.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

## 2.21 System Configuration Registers

### 2.21.1 CFGCON0 Registers

CFGCON0.SWOEN is non-functional, which makes PB7 function as SWO during debugging only. PB7 works normally when not doing debug.

**Work Around:**
Do not use PB7 as GPIO while debugging.

**Note:**
The work around is working in A2 and newer versions.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

### 2.21.2 System Bus QoS

The Power-on Reset values of the CFGPGQOS register sets all bus host QoS values to zero (Background) instead of the required Power-on Reset values.

**Work Around:**

Use the Microchip-provided SDK and bootloader. This software will initialize the CFGPGQOS register to the data sheet-specified default value. If using third-party tools and other custom developed software, set this register to the data sheet default value of 0xE040_004C.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.22 Timer/Counter for Control Applications (TCC)

### 2.22.1 Counting-down Mode Not Supported in RAMP2

The Timer/Counter counting-down mode (CTRLBCLR.DIR=CTRLBSET.DIR=1) is not supported in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS).

**Work Around:**

Use Timer/Counter counting up mode (CTRLBCLR.DIR=CTRLBSET.DIR=0).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.22.2 ALOCK Feature

The ALOCK feature is not functional.

**Work Around**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.22.3 Hi-resolution in 2RAMP Mode

In 2RAMP mode with Hi-resolution, multiple restarts can be observed when a fault occurs.

**Work Around:**

In two Ramp modes (RAMP2, RAMP2A, RAMP2C, RAMP2CS), a re-trigger is not supported in Dithering mode.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.22.4 LUPD in Descendent Mode

When the TCC is used in the Down-counting mode, transfer of the PERBUF register value to the PER register is delayed by one counter cycle, and, therefore, the LUPD feature must not be used with the PER register.

**Work Around:**

In the Down-counting mode, write period value directly to the PER register instead of writing to PERBUF. Alternatively, the Up-counting mode in the TCC can be used if the LUPD feature is required.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.22.5 Re-trigger in RAMP2 Operations

Re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C) is not supported if a prescaler is used (CTRLA.PRESCALER != 0) and the re-trig of the counter is done on the next GCLK (CTRLA.PRESCSYNC = GCLK or CTRLA.PRESCSYNC = RESYNC).

**Work Around:**

Configure the re-trigger of the counter on the next prescaler clock (CTRLA.PRESCSYNC = PRESC).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.22.6 Re-trigger

If a Re-trigger event (EVCTRL.EVACTn=0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

**Work Around:**
Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.22.7 TCC in Dithering Mode

Using the TCC in the Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses or shrink of left-aligned pulses.

**Work Around:**
Do not use re-trigger events or actions when the TCC module is configured in the Dithering mode.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.22.8 TCC in SYNC or RESYNC Mode

The TCC peripheral is not compatible with an EVSYS channel in the SYNC or RESYNC mode.

**Work Around:**
Use the TCC with an EVSYS channel in the ASYNC mode.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.22.9 TCC Outputs

The TCC0/TCC1 output is not working as expected with PPS; output signals are not visible on output pins via PPS even though the TCC is working correctly. TCC2 cannot be used to drive external pins.

**Work Around:**
Use the CCL module to output up to 2 TCCx_WO[n] signals on CCL0_OUT and CCL1_OUT using PPS to the desired pins.

The required configuration in CCL1/2:

- CCL.CTRL.ENABLE=1 – To enable CCL
- CCL.LUTCTRLx.ENABLE=1 – To enable LUT in CCL
- CCL.LUTCTRLx.INSELx=8 – To select TCC as input source
- CCL.LUTCTRLx.TRUTH – To match the toggle of TCC
  - CCL.LUTCTRLx.TRUTH=0xAA – To match toggle on WO[0]
  - CCL.LUTCTRLx.TRUTH=0xCC – To match toggle on WO[1]
  - CCL.LUTCTRLx.TRUTH=0xF0 – To match toggle on WO[2]
- CFGCON1.CCL_OE=1 – To enable CCL output onto PADs

Then, configure PPS for CCL output to desired pin.

**Note:**
CCL0_OUT allows one instance of TCC0_WO[n], and CCL1_OUT allows one instance of TCC1_WO[n].

The work around is working in A2 and newer version.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

### 2.22.10 MCx Interrupt Status Flag is Not Cleared Automatically

In the capture operation, MC0/MC1 interrupt status flags (INTFLAG.MC0/INTFLAG.MC1) are not automatically cleared when the CC0/CC1 registers are read.

**Work Around**
The MC0/MC1 interrupt status flags must be cleared by software (INTFLAG.MC0=1/INTFLAG.MC1=1).

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.22.11 DMA Request is Not Set on Overflow Condition in One-shot DMA Trigger Mode of RAMP2C Operation

TCC Overflow (OVF) will not trigger a DMA request in the One-shot DMA Trigger (DMAOS) mode of RAMP2C operation.

DMA triggers are not applicable for the RAMP2C mode.

**Work Around:**
None

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.23 Timer/Counter (TC)

### 2.23.1 Issues After Clearing STATUS.PERBUFV/STATUS.CCBUFx flag

When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.

**Work Around:**
Clear successively twice the STATUS.PERBUFV/STATUS.CCBUFVx flag to ensure that the PERBUF/CCBUFx register value is properly restored before updating it.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.23.2 Re-trigger

If a Re-trigger event (EVCTRL.EVACTn=`0x1`, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

**Work Around**
Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

**Affected Silicon Revisions**
PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.23.3 MCx Interrupt Status Flag is Not Cleared Automatically

In a capture operation, MC0/MC1 interrupt status flags (INTFLAG.MC0/INTFLAG.MC1) are not automatically cleared when CC0/CC1 registers are read.

**Work Around**

The MC0/MC1 interrupt status flags must be cleared by software (INTFLAG.MC0=1/INTFLAG.MC1=1).

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.23.4 TC.PER not updated properly

In the 8-bit mode, the PER register updates using the DMA are not possible in the Standby mode.

**Work Around:**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

### 2.23.5 TC Outputs

The TC0/1/2/3 output is not working as expected with PPS; output signals are not visible on output pins via PPS even though the TC is working correctly.

**Work Around:**

Set COPENx and CAPTENx before enabling/re-enabling the Timer Counter.
Set TC.CTRLA.COPENx=1 and TC.CTRLA.CAPTENx=1 before enabling/re-enabling the timer counter.

- Configure PPS for output to the desired pin.
- Initialize the timer counter.
- TC.CTRLA.COPENx=1
- TC.CTRLA.CAPTENx=1
- Start/enable the timer counter.

**Note:**

This work around is only applicable to the A0 revision and does not work in the A2 revision.

For A2, TC0/1/2/3 are working as expected with PPS.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| | | | | | |

### 2.23.6 ALOCK Feature

The ALOCK feature is not functional.

**Work Around**

None

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

## 2.24 Watchdog Timer (WDT)

### 2.24.1 Watchdog Counter

When the interval between clearing the watchdog timer (in other words, clearing the Run mode watchdog counter) and the sleep instruction is less than 1 WDT clock cycle, the “Run Mode” watchdog counter is not cleared. When using LPRC for the clock source, the interval is 1 LPRC clock. The watchdog timer is in the LPRC domain, which is much slower than the CPU clock; therefore, the sleep instruction is executed even before the “Run mode” watchdog counter is cleared. Hence, the “Run mode” watchdog counter remains frozen to its last count instead of clearing to 0.

While in Sleep mode, the “Sleep mode” watchdog counter is incrementing, and, at the end of the WDTPS, it generates an NMI, which causes the CPU to wake up.

After waking up, the user would expect, because they cleared the WDT just before going to sleep, that they have an entire WDT period available to them before they have to clear WDT again. But, because the “Run mode” counter was not cleared before going into sleep, the WDT Reset occurs earlier than expected.

**Work Around (either or both can be used):**

1. Add a delay of more than 1 WDT Clock (LPRC clock) between clearing the WDT and execution of the sleep instruction.
2. Execute the WDT clear instruction as soon as the CPU wakes up.

**Affected Silicon Revisions**

PIC32CX1012BZ25048/WBZ451/WBZ451H/WBZ451PE-E

| A0 | A2 | | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

PIC32CX1012BZ24032/WBZ450

| A2 | | | | | |
|---|---|---|---|---|---|
| X | | | | | |

# 3. Data Sheet Clarifications

The following clarifications and additional information are applicable to the latest version of the *PIC32CX-BZ2 and WBZ45 Family Data Sheet* (DS70005504):

- The VZPBOR33 information is updated from 1.8V to 2.1V in *43.4 Power Supply Electrical Specifications*.
- Added Wake-up Timing Specification for Low Power Modes in *43.15 Wake-Up Timing from Low Power Modes AC Electrical Specifications*.
- The ADC Single-Ended Mode information was updated in *Table 43-25: ADC Single-Ended Mode AC Electrical Specifications* in *43.22 ADC Electrical Specifications*.

# 4. Document Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

| Revision | Date | Section | Description |
|---|---|---|---|
| E | 2/2025 | Overview, Silicon Errata Summary, Silicon Errata Issues | Added errata information that are applicable for the WBZ451PE-E device |
| | | Data Sheet Clarifications | • Added information on Wake-up Timing Specification for Low Power Modes<br>• Updated information on ADC Single-Ended Mode |
| D | 11/2024 | Overview, Silicon Errata Summary, Silicon Errata Issues | Added WBZ451H related errata and information |
| | | I2C | Added new errata |
| | | VDD min for A0 device is 2.1V | Added new errata |
| | | Data Sheet Clarifications | Added new section |

**.....continued**

| Revision | Date | Section | Description |
|---|---|---|---|
| C | 07/2024 | Silicon Errata Issues | Added new errata:<br>• POR Rearm Event<br>• Incorrect VDD33/2 for ADC Internal Input Channel AN11<br>• Output Logic is Stuck when Enabling a LUT with Sequential Logic after the CCL is Enabled<br>• PAC Error when Writing CCL.CTRL.SWRST Bit<br>• DMA Writeback Descriptor Corruption Issue<br>• Asynchronous Edge Detection<br>• Spurious Overrun<br>• SYS Reset Not Getting Released when Asserted Post-Erase Retry<br>• DMA in Sleep Mode<br>• QSPI Status Register Bits Not Updated when PB-Bridge-B (PB2_CLK) is Not Equal to System Clock (SYS_CLK)<br>• Incorrect Periodic Daily Event at 23:59:58<br>• Timestamp is Updated Even Tamper Flag is Not Cleared<br>• Timestamp Register is Cleared After Debug Read<br>• Two Stop Bits Mode is Not Supported in SERCOM USART LIN Host Mode<br>• SERCOM LIN Adding Additional Delay Between Break and Sync Bits<br>• SERCOM-USART: Flow Control in 32-bit Extension Mode<br>• SERCOM-USART: SERCOM USART in TX Mode Only<br>• ALOCK Feature<br>• MCx Interrupt Status Flag is Not Cleared Automatically<br>• Re-trigger<br>• MCx Interrupt Status Flag is Not Cleared Automatically |
| | | | Updated the work around for the following errata:<br>• SERCOM-USART: Error Interrupts<br>• SERCOM-I2C: Automatic Acknowledge Feature Not Usable<br>• SERCOM-I2C: 10-Bit Addressing Mode<br>• SERCOM-I2C: Repeated Start<br>• Hi-resolution in 2RAMP Mode<br>• LUPD in Descendent Mode<br>• TCC in Dithering Mode<br>• TCC in SYNC or RESYNC Mode |

**.....continued**

| Revision | Date | Section | Description |
|---|---|---|---|
| B | 01/2024 | Overview | Added PIC32CX1012BZ24032/WBZ450-related information |
| | | Silicon Errata Summary | • Added PIC32CX1012BZ24032/WBZ450-related information<br>• Added new errata |
| | | Silicon Errata Issues | • Added PIC32CX1012BZ24032/WBZ450-related information<br>• Incorrect VDD Scaler Reference for AC_CMP0<br>– Updated description and workaround<br>– Added note<br>• Incorrect VDD Scaler Reference with CMP0 and CMP1 Enabled Concurrently<br>– Updated workaround<br>– Added note<br>• VIL Input Low Voltage<br>– Added note<br>• Programming or Debugging<br>– Updated workaround<br>• CPU Hang Configuration Switch<br>– Updated description and workaround<br>– Added note<br>• Bus Error Address Checks<br>– Added note<br>• CFGCON0 Registers<br>– Added note<br>• TCC Outputs<br>– Added note<br>• TC Outputs<br>– Updated description<br>– Added note |

**.....continued**

| Revision | Date | Section | Description |
|---|---|---|---|
| B | 01/2024 | Silicon Errata Issues | Added new errata:<br>• Occurrence of Fetch Error<br>• Measurement Clock Stalls<br>• False Tamper Detection<br>• Reset of General Purpose Registers on Tamper Detection<br>• Reset of INTFLAG.TAMPER Bit Fails<br>• RTC SYNCBUSY Register Bits Not Cleared<br>• Unwanted Event and Interrupt Generation<br>• SERCOM-USART: INTFLAG.TXC being Set Incorrectly<br>• SERCOM-USART: Overconsumption in Standby Mode<br>• SERCOM-USART: Error Interrupts<br>• SERCOM-I2C: Automatic Acknowledge Feature Not Usable<br>• SERCOM-I2C: Error Interrupt after Unexpected STOP<br>• SERCOM-I2C: Repeated Start Not Issued Correctly<br>• SERCOM-I2C: 10-Bit Addressing Mode<br>• Counting-down Mode Not Supported in RAMP2<br>• Hi-resolution in 2RAMP Mode<br>• LUPD in Descendent Mode<br>• TCC in Dithering Mode<br>• TCC in SYNC or RESYNC Mode<br>• Issues After Clearing STATUS.PERBUFV/STATUS.CCBUFx flag<br>• TC.PER not updated properly |
| A | 10/2022 | Document | Initial revision |

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