Evaluating the AD3552R, 16-Bit, Dual-Channel, Current Output DAC

FEATURES

- Full featured evaluation board for the AD3552R
- High speed and high precision transimpedance amplifiers
- Selectable transimpedance gain with rotary switch
- On-board or external power supply
- On-board or external voltage reference
- Usable with controller boards SDP-H1 and Digilent ZedBoard
- DAC channel aggregation

EVALUATION KIT CONTENTS

- EVAL-AD3552RFMCZ

HARDWARE REQUIRED

The evaluation board can be used with one of the following controllers, that must be purchased separately:

- SDP-H1 board
- Digilent ZedBoard

SOFTWARE REQUIRED

If using the SDP-H1 controller board:

- ACE software
- Board.AD35X2R ACE plugin (automatically downloaded within ACE)

If using the Digilent ZedBoard as controller (see EVAL-AD3552R Wiki):

- Kuiper Linux Image
- IIO Scope tool
- UART terminal tool

ONLINE RESOURCES

- Bill of materials and layout files

EVALUATION BOARD PHOTOGRAPH

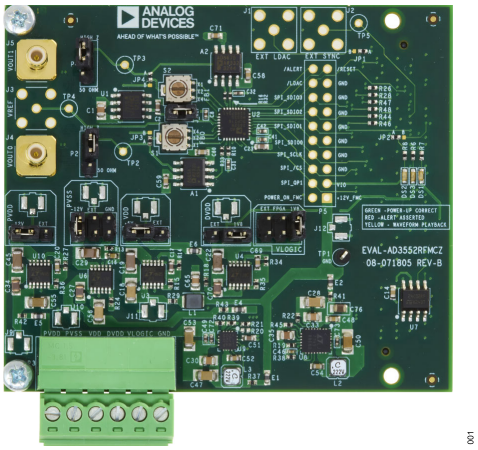

Figure 1. EVAL-AD3552RFMCZ Top View

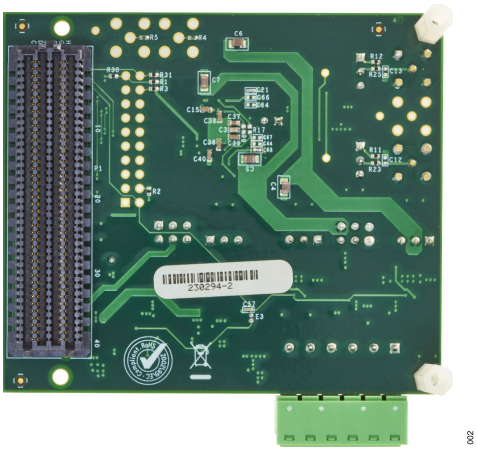

Figure 2. EVAL-AD3552RFMCZ Bottom View

GENERAL DESCRIPTION

The EVAL-AD3552RFMCZ is an evaluation board for the AD3552R, a dual-channel, 16-bit fast precision digital-to-analog converter (DAC). Each channel of the AD3552R is equipped with a different transimpedance amplifier: Channel 0 has a fast amplifier that achieves the optimal dynamic performance and Channel 1 has a precision amplifier that guarantees the optimal DC precision over temperature.

The board allows testing all the output ranges of the DAC, waveform generation, power supply, and reference options.

The EVAL-AD3552RFMCZ interfaces to the USB port of a PC via a system demonstration platform (SDP-H1 board). It can also be connected to the ZedBoard or a different controller board using the pin header connector at position P5. Refer to the EVAL-AD3552RFMCZ Wiki page for details on using the EVAL-AD3552RFMCZ with the ZedBoard.

This user guide covers the details of the configuration and operation of the EVAL-AD3552RFMCZ board and the associated ACE plugin. Refer to the AD3552R data sheet for additional information on the DAC operation.

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REVISION HISTORY

10/2024—Rev. A to Rev. B

Changes to Figure 20 17

5/2024—Revision A: Initial Version

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EVALUATION BOARD QUICK START PROCEDURE

INSTALLING THE SOFTWARE

To evaluate the EVAL-AD3552RFMCZ with the ACE software and the AD3552R plugin, take the following steps:

1. Download and run the latest version of the ACE installer. It installs the application and the necessary drivers for the SDP-H1 controller board.
2. Click the **Plugin Manager** item on the left-hand menu as shown in Figure 3.
3. Go to **Available Packages**, select **Board.AD35X2R**, and click the **Install Selected** button at the bottom of the list. Once the plugin is installed, it moves to the **Installed Packages** section.
4. Click the **Home** item on the left-hand menu. If the EVAL-AD3552RFMCZ board is connected, it will show up in the **Attached Hardware** section as shown in Figure 4. If you do not have an EVAL-AD3552RFMCZ board, you can still explore the functionality of the plugin by double clicking the desired board in the **Explore Without Hardware** list.

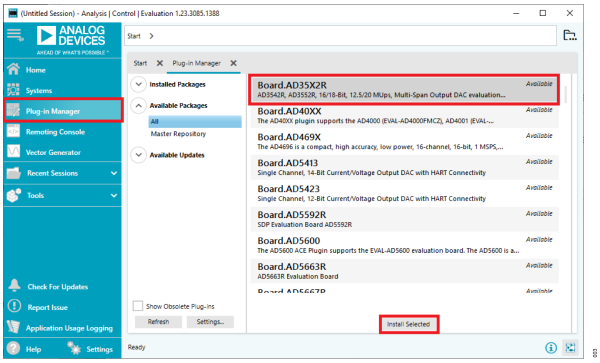

Figure 3. Plugin Manager

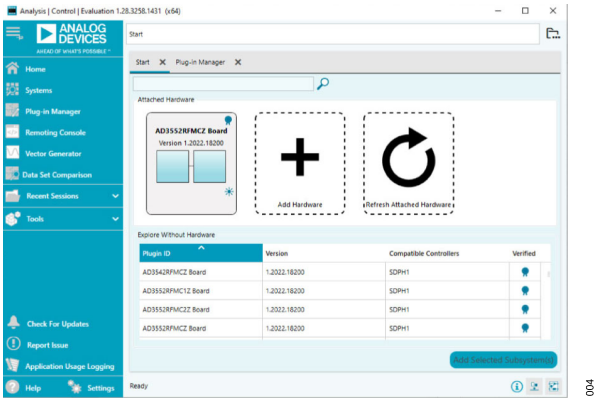

Figure 4. Start Tab

CONNECTING THE BOARD

To set up the EVAL-AD3552RFMCZ evaluation board with the SDP-H1 controller, take the following steps:

1. Make sure that all the links are set in the default positions listed in Table 2.
2. Plug the EVAL-AD3552RFMCZ evaluation board on the SDP-H1 controller board.
3. Connect the USB cable between the SDP-H1 board and the PC.
4. Connect the wall-plug brick power supply to the SDP-H1 DC jack and power from the AC network. Power LEDs on the SDP-H1 turn on green. A message bubble may appear from the icon tray indicating that the SDP-H1 board has been detected.
5. Start up the ACE application. The EVAL-AD3552RFMCZ board is detected and displayed in the **Attached Hardware** section, as shown in Figure 4. Double click the board icon to open the board view, as seen in Figure 9. The board view shows the relevant parts included in the evaluation board, where the AD3552R chip is highlighted in a darker blue.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-AD3552RFMCZ includes a complete power conversion solution to allow powering the evaluation board from the SDP-H1 or from a single 12 V supply. The board includes two DC/DC converters LT8336 and LTC7149 to generate ±16 V from the 12 V power provided by SDP-H1. LDOs LT3045 and LT3094 are used to generate ±12 V for the transimpedance amplifiers. Another two LT3045 LDOs are used to generate the 5 V and 1.8 V supplies for the AD3552R. This power solution is configured with the default link settings shown in Table 2.

Alternatively, the board can be powered from a collection of external power supplies via connector P3. The assignment of the pins in connector P3 is listed in Table 1.

Table 1. Pin Assignment on Power Supply Connector P3

Pin Number	Signal	Description
1	EXT_PVDD	External positive supply for transconductance amplifier. 12 V ± 5%.
2	EXT_PVSS	External negative supply for transconductance amplifier. −12 V ± 5%.
3	EXT_VDD	External AV_{DD} analog supply for AD3552R. 5 V ± 5%.
4	EXT_DVDD	External DV_{DD} digital supply for AD3552R. 1.8 V ± 5%.
5	EXT_VLOGIC	External V_{LOGIC} digital I/O supply for AD3552R. 1.1 V to 1.9 V.
6	GND	Ground.

The EVAL-AD3552RFMCZ also integrates an on-board 2.5 V analog reference ADR4525.

LINK OPTIONS

The EVAL-AD3552RFMCZ board is delivered with the links and switches placed in the default positions listed in Table 2. This configuration is suitable for operating the board out of the box. However, the S1 and S2 switches and the J_REF link may need to be adjusted depending on the configuration set in the registers of the AD3552R.

Table 2. Link Options

Link/Switch	Silkscreen	Description	Default Position
S1	S1	This link selects the gain of transimpedance amplifier for Channel 0. The gains are labeled ×1, ×2, and ×4 which correspond to the multiplicative factor between them. The gain must be set in accordance to the desired output range listed in Table 6. Rotate the switch so that the notch points at the desired gain.	×1
S2	S2	This link selects the gain of transimpedance amplifier for Channel 1. The gains are labeled ×1, ×2, and ×4 which correspond to the multiplicative factor between them. The gain must be set in accordance to the desired output range listed in Table 6. Rotate the switch so that the notch points at the desired gain.	×1
J_REF	J_REF	This link allows connecting the on-board reference to AD3552R. This link must be removed if an external reference is provided via connector J3 or if the internal reference is output to the V_{REF} pin.	Inserted
J_PVDD	PVDD	This link selects the positive voltage supply for the transimpedance amplifier. 12 V selects the supply from the on-board LDO. EXT selects the supply provided externally on connector P3.	12 V
J_PVSS	PVSS	This link selects the negative voltage supply for the transimpedance amplifier. −12 V selects the supply from the on-board LDO. EXT selects the supply provided externally on connector P3. GND sets the supply rail to ground.	−12 V
J_VDD	VDD	This link selects the voltage supply for the analog section of AD3552R. +5 V selects the supply from the on-board LDO regulator. EXT selects the supply provided externally on connector P3.	5 V
J_DVDD	DVDD	This link selects the voltage supply for the digital section of AD3552R. 1V8 selects the supply from the on-board LDO regulator. EXT selects the supply provided externally on connector P3.	1V8
J_VIO	VLOGIC	This link selects the voltage supply for AD3552R I/O pins. 1V8 selects the supply for the on-board LDO regulator. FPGA selects the supply provided from the SDP-H1 board, the same as used in the FPGA I/O pins. EXT selects the supply provided externally on connector P3.	1V8
P2	P2	This link configures the on-board matching pad to adapt to the impedance of the instrument connected on VOUT0. Set the link to HIGH Z if VOUT0 is connected to an instrument with high input impedance using a coaxial cable. Set the link to 50 OHM if VOUT0 is connected to an instrument with 50 Ω input impedance.	HIGH Z

EVALUATION BOARD HARDWARE

Table 2. Link Options (Continued)

Link/Switch	Silkscreen	Description	Default Position
P4	P4	This link configures the on-board matching pad to adapt to the impedance of the instrument connected on VOUT1. Set the link to HIGH Z if VOUT1 is connected to an instrument with high input impedance using a coaxial cable. Set the link to 50 OHM if VOUT1 is connected to an instrument with 50 Ω input impedance.	HIGH Z
JP1	JP1	This link configures the source of the $\overline{\text{LDAC}}$ signal. If the link is set to A, the signal is taken from the controller via connectors P1 or P5. If the link is set to B, the signal is taken from an instrument connected on J1.	A
JP2	JP2	This link configures the source driving the red ALERT LED. If the link is set to A, the LED is driven by the AD3552R via the $\overline{\text{ALERT}}$ pin. If the link is set to B, the LED is driven by the controller via connector P1. The controller must sense the $\overline{\text{ALERT}}$ signal and turn on the LED when needed.	A

ON-BOARD CONNECTORS

Table 3 shows the list of connectors available on EVAL-AD3552RFMCZ and their corresponding use.

Table 3. List of Connectors

Connector	Signal Name	Function
J1	EXT_LDAC	Input for an external LDAC signal. This connector is terminated to 50 Ω. The voltage of the signal must not exceed V_{LOGIC} voltage by more than 0.3 V.
J2	EXT_SYNC	Input for an external synchronization signal provided to the FPGA. This connector is terminated to 50 Ω. The voltage of the signal must not exceed the FPGA I/O voltage by more than 0.3 V.
J3	VREF	Reference voltage input/output. This connector can be used to provide an external reference voltage to the AD3552R or to monitor the reference generated by ADR4525 or AD3552R. If an external voltage is provided on this connector, the link J_REF must be removed and the V_{REF} pin of the AD3552R must be configured as input.
J4	C_VOUT0	Voltage output of transimpedance amplifier A1, corresponding to DAC Channel 0.
J5	C_VOUT1	Voltage output of transimpedance amplifier A2, corresponding to DAC Channel 1.
P1	Multiple[1]	FMC connector carrying the digital signals and voltage supplies between the evaluation board and the controller board.
P3	Multiple[2]	External supply connector. Pin assignment given in Table 1.
P5	Multiple[3]	Custom controller interface. This connector is used to control the AD3552R with a controller different from SDP-H1 or ZedBoard. The pin assignment is listed in Table 4. The pin header is not assembled by default so that the holes can be used as test points for the digital signals.

[1] See the Evaluation Board Schematics section.

[2] See Table 1.

[3] See Table 4.

Connector P5 is used to connect an external controlled when the SDP-H1 is not present. This connector grants access to all the digital signals of AD3552R and some board supplies and control lines.

Table 4. Pin Assignment on Connector P5

Pin number	Connector Label	Function
1	+12V_FMC	External 12 V power supply. Use this pin to supply the EVAL-AD3552RFMCZ board when using a custom controller different from the SDP-H1 or the ZedBoard.
2	POWER_ON_FMC	Enable signal for the onboard regulators. This pin is used to turn on the LDOs and DC/DC converters. Set a voltage higher than 1.24 V to turn on. If the controller is not driving this signal, it must be set manually to use the board.
3	VIO	Voltage supply used for AD3552R I/O pins. If this pin is used to supply V_{LOGIC}, remove the VLOGIC link or set it to EXT.
4	SPI_QPI[1]	Signal SPI_QPI. A high level sets the bus in Quad SPI mode. A low level sets the bus in classic SPI mode.
5	GND	Ground.
6	SPI_CS[1]	SPI Chip Select signal.
7	GND	Ground.
8	SPI_SCLK[1]	SPI clock signal.
9	GND	Ground.
10	SPI_SDIO0[1]	SDI/MOSI signal in Classic SPI mode or SDIO0 signal in Dual/Quad SPI modes.
11	GND	Ground.

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Table 4. Pin Assignment on Connector P5 (Continued)

Pin number	Connector Label	Function
12	SPI_SDIO1[1]	SDO/MISO signal in Classic SPI mode or SDIO1 signal in Dual/Quad SPI modes.
13	GND	Ground.
14	SPI_SDIO2[1]	SPI SDIO2 signal in Quad SPI mode.
15	GND	Ground.
16	SPI_SDIO3[1]	SPI SDIO3 signal in Quad SPI mode.
17	GND	Ground.
18	/LDAC[1]	$\overline{\text{LDAC}}$ signal.
19	/RESET[1]	$\overline{\text{RESET}}$ signal.
20	/ALERT[1]	$\overline{\text{ALERT}}$ signal.

[1] The voltage on this pin must not exceed V_{LOGIC} voltage by more than 0.3 V.

The board includes several test points to access relevant signals. Only TP1 has the test ring assembled. The list is given in Table 5.

Table 5. List of Test Points

Test Point	Signal	Description
TP1	GND	Ground
TP2	VOUT0	Voltage output of transimpedance amplifier A1, corresponding to DAC Channel 0
TP3	VOUT1	Voltage output of transimpedance amplifier A2, corresponding to DAC Channel 1
TP4	V_{REF}	Reference voltage for AD3552R (internal, on-board or external)
TP5	EXT_SYNC	External synchronization signal.

LED INDICATORS

The EVAL-AD3552RFMCZ has three LED indicators as follows:

- DS1. This yellow LED turns on when the controller starts a waveform playback in streaming mode. This LED is controlled from a GPIO on connector P1, Pin H13. Therefore, this functionality depends on the SW and the controller used with the evaluation board.
- DS2. This red LED turns on when the $\overline{\text{ALERT}}$ pin is asserted in the AD3552R. This LED can also be controlled from a GPIO if the link JP2 is changed to position B.
- DS3. This green LED turns on when the chip gets 1.8 V DV_{DD} power. This indicator lights up dimly because 1.8 V is barely the band gap voltage of a green LED.

DAC OUTPUT RANGE SELECTION

The selection of the output range requires a combination of register configurations and a given transimpedance gain. The gains corresponding to each output range are listed in Table 6. See the AD3552R data sheet for more details on output range configuration. The gain is configured with Switch S1 and Switch S2 for DAC Channel 0 and DAC Channel 1, respectively.

Table 6. Transimpedance Gain Setting

CHx_OUTPUT_RANGE_SEL Field Value	Output Range (V)	Transimpedance Gain Setting
000	2.5	×1
001	5	×1
010	10	×2
011	±5	×2
100	±10	×4

OUTPUT IMPEDANCE MATCHING

The AD3552R is a fast precision DAC that settles much faster than traditional precision DACs. At this speed, transmission line effects on the cable cannot be neglected. The board implements an impedance matching network with two configurations selectable using links P2 and P4 for Channel 0 and Channel 1, respectively. The diagram of this network is shown in Figure 5.

- HIGH Z option provides impedance matching on the source side. This configuration sets a 52.3 Ω resistor in series with the output of the amplifier. This resistor provides some return loss to attenuate reflected waveforms originated on the high-impedance end of the coaxial cable. It also provides isolation from the capacitance of the cable to prevent the oscillation of the high-speed amplifier. This series resistor introduces a DC error of 50 ppm if the load is an oscilloscope, and 5 ppm if the load is a multimeter.
- 50 OHM option provides impedance matching when the load at the other end of the cable is 50 Ω. This configuration offers optimal signal transmission over a wide frequency band, but it

EVALUATION BOARD HARDWARE

is not for free. The matching network introduces an attenuation factor of 39.18, or 31.86 dB.

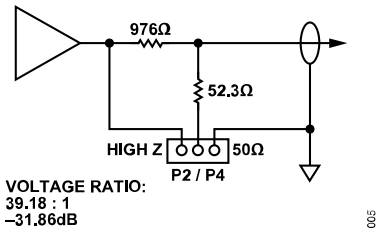

Figure 5. Impedance Matching Network

Some recommendations are given for the following different types of measurements:

- DC measurements. It is recommended to connect the multimeter using a coaxial cable to minimize noise and interference. The matching network must be set to HIGH Z mode to obtain the highest SNR. For long-term measurements, it is recommended to cover the evaluation board with a cardboard box to prevent air flow. Do not cover the SDP-H1 controller because its power dissipation is high.
- Step response measurements. It is recommended to connect the oscilloscope using a coaxial cable with 50 Ω impedance. The matching network must be set to 50 OHM and the oscilloscope input configured to 50 Ω. Use $\overline{\text{LDAC}}$ or $\overline{\text{CS}}$ to trigger the oscilloscope and set the acquisition mode to averaging to reduce noise and be able to measure settling time accurately. Passive probes are not recommended for settling time because their compensation circuits alter the step response.
- Noise measurements. Noise is so low that it is only visible in the HIGH Z configuration. An instrument with 50 Ω input impedance may be connected as long as it is AC-coupled. Note that the noise spectral density depends on the load impedance. Therefore, using a 50 Ω instrument results in a lower voltage than using a high impedance instrument.
- Glitch amplitude. The glitch is so small that it is only visible in the HIGH Z configuration. It is recommended to use an oscilloscope or a digitizer with 12- to 16-bit resolution, AC coupling, and the maximum vertical resolution. Use $\overline{\text{LDAC}}$ or $\overline{\text{CS}}$ to trigger the oscilloscope and set the acquisition mode to averaging to distinguish the glitch from the noise.
- THD and SFDR. THD at low frequency can be measured using a digitizer or an audio analyzer. In this case, the matching network must be set to HIGH Z because these instruments are high impedance. For higher frequencies, a spectrum analyzer is needed. In this case, the matching network must be set to 50 OHM. Most spectrum analyzers do not have enough linearity to measure the harmonics of AD3552R reliably. Therefore, it is recommended to use high-pass filters to attenuate the fundamental tone. Alternatively, the 20-bit fast precision ADC AD4080 can be used to measure THD at high frequency and high impedance.

DAC CHANNEL COMBINATION

The EVAL-AD3552RFMCZ allows combining two DAC channels with a single amplifier. Combining channels has the following advantages:

- Increased resolution. Full-scale current doubles while the error is averaged, which increases the resolution by up to one bit. An additional bit can be gained using different codes on each DAC.
- Lower noise. While the output current doubles, uncorrelated noise increases by $\sqrt{2}$ only. This results in an SNR increase by the same amount or a reduction of noise in relation to a single DAC using the same R_{FBx} resistor.
- Faster settling time. If the two DAC channels change simultaneously with the same code, the current step is double while the parasitic capacitance of the amplifier is the same as for a single channel. In addition, if the feedback resistors are connected in parallel, the lower resistance results in higher closed-loop bandwidth for the external amplifier.

Table 7 summarizes the list of changes required to combine two DAC outputs on one of the amplifiers. Once the changes are made, the current of the two DACs is combined into a single amplifier; the other amplifier remains powered and in open loop.

Table 7. Configurations for Channel Combination

	Output on VOUT0	Output on VOUT1
R9	0 Ω	0 Ω
R10	1 kΩ	1 kΩ
R16	DNI	0 Ω
R17	0 Ω	0 Ω
R32	1 kΩ	1 kΩ
R33	0 Ω	DNI
JP3	0 Ω on A	0 Ω on B
JP4	0 Ω on B	0 Ω on A

The configuration to combine both channels on amplifier A1 is shown in Figure 6.

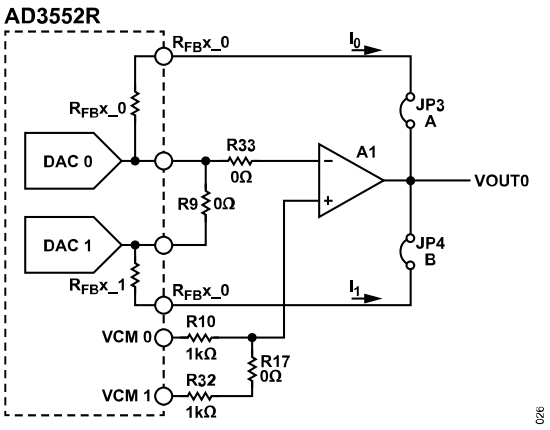

Figure 6. Combination of Two Channels on VOUT0

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The voltage expected at the output is given by the following expression:

$$VOUT0 = \frac{V_{CM0} + V_{CM1}}{2} - \left(I_0 + I_1\right) \times \frac{R_{FBx0} \times R_{FBx1}}{R_{FBx0} + R_{FBx1}} \quad (1)$$

Assuming that $V_{CM}0 = V_{CM}1 = VCM$ and $R_{FBx}0 = R_{FBx}1 = R_{FBx}$, the expression is simplified as:

$$VOUT0 = V_{CM} - \left(I_0 + I_1\right) \times \frac{R_{FBx}}{2} \quad (2)$$

ACE PLUGIN DESCRIPTION AND FEATURES

ACE PLUGIN HIERARCHY

ACE has several views to control different aspects of the DAC. When a view is first opened, it creates a new tab at the top of the main window. The AD3552R plugin has a **Board View**, a **Chip View**, a **Memory Map View**, a **Waveform Generator View**, and a **Vector Generator View**. Figure 7 shows the hierarchical relation between these views. Refer to the ACE User Manual for more details. The user manual is accessible from the help panel displayed when click the **Help** button on the lower left angle of the application.

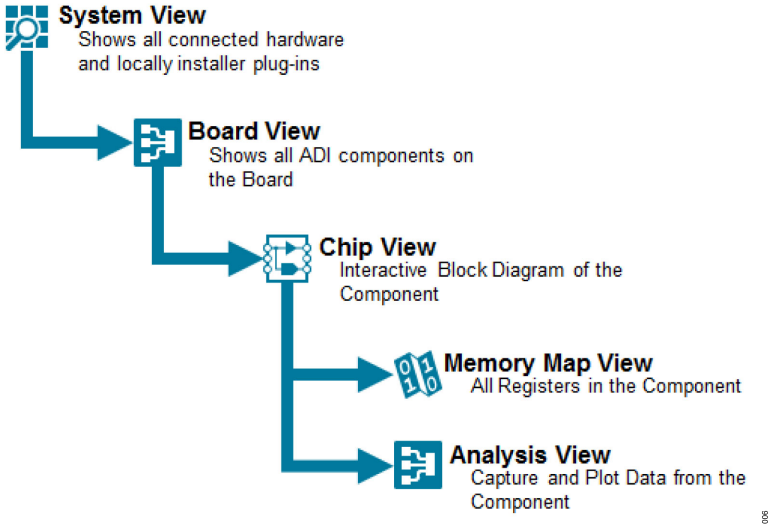

Figure 7. ACE Plugin Hierarchy

ACE PLUGIN DESCRIPTION AND FEATURES

BOARD VIEW

The **Board View** displays a simplified diagram of the evaluation board including some relevant connectors and the interconnection between chips, as seen in Figure 8. Analog Devices, Inc., chips are shown with their part number and the AD3552R is highlighted in darker blue.

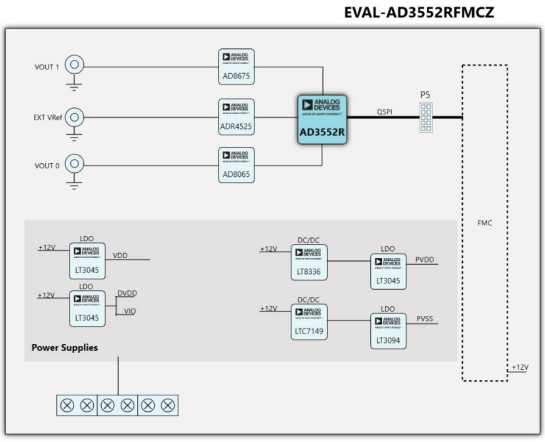

Figure 8. AD3552R Board View

The actions that can be performed at this level are displayed as buttons at the top of the main window, as seen in Figure 9.

- **Poll Device**. This action is performed automatically every second to verify that the evaluation board is connected to the system. The button allows turning on or off this feature. This feature must be turned off when using the application without the evaluation board to avoid error bubbles showing up continuously.
- **Reset Board**. This action performs a power cycle on the evaluation board, bringing everything back to default.

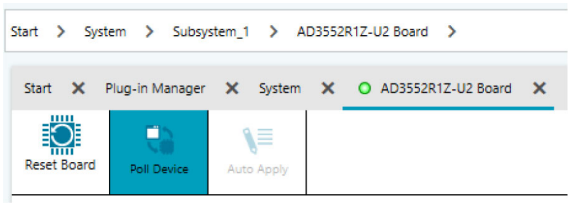

Figure 9. AD3552R Board View Buttons

To open the **Chip View**, double click the AD3552R block.

CHIP VIEW

The **Chip View** displays a simplified internal diagram of the chip showing the interface logic, the DAC cores, the precision feedback resistors, and the relevant pins for those blocks. This view contains three interactive areas, as depicted in Figure 10:

1. **Button list.** These buttons perform the following actions on the chip:
   - **Apply Changes:** changes in the values of the registers are recorded in a cached copy kept on the PC memory. When the button **Apply Changes** is pressed, only the registers that were changed are updated in the AD3552R.
   - **Read All:** this button reads all the registers from the AD3552R and updates the cached copy in the PC memory, displaying the values in the corresponding fields.
   - **Reset Chip:** this button resets the AD3552R but not the board. All registers are cleared to default values and ACE reads them back to keep the cached copy synchronized.
   - **Diff:** this button reads the registers of AD3552R and compares their value to the cached copy, highlighting in bold those that are different.
   - **Software Defaults:** this button loads the software default values in the cached copy without copying the values to the AD3552R.
   - **Memory Map Side-By-Side:** this button opens a new window besides the **Chip View** containing the list of AD3552R registers.
2. **DAC Registers.** Each DAC symbol contains an editable field where the hexadecimal code can be written to the DAC Output register. This allows performing an static update of the DAC. After writing the value, the **Apply Changes** button must be pressed to update the DAC output.
3. **Shortcuts to other views.** There are two buttons on the lower right corner to access the **Register Map View** and the **Waveform Generator View**. The use of these panels is explained in the Memory Map View section and Generating a Waveform section.

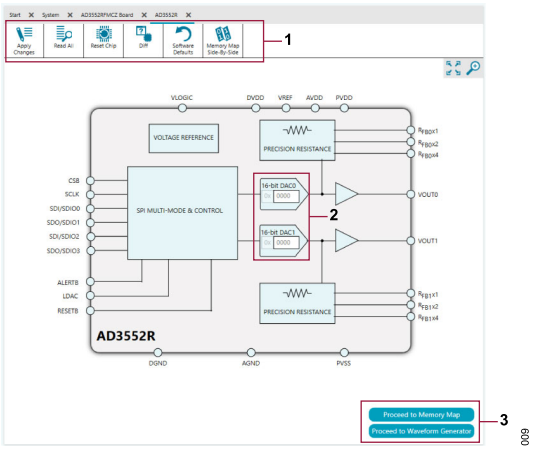

Figure 10. Chip View

MEMORY MAP VIEW

The **Memory Map View** displays the entire configuration space of the AD3552R. The configuration space can be displayed as a list of registers or as a list of bit fields. The application allows sorting by any of the column categories or searching by register name or field name. Registers can be displayed collapsed or expanded into its bit fields, as shown in Figure 11.

This view has the following interactive elements:

ACE PLUGIN DESCRIPTION AND FEATURES

1. **Button list.** These buttons perform the following actions:
   - **Apply Changes:** this button writes all the registers that have been changed since the last update.
   - **Apply Selected:** this button writes only the register or bit field that is selected in the list.
   - **Read All:** this button forces the reading of all the AD3552R registers and the update of the cached copy.
   - **Read Selected:** this button reads only the register or bit field that is selected and updates its value in the cached copy.
   - **Reset Chip:** this button resets the AD3552R and forces the reading of all registers to update the cached copy.
   - **Diff:** this button reads the registers of AD3552R and compares them with the cached copy, highlighting in bold those that have any difference.
   - **Software Defaults:** this button loads the software default values in the cached copy without copying the values to the AD3552R.
   - **Export:** this button exports the list of registers and their values to a CSV file. This feature is useful to generate the configuration file for a given application avoiding human error.
   - **Import:** this button allows reading a CSV file containing the register values.
   - **Chip View Side-by-Syde:** this button displays the chip view by the side of the register map.
   - **Show Bitfields / Show Registers:** this button toggles presentation mode as register list or bit field list.
2. **Register value.** This field allows editing the entire register value in hexadecimal (left side) or toggling the bits one by one (right side). Modified registers are highlighted in bold.
3. **Bit field values.** Registers can be expanded into their bit fields and each bit can be edited individually by clicking on it to toggle its value. Modified registers are highlighted in bold.

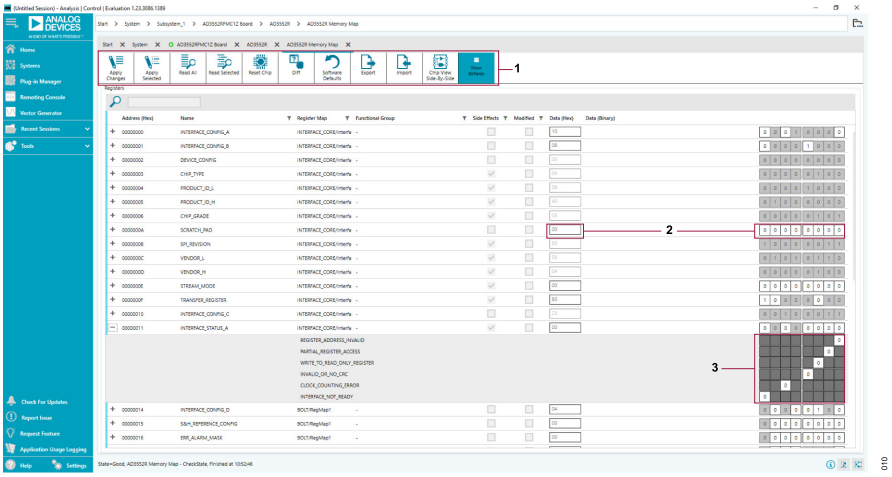

Figure 11. AD3552R Memory Map View

ACE PLUGIN DESCRIPTION AND FEATURES

WAVEFORM GENERATOR VIEW

The **Waveform Generator View** allows assigning vectors to the channels and starting or stopping waveform generation. A screenshot of this view is shown in Figure 12.

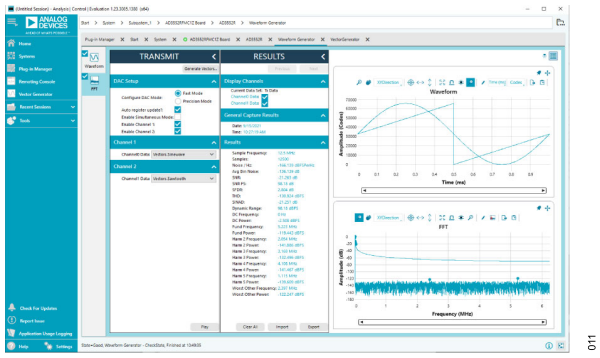

Figure 12. Waveform Generator View

The operation mode of AD3552R and the assignment of the waveforms are controlled from the **Transmit** pane that contains the following controls:

- **Generate Vectors**. This button opens the **Vector Generator** view where waveforms can be defined, scaled, loaded, or exported. The use of this generator is covered in the Vector Generator View section.
- **DAC Mode**. Radio buttons allow selecting **Fast Mode** that uses 16-bit data or **Precision Mode** that uses 24-bit data. The same mode is used for both DAC channels when operated simultaneously.
- **Auto Register Update**. This feature automatically configures the interface registers to operate in streaming mode with the highest possible update rate. If this box is not checked, configuration must be made manually on the memory map. The settings are described at the end of this section.
- **Enable Simultaneous Mode**. This checkbox allows playing the same samples on both channels. Data is written to the DAC Page register, therefore maintaining the same update rate as for a single channel. When this box is checked, the waveform is selected in the **Simultaneous Update** menu as seen in Figure 14.
- **Enable Channel 1/2**. These checkboxes allow enabling channels individually. When both channels are enabled, each one can play a different waveform, as seen in Figure 13. The update rate depends on the **DAC Mode** and the update mode; all the combinations are shown in Table 8.
- **Play Button**. This button starts and stops the waveform playback. The status of the playback is displayed on the EVAL-AD3552RFMCZ by turning the yellow LED DS1 on.

Table 8. Update Rate Combinations in MUPS

	Fast Mode (16-Bit Data)	Precision Mode (24-Bit Data)
Dual Channel Mode	12.5	8.33
Single Channel/Simultaneous Mode	25	16.66

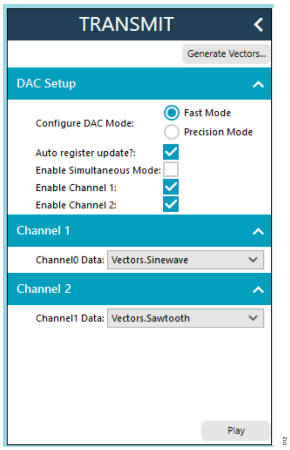

Figure 13. Waveform Generation in Dual Mode

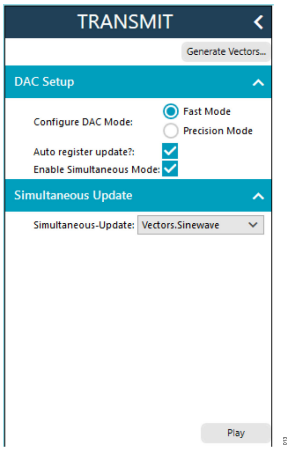

Figure 14. Waveform Generation in Simultaneous Mode

Manual Register Configuration for Streaming Mode

If the **Auto register update** checkbox is not checked, the streaming mode parameters have to be configured manually in the memory map before pressing the **Play** button. The following registers must be set:

- STREAM_MODE register (0x0E). Length value must be set according to Table 9.
- TRANSFER_REGISTER (0x0F). Set STREAM_LENGTH_KEEP_VALUE bit to 1.
- INTERFACE_CONFIG_D register (0x14). Set SPI_CONFIG_DDR bit to 1.

ACE PLUGIN DESCRIPTION AND FEATURES

Table 9. Stream Mode Length Values

	Fast Mode (16-Bit Data)	Precision Mode (24-Bit Data)
Dual Channel Mode	2	3
Single Channel/ Simultaneous Mode	4	6

VECTOR GENERATOR VIEW

The **Vector Generator View** allows defining or loading waveforms that can later be assigned to the DAC channels. Waveforms are identified by name. The generator automatically adapts the sample rate based on the operating mode and the number of DAC channels enabled. A snapshot of this view is presented in Figure 16.

The Vector Generator tool is composed of the following sections:

1. **Predefined Waveforms.** The generator has several predefined waveforms: DC, single tone, square, triangle, sawtooth, chirp, noise, and multitone. Clicking the **Add Vector** button shown in Figure 15 adds this waveform to the **GENERATE** panel where it can be customized.

Figure 15. Add Vector Button

2. **Waveforms from File.** The generator can load waveforms from file in three different formats: text file, hexadecimal file, or ACE Vector file. Refer to the ACE user manual for further details on the file formats. When loading a waveform, all the samples are played irrespective of the update rate. Therefore, the waveform files must be generated for a specific update rate.
3. **First Waveform Parameters.** Every waveform has a set of parameters that can be customized:
   - **Vector Name:** specify a name in this field to identify the waveforms in the **Waveform Generator View**.
   - **Desired Frequency:** specify the repetition frequency of the waveform. The value is assumed to be in Hz if no unit is specified. If the unit is specified, it must adhere to the standard capitalization (for example kHz, not khz).
   - **Attenuation:** all waveforms are generated at full scale by default. Attenuation can be used to reduce the signal amplitude keeping the offset constant at midscale. Amplitude is scaled by $10^{-Att/20}$.
   - **Relative Phase:** specify the phase offset relative to the start of the waveform record.
   - **Preview button:** pressing this button displays the waveform in the time-domain and its FFT in the frequency-domain window, if present.
   - **Copy:** pressing this button duplicates the waveform entry in the **Generate** pane.
   - **Export:** pressing this button allows exporting the waveform as a text file containing decimal numbers.
4. **Second Waveform Parameters.** If a second waveform is added, it shows up stacked in the **Generate** pane under the first waveform. The same parameters are applicable.
5. **Time-domain waveform preview.** A preview of the selected waveform is displayed in this window. Only one waveform is displayed at a time. The plot window allows zooming, panning, and measuring on the waveform.
6. **Waveform FFT.** The frequency-domain analysis of the selected waveform is displayed in this window. The plot window allows zooming, panning, and measuring on the spectrum.

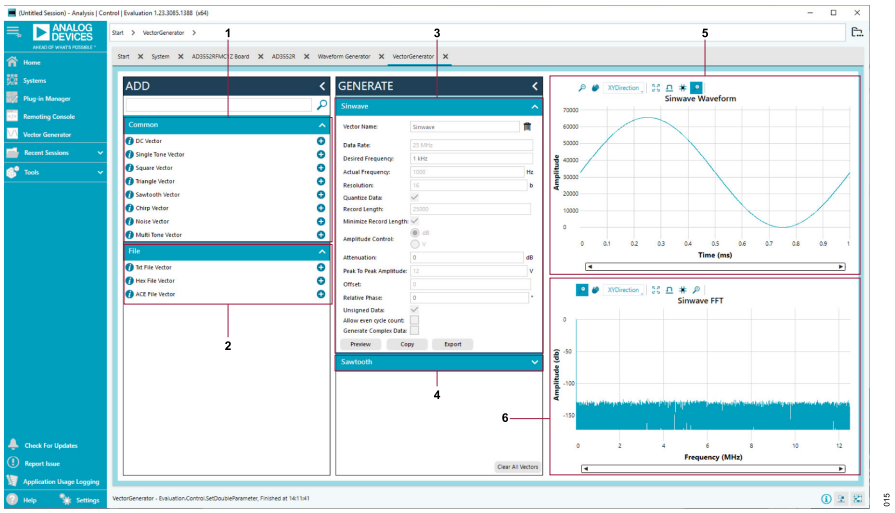

Figure 16. Vector Generator View

ACE PLUGIN DESCRIPTION AND FEATURES

GENERATING A WAVEFORM

Follow these steps to produce a dual waveform playback on the EVAL-AD3552RFMCZ evaluation board:

1. From the start page, double click the board icon to open the Board View.
2. Double click the AD3552R block to open the Chip View.
3. Click the **Proceed to Memory Map** button to open the Memory Map View.
4. Go to CH0_CH1_OUTPUT_RANGE register and set the desired output range (0x33 in this example). Refer to Table 6 for the possible values of this register. Then click **Apply All** to force the register update.
5. Click the **Vector Generator** item on the left-hand panel to open the Vector Generator View.
6. Follow the instructions given in Vector Generator View to create a 1 kHz sinewave and a 1 kHz sawtooth.
7. Follow the shortcuts in the gray bar at the top of the window to go back to the Chip View. Then click the **Proceed to Waveform Generator** button to open the Waveform Generator View.
8. Select **Fast Mode**, **Enable Channel 1**, and **Enable Channel 2**. Then unfold the Channel 1 and Channel 2 sections to select each of the waveforms you created. Finally, click the **Play** button.
9. The DS1 LED on the EVAL-AD3552RFMCZ turns yellow and the playback starts. The waveforms must look as the ones shown in Figure 17 in the oscilloscope.

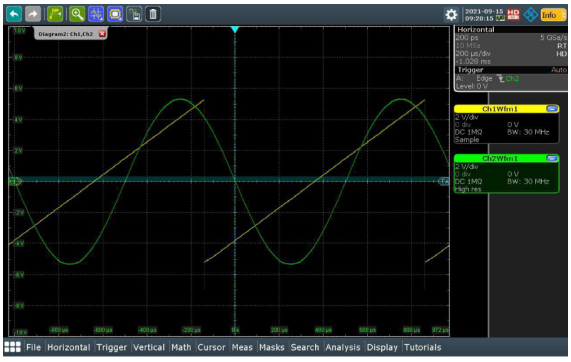

Figure 17. Simultaneous Waveform Output

UNSUPPORTED FEATURES IN THE PLUGIN

The ACE plugin does not support all the features of the AD3552R and the EVAL-AD3552RFMCZ. The following are the nonsupported features:

- DAC output range selection and customization. There is no visual control to change this. The configuration must be entered manually in the **Memory Map View**.
- CRC checking.
- Amplitude and offset control in waveform generation. Waveform scaling is only possible using the attenuation field in dB. Offset is fixed to midscale.
- Using the $\overline{\text{LDAC}}$ line to update the DAC output. The FPGA writes the DAC register directly. In streaming mode, DAC Channel 1 is delayed from DAC Channel 0 by two clock cycles.
- $\overline{\text{ALERT}}$ pin monitoring, error status readback, and on-screen reporting. The alert condition is displayed visually using an LED, but the application does not report it.
- External triggering of waveform playback.

EVALUATION BOARD SCHEMATICS

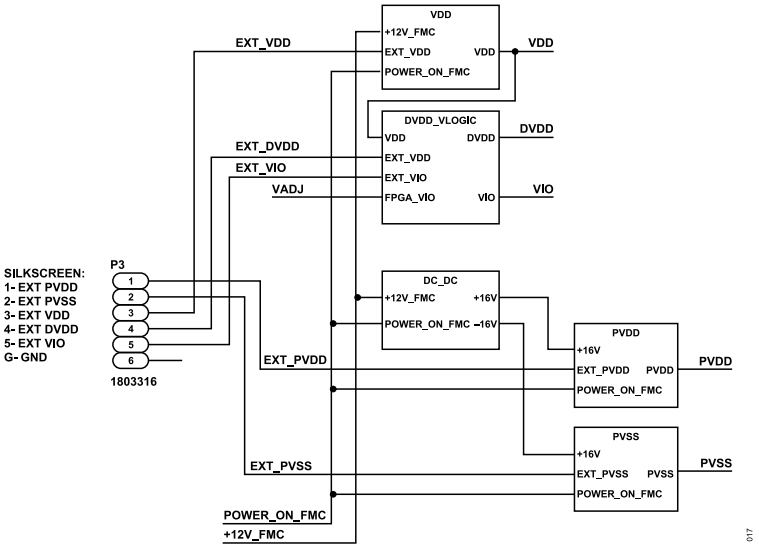

Figure 18. Power Supply Tree

EVALUATION BOARD SCHEMATICS

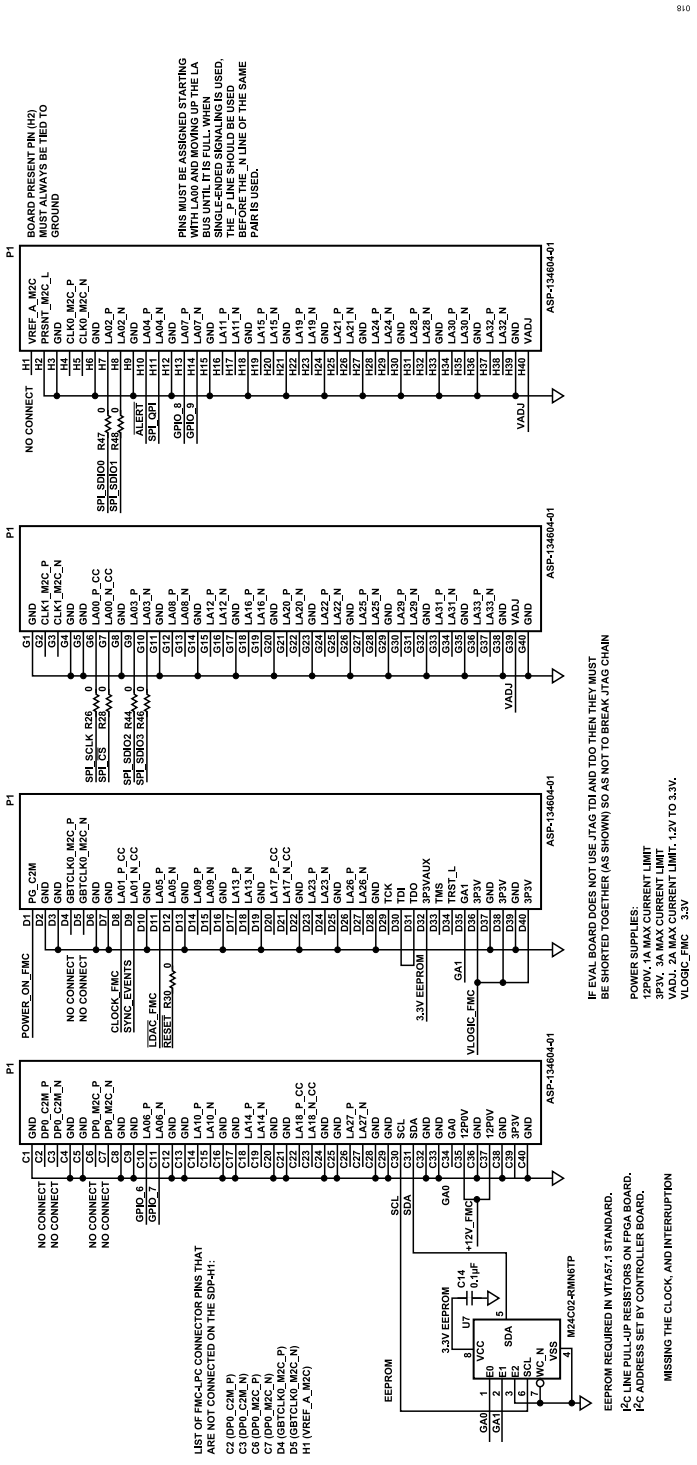

Figure 19. FMC Connector and Electronically Erasable Programmable Read-Only Memory (EEPROM)

EVALUATION BOARD SCHEMATICS

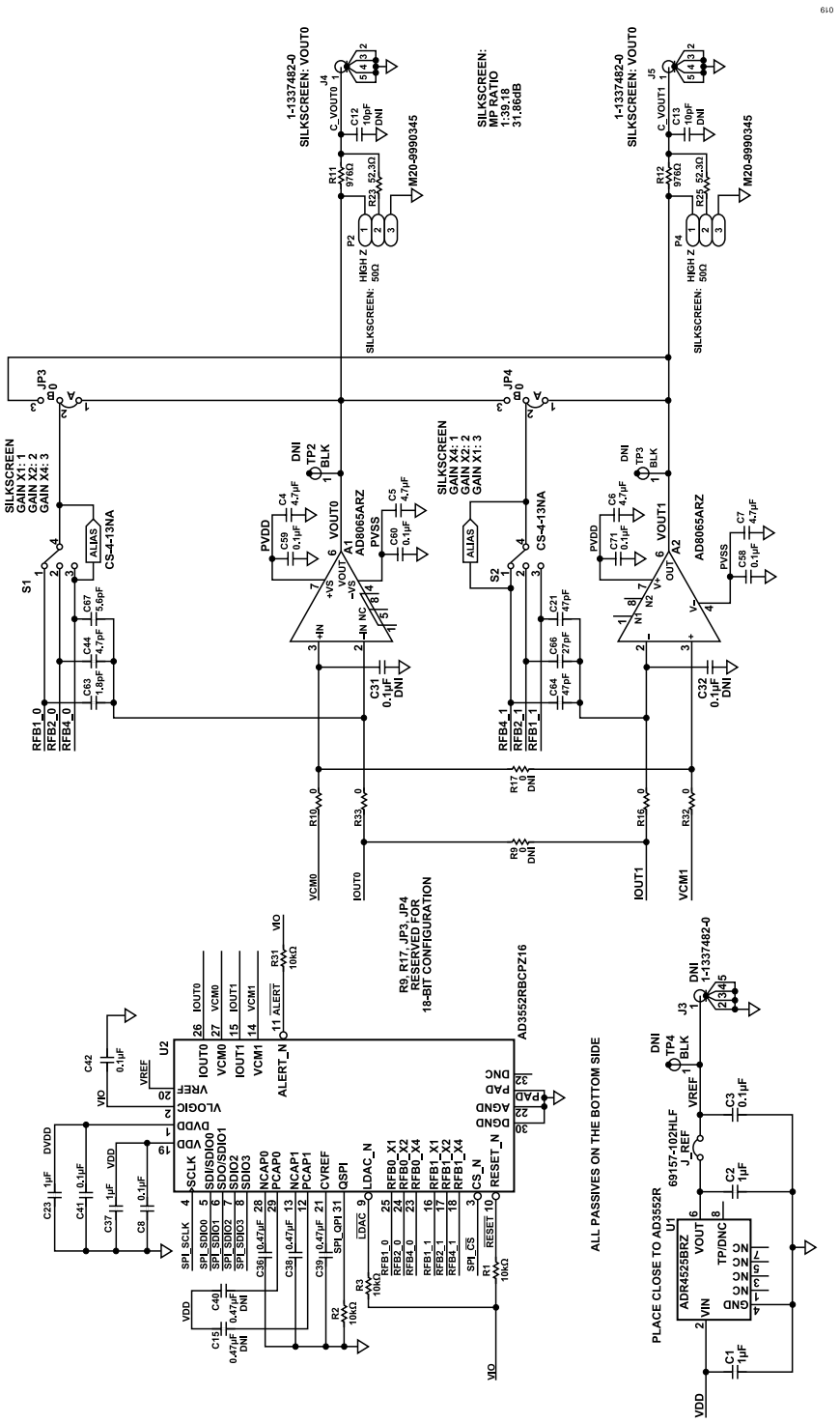

Figure 20. AD3552R, Amplifiers, and Reference

EVALUATION BOARD SCHEMATICS

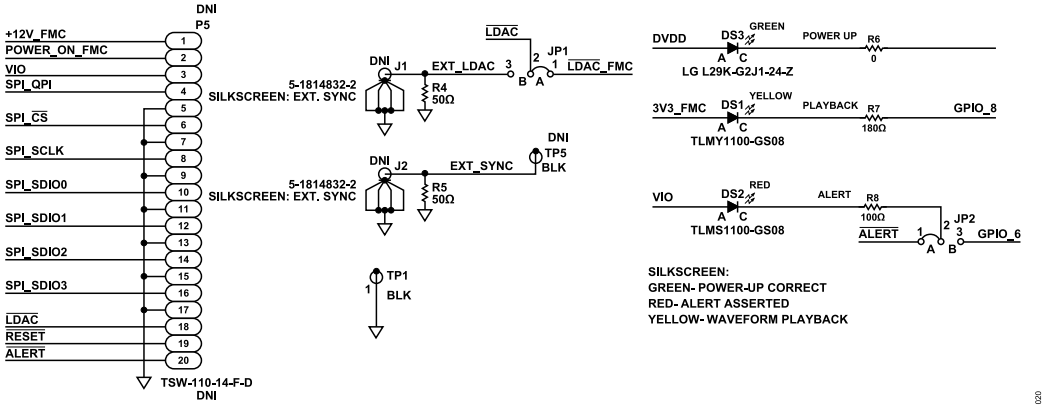

Figure 21. Digital Connectors and LEDs

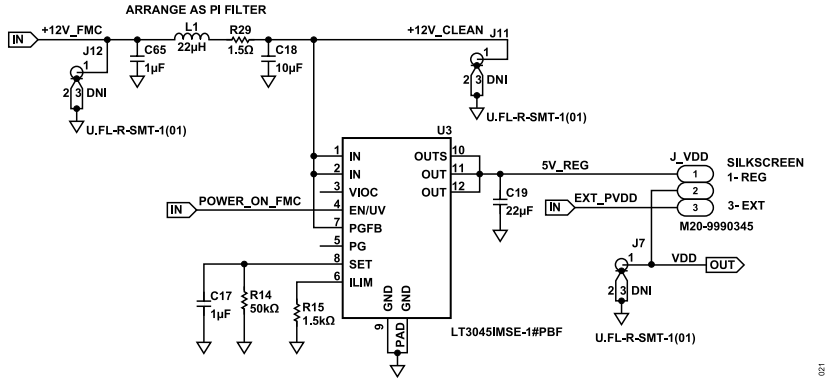

Figure 22. AV_{DD} LDO

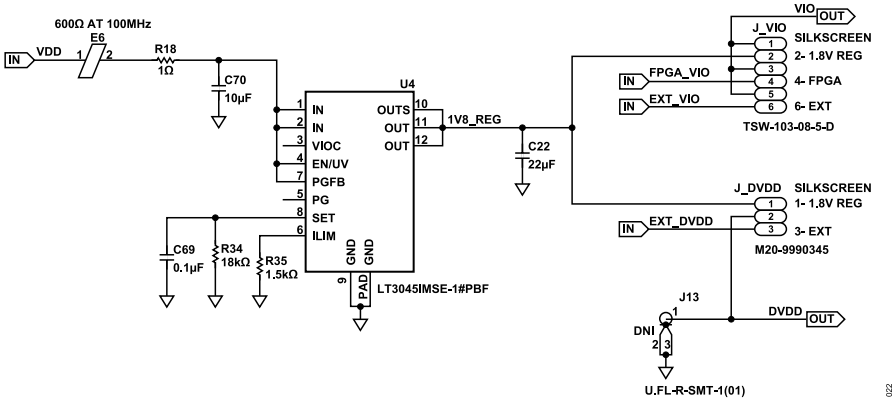

Figure 23. DV_{DD} and V_{LOGIC} LDOs

EVALUATION BOARD SCHEMATICS

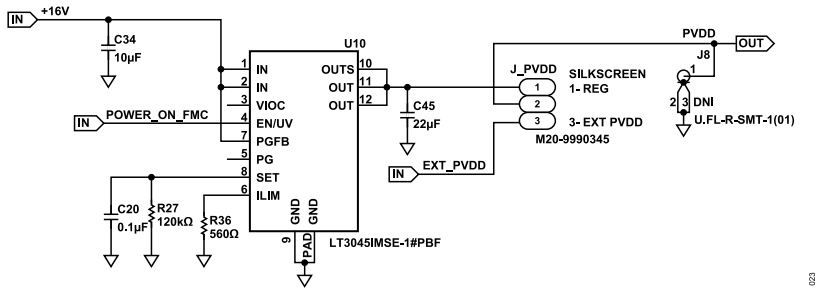

Figure 24. PV_{DD} LDO

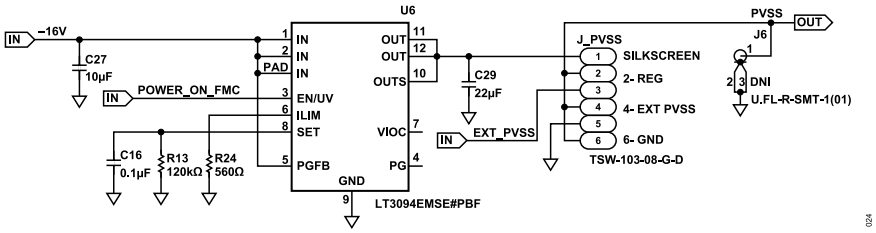

Figure 25. PV_{SS} LDO

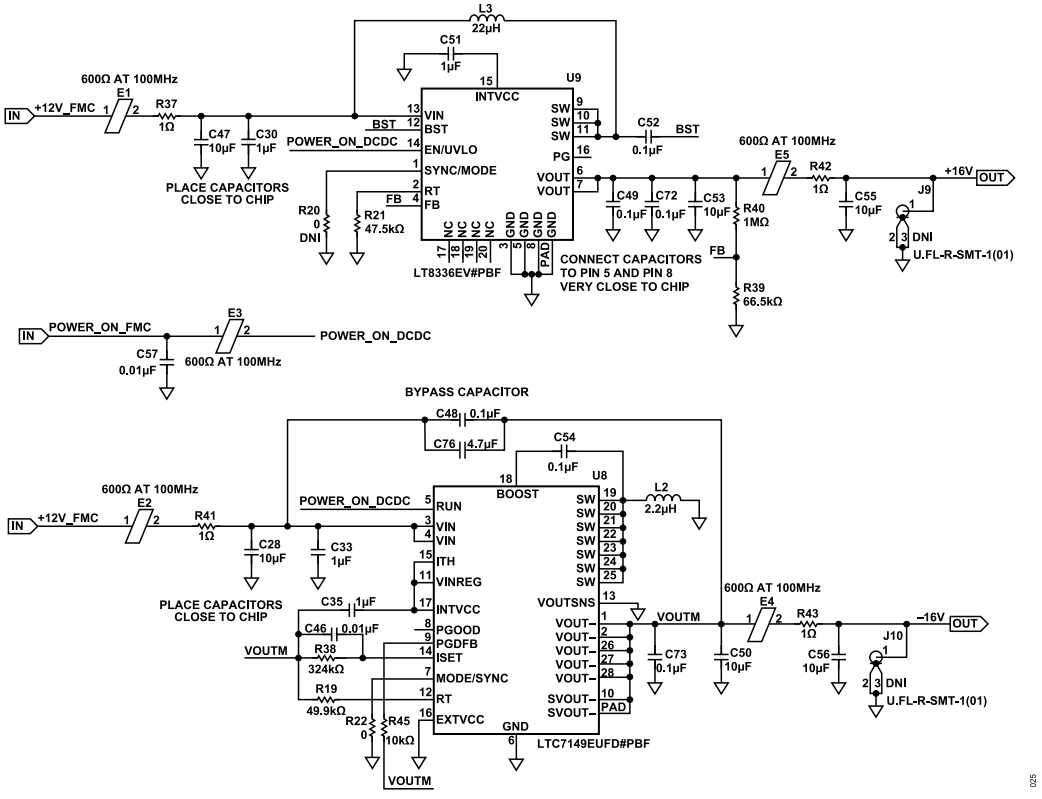

Figure 26. DC/DC Converters

EVALUATION BOARD SCHEMATICS

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.