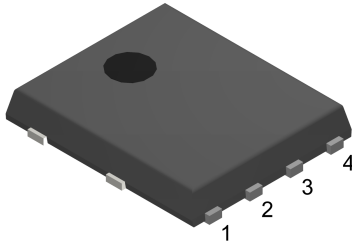
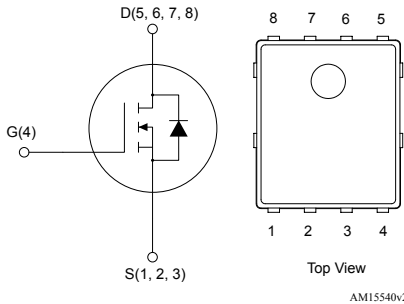


N-channel logic level 60 V, 2.5 mΩ max., 160 A, STripFET F7 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D
STL160N6LF7	60 V	2.5 mΩ	160 A

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Logic level V_{GS(th)}

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



Product status link

[STL160N6LF7](#)

Product summary

Order code	STL160N6LF7
Marking	160N6LF7
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	60	V
V _{GS}	Gate-source voltage	±20	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C ⁽²⁾	160	A
	Drain current (continuous) at T _C = 100 °C ⁽²⁾	110	
	Drain current (continuous) at T _C = 25 °C ⁽³⁾	120	
I _{DM} ⁽¹⁾⁽²⁾⁽⁴⁾	Drain current (pulsed)	640	A
P _{TOT}	Total power dissipation at T _C = 25 °C	125	W
I _{AS}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	60	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _{AV} = 60 A, R _{Gmin.} = 25 Ω)	141	mJ
T _J	Operating junction temperature range	-55 to 175	°C

1. Specified by design, not tested in production.
2. This is the theoretical current value only related to the silicon.
3. This current value is limited by package.
4. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJA} ⁽¹⁾	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still air)	15.6	°C/W
R _{thJC}	Thermal resistance, junction-to-case	1.2	°C/W

1. Defined according to JEDEC standards (JESD51-5, -7).

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.2		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 60\text{ A}$		2.0	2.5	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 60\text{ A}$		3.0	4.2	

1. Specified by design and evaluated by characterization, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}^{(1)}$	Input capacitance	$V_{DS} = 30\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	3700	-	pF
$C_{oss}^{(1)}$	Output capacitance		-	1550	-	pF
$C_{rss}^{(1)}$	Reverse transfer capacitance		-	70	-	pF
$Q_g^{(1)}$	Total gate charge	$V_{DD} = 30\text{ V}$, $I_D = 60\text{ A}$, $V_{GS} = 0$ to 10 V (see Figure 18. Test circuit for gate charge behavior)	-	63	-	nC
		$V_{DD} = 30\text{ V}$, $I_D = 60\text{ A}$, $V_{GS} = 0$ to 4.5 V (see Figure 18. Test circuit for gate charge behavior)	-	33	-	nC
$Q_{gs}^{(1)}$	Gate-source charge	$V_{DD} = 30\text{ V}$, $I_D = 60\text{ A}$, $V_{GS} = 0$ to 4.5 V	-	12	-	nC
$Q_{gd}^{(1)}$	Gate-drain charge	(see Figure 18. Test circuit for gate charge behavior)	-	14	-	nC
$R_g^{(1)}$	Intrinsic gate resistance		-	2	-	Ω
$Q_{g(sync)}^{(1)}$	Total gate charge, sync. MOSFET	$I_D = 60\text{ A}$, $V_{GS} = 0$ to 10 V	-	52	-	nC
$Q_{oss}^{(1)}$	Output charge	$V_{DD} = 30\text{ V}$, $V_{GS} = 0\text{ V}$	-	64	-	nC

1. Specified by design and evaluated by characterization, not tested in production.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ ⁽¹⁾	Turn-on delay time	$V_{DD} = 30 \text{ V}$, $I_D = 60 \text{ A}$,	-	14	-	ns
t_r ⁽¹⁾	Rise time	$R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$	-	7	-	ns
$t_{d(off)}$ ⁽¹⁾	Turn-off delay time	(see Figure 17. Test circuit for resistive load switching times and Figure 21. Unclamped inductive waveform)	-	57	-	ns
t_f ⁽¹⁾	Fall time		-	16	-	ns

1. Specified by design and evaluated by characterization, not tested in production.

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} ^{(1) (2)}	Forward on current (continuous)		-		83	A
V_{SD}	Forward on voltage	$I_{SD} = 60 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.2	V
t_{rr} ⁽¹⁾	Reverse recovery time	$I_{SD} = 60 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	44		ns
Q_{rr} ⁽¹⁾	Reverse recovery charge	$V_{DD} = 48 \text{ V}$	-	40		nC
I_{RRM} ⁽¹⁾	Reverse recovery current	(see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	1.8		A

1. Specified by design and evaluated by characterization, not tested in production.

2. This is the theoretical current value only related to the silicon.

2.1 Electrical characteristics (curves)

Figure 1. Total power dissipation

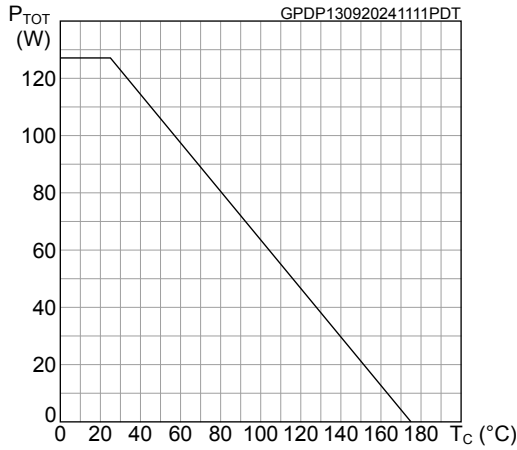


Figure 2. Drain current vs case temperature

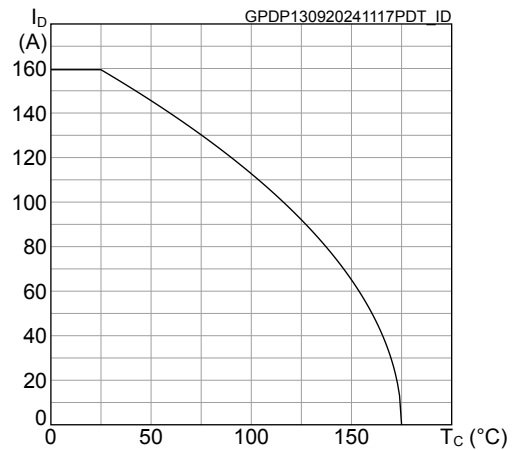


Figure 3. Safe operating area

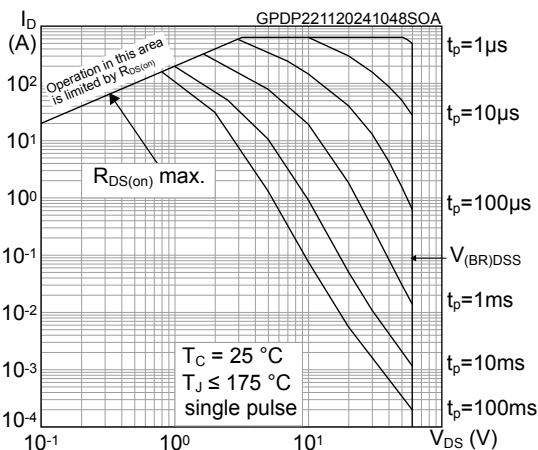


Figure 4. Normalized transient thermal impedance

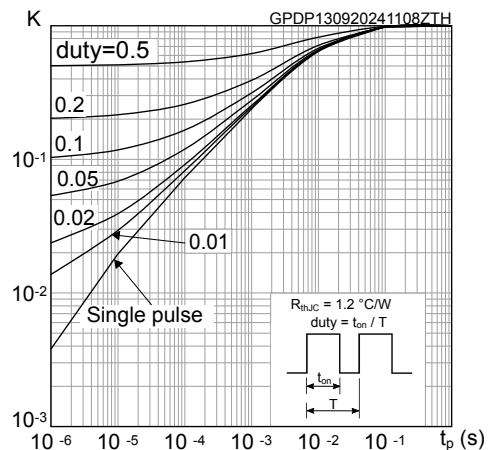


Figure 5. Typical output characteristics

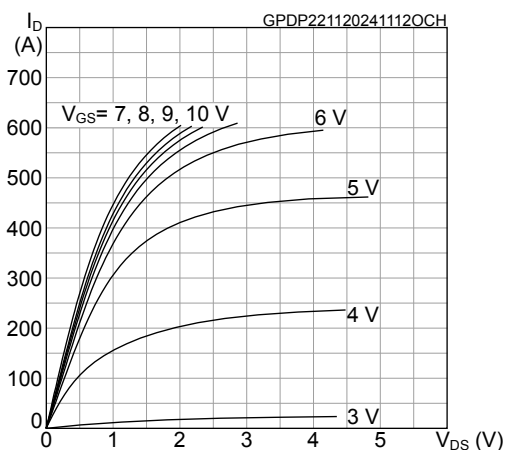


Figure 6. Typical transfer characteristics

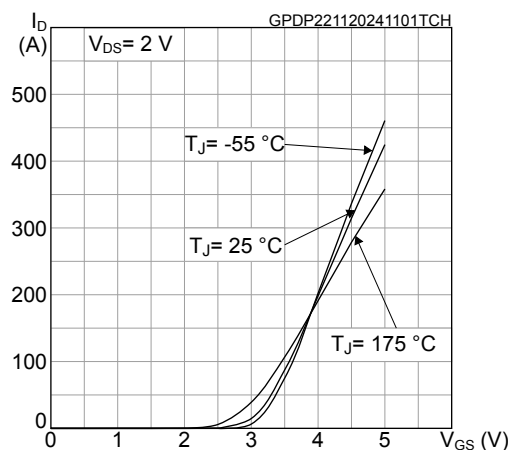


Figure 7. Typical gate charge characteristics

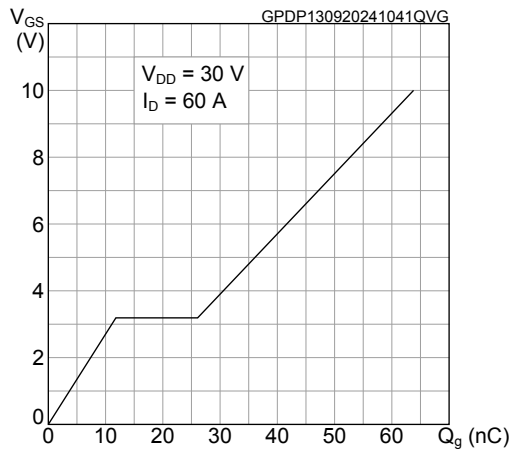


Figure 8. Typical capacitance characteristics

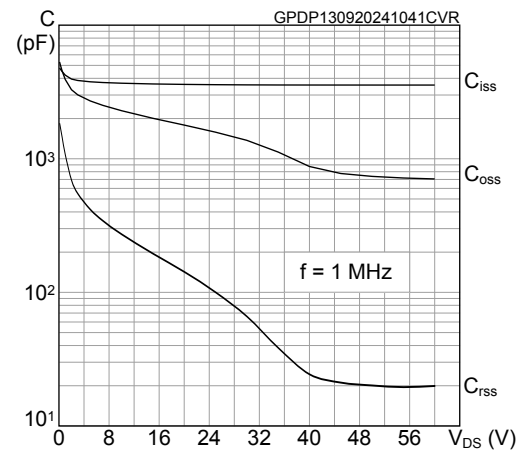


Figure 9. Avalanche characteristics

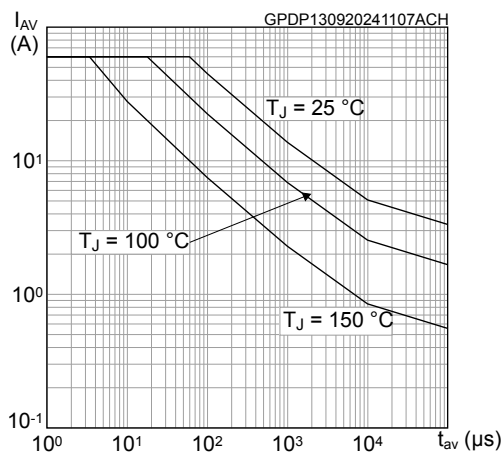


Figure 10. Avalanche energy

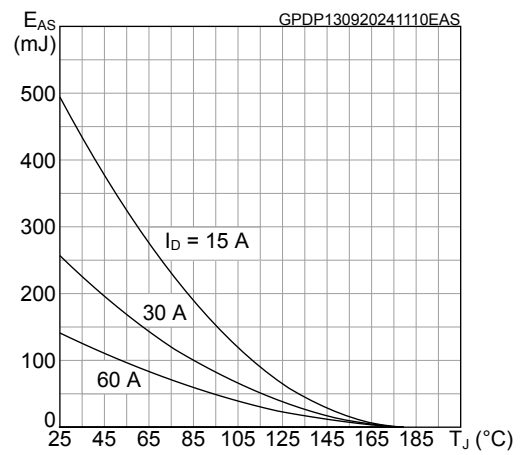


Figure 11. Typical drain-source on-resistance

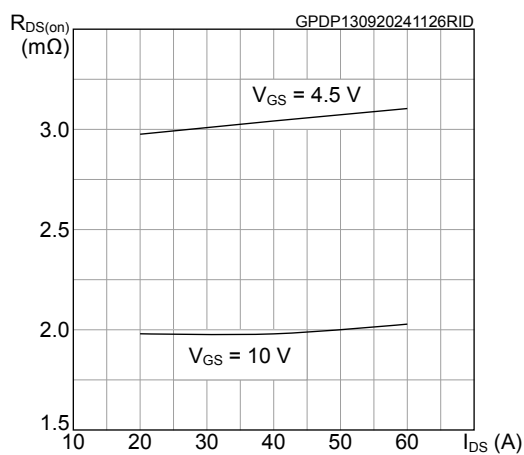


Figure 12. Typical on-resistance vs gate-source voltage

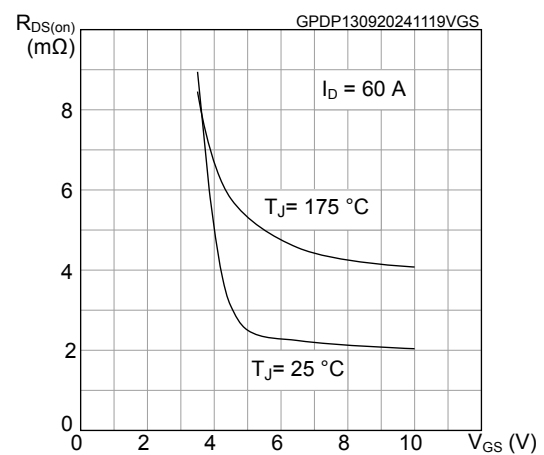


Figure 13. Normalized on-resistance vs temperature

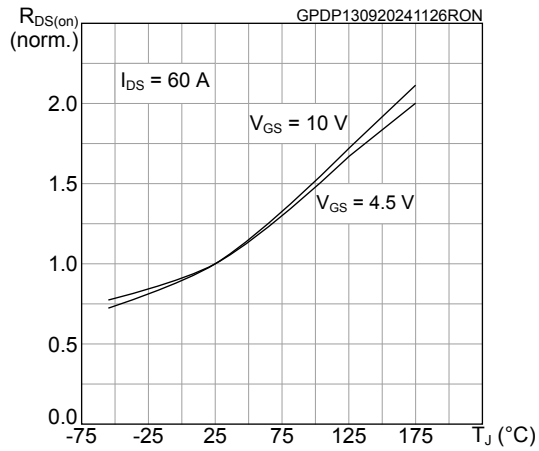


Figure 14. Normalized gate threshold voltage vs temperature

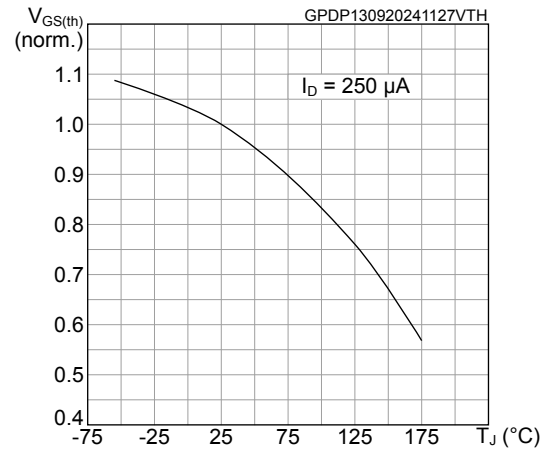


Figure 15. Typical reverse diode forward characteristics

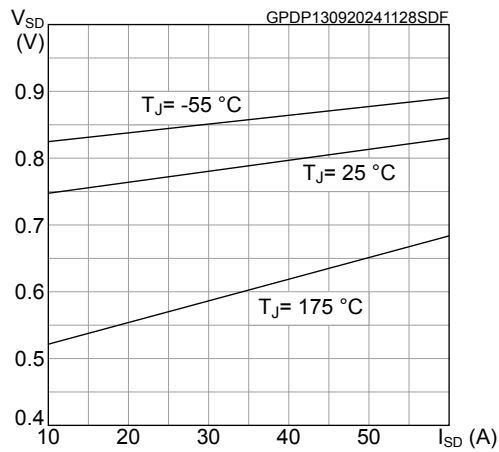
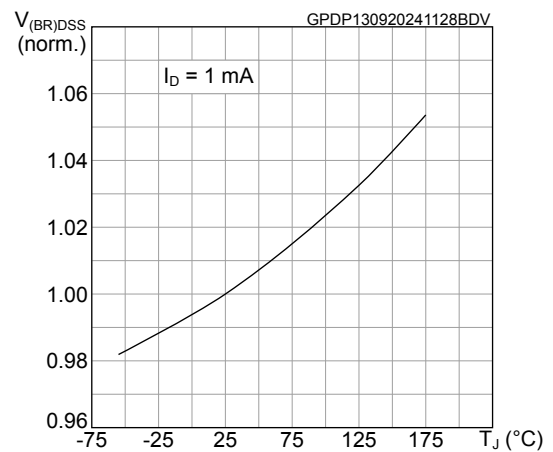
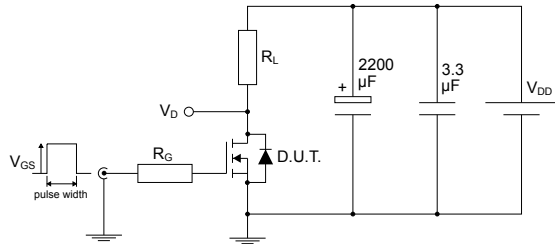


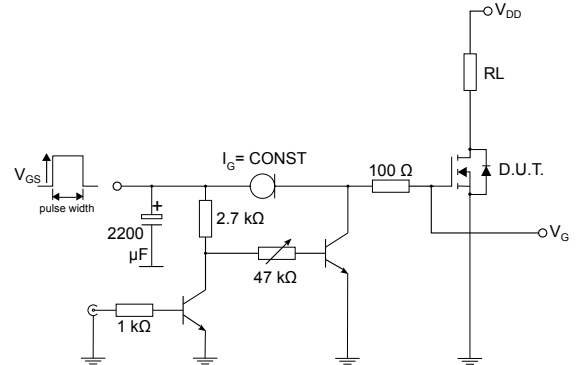
Figure 16. Normalized $V_{(BR)DSS}$ vs temperature



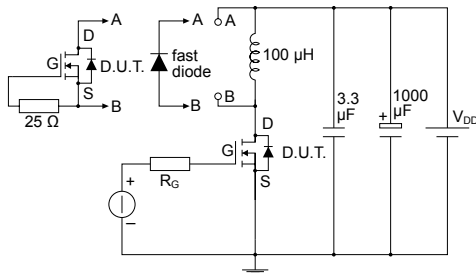
3 Test circuits

Figure 17. Test circuit for resistive load switching times


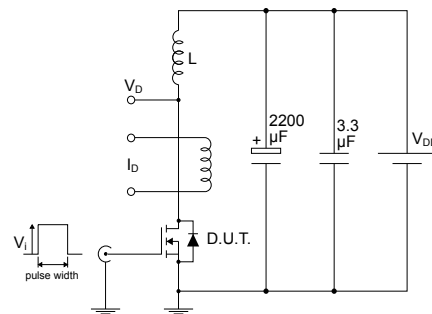
AM01468v1

Figure 18. Test circuit for gate charge behavior


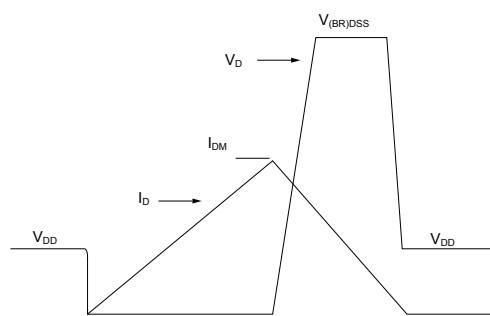
AM01469v10

Figure 19. Test circuit for inductive load switching and diode recovery times


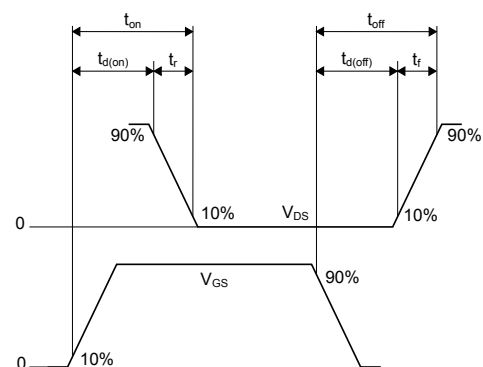
AM01470v1

Figure 20. Unclamped inductive load test circuit


AM01471v1

Figure 21. Unclamped inductive waveform


AM01472v1

Figure 22. Switching time waveform


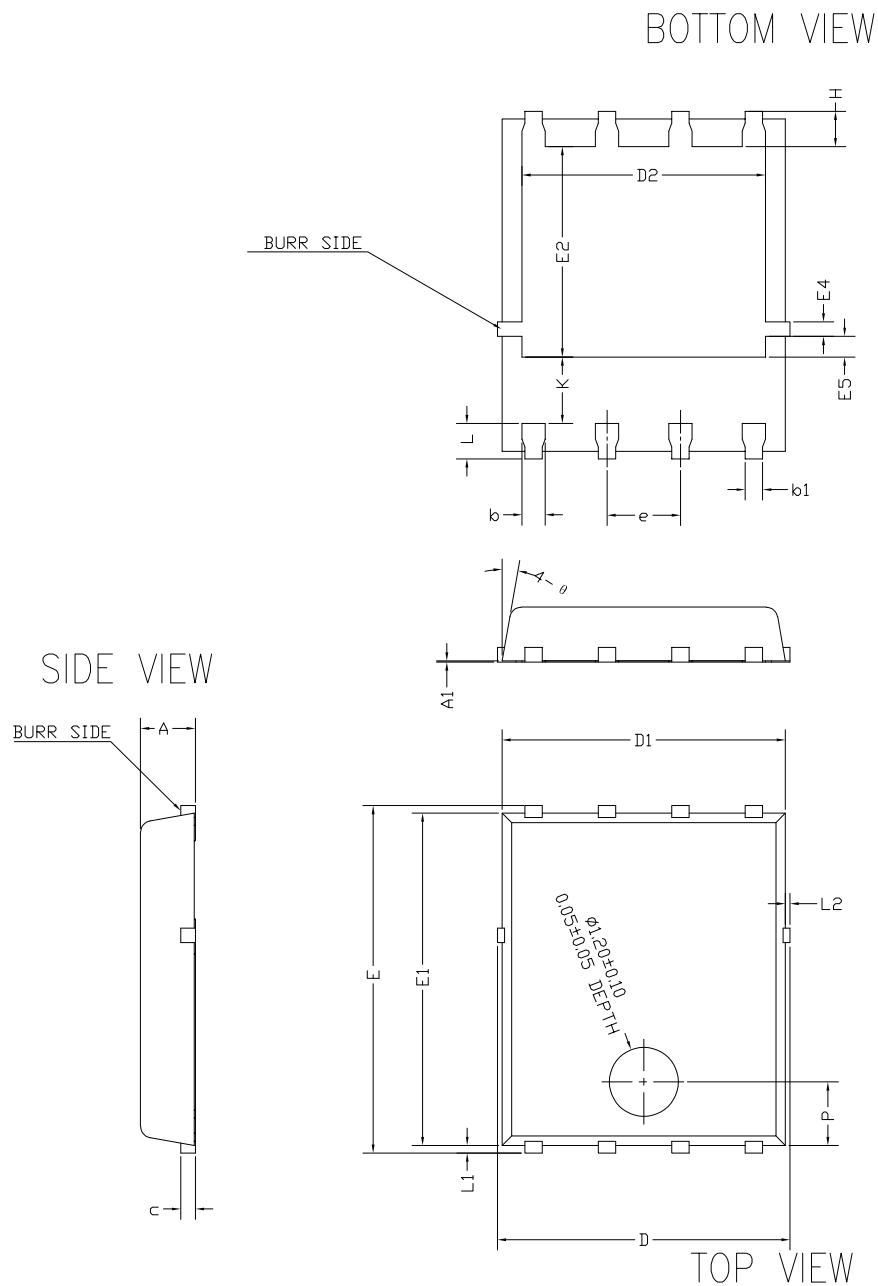
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 type B package information

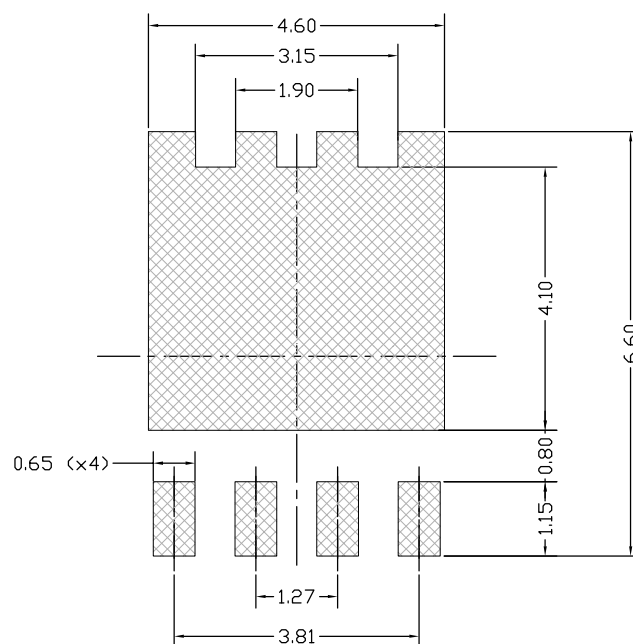
Figure 23. PowerFLAT 5x6 type B package outline



Drawing_8472137_typeB rev5

Table 7. PowerFLAT 5x6 type B mechanical data

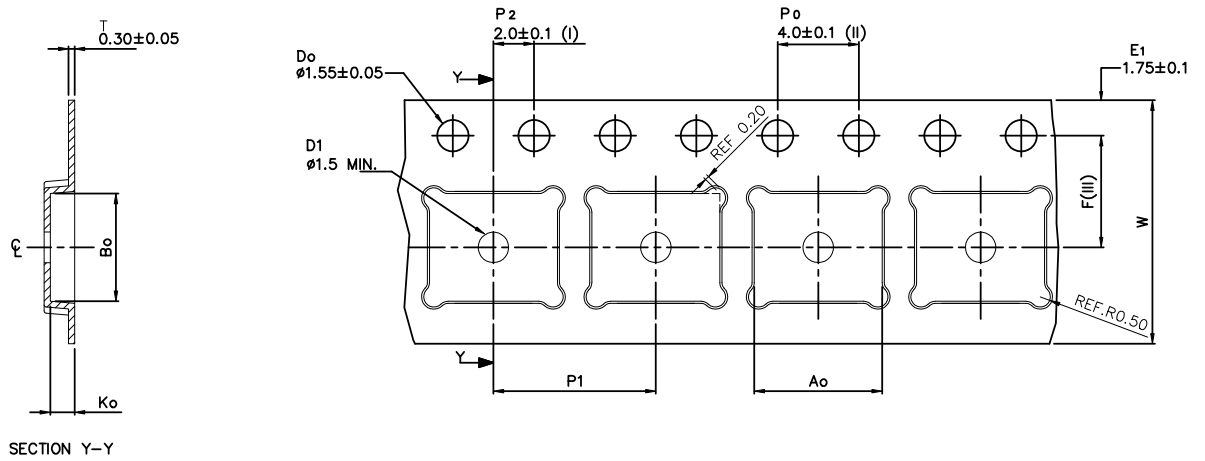
Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D	4.80		5.10
D1	4.80	4.90	5.00
D2	4.01	4.21	4.31
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.54	3.64	3.74
E4	0.15	0.25	0.35
E5	0.26	0.36	0.46
H	0.51	0.61	0.71
K	0.95		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

Figure 24. PowerFLAT 5x6 recommended footprint (dimensions are in mm)


Footprint_8472137_typeB rev5

4.2 PowerFLAT 5x6 packing information

Figure 25. PowerFLAT 5x6 tape (dimensions are in mm)



A_0	6.30 +/- 0.1
B_0	5.30 +/- 0.1
K_0	1.20 +/- 0.1
F	5.50 +/- 0.1
P_1	8.00 +/- 0.1
W	12.00 +/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 26. PowerFLAT 5x6 package orientation in carrier tape

Pin 1 identification

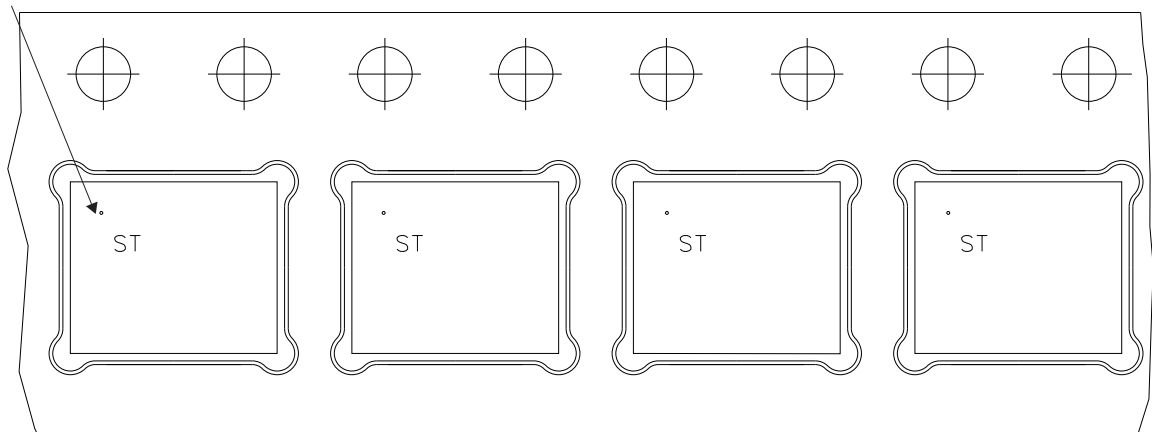
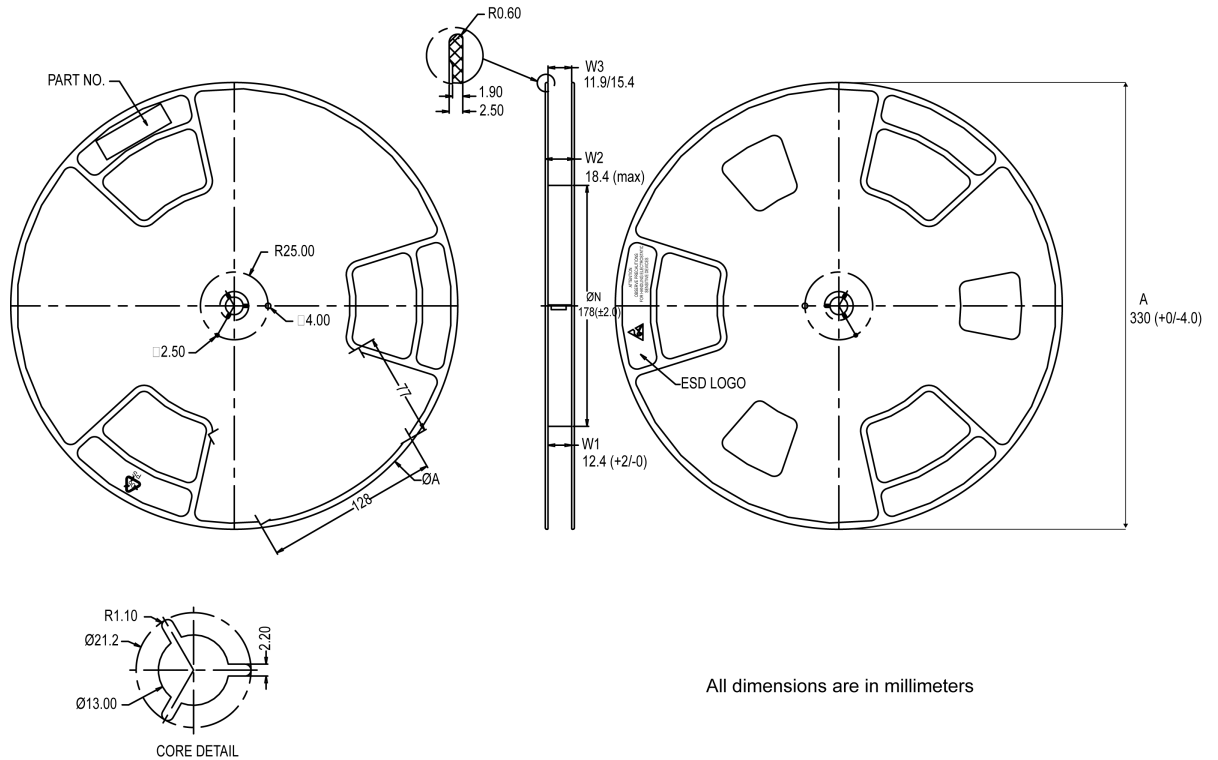


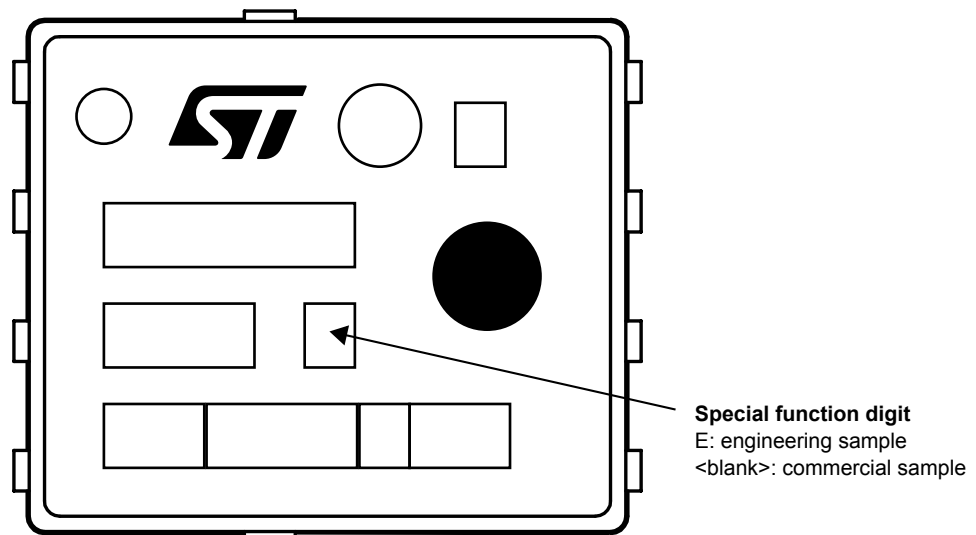
Figure 27. PowerFLAT 5x6 reel



8234350_Reel_rev_C

4.3 PowerFLAT 5x6 marking information

Figure 28. PowerFLAT 5x6 marking information



Note: *Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.*

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

Revision history

Table 8. Document revision history

Date	Version	Changes
09-Nov-2018	1	First release.
20-Sep-2024	2	Updated title and <i>Features</i> in cover page. Updated <i>Section 1: Electrical ratings</i> , <i>Section 2: Electrical characteristics</i> and <i>Section 4.1: PowerFLAT 5x6 type B package information</i> . Added <i>Section 2.1: Electrical characteristics (curves)</i> . Minor text changes.
13-Dec-2024	3	Updated <i>Table 2. Thermal data</i> . Added <i>Figure 3. Safe operating area</i> , <i>Figure 5. Typical output characteristics</i> and <i>Figure 6. Typical transfer characteristics</i> .
26-Mar-2025	4	Updated <i>Figure 9. Avalanche characteristics</i> .

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information	9
4.1	PowerFLAT 5x6 type B package information	9
4.2	PowerFLAT 5x6 packing information	11
4.3	PowerFLAT 5x6 marking information	12
	Revision history	13

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