STDRIVE102BH, STDRIVE102H

Datasheet

Triple half-bridge gate driver with programmable currents

VFQFPN 48L, 6x6x1 mm

VFQFPN 40L, 5x5x1 mm

STDRIVE

Product status link
STDRIVE102BH
STDRIVE102H

Product label
SUSTAINABLE TECHNOLOGY

Features

- Operating voltage from 6 to 50 V
- Gate drivers with programmable current capability up to:
  - 1 A source current
  - 2 A sink current
- High robustness against below-ground and overshoot
- Charge pump for 100 % duty cycle operation with dedicated undervoltage lockout protection
- Flexible power management:
  - 12 V LDO linear regulator with dedicated undervoltage lockout protection
  - 3.3 V LDO linear regulator with dedicated undervoltage lockout protection
- Standby mode for low consumption less than 50 nA
- Thermal shutdown protection
- V_{DS} monitoring for safe driving operation of the power MOSFETs
- Flexible analog front-end:
  - Up to three wide-bandwidth operational amplifiers
  - Up to three high-speed comparators
- Dual control modes:
  - ENx/INx
  - INHx/INLX with interlocking
- Matched propagation delay for all channels
- Logic inputs up to 5 V, TTL compatible

Applications

- Battery supplied power tools
- Portable vacuum cleaners
- E-bikes
- Industrial automation
- Robotics
- Pumps and fans

Description

The STDRIVE102BH and the STDRIVE102H are triple half-bridge gate drivers suitable for 3-phase brushless motor driving.

The STDRIVE102BH/H is the optimal solution for battery supplied motor driver applications such as power tools, vacuum cleaner and small appliances thanks to its very efficient stand-by mode, that strongly reduce the current consumption when the device is not active.

The gate drivers are designed to drive, with a programmable gate current, six external N-channel power MOSFETs, allowing a superior performance of the power stage and regulating the slew rate of power outputs without the need of external gate resistors. The different configurations of the drivers can be selected through two analog pins (IGATE and TCC).

An integrated charge pump supplies the three high-side drivers, enabling unlimited on-time of the high-side MOSFETs.

An embedded 12 V LDO linear regulator provides the supply of the three low-side drivers and its output is available on the VCC pin, to also supply external loads.

Another LDO linear regulator provides a 3.3 V on the VDD pin to supply external low-voltage components and the embedded analog front-end (AFE), which has a different configuration, depending on the device part number: the STDRIVE102BH integrates three operational amplifiers and three comparators, the STDRIVE102H integrates one operational amplifier and two comparators. In a typical application, the operational amplifiers can be used to monitor the voltage across the shunt resistor(s) sensing the current flowing in the motor phases. Concurrently, the comparators can be used to detect dangerous overcurrent conditions.

A full set of embedded protections is present to increase the overall application robustness: undervoltage lockout (UVLO) on each supply (VCC, VDD, and charge pump voltage), thermal shutdown, and a V_{DS} monitoring on both high-side and low-side MOSFETs. In case a protection is triggered, the nFAULT open-drain pin signals the event. The STDRIVE102BH has another dedicated open-drain pin (FLAG) which indicates whether the gate driver supply V_{CC} falls below the guard limit. The device integrates a smart shutdown function which allows immediate turn-off of the outputs of the gate driver in the case of fault, by minimizing the propagation delay between the fault detection event and the actual output switch-off.

In addition to the main supply pin (VS), the STDRIVE102BH/H has dedicated pin VM, which should be connected to the motor supply voltage, in correspondence of the drains of the high side N-channel MOSFETs. The VM pin is used for the integrated V_{DS} monitoring as well as a reference voltage for the charge pump. To increase device's flexibility, the VS and VM pin can operate at different voltages.

1 Block diagram

Figure 1. **STDRIVE102BH block diagram**

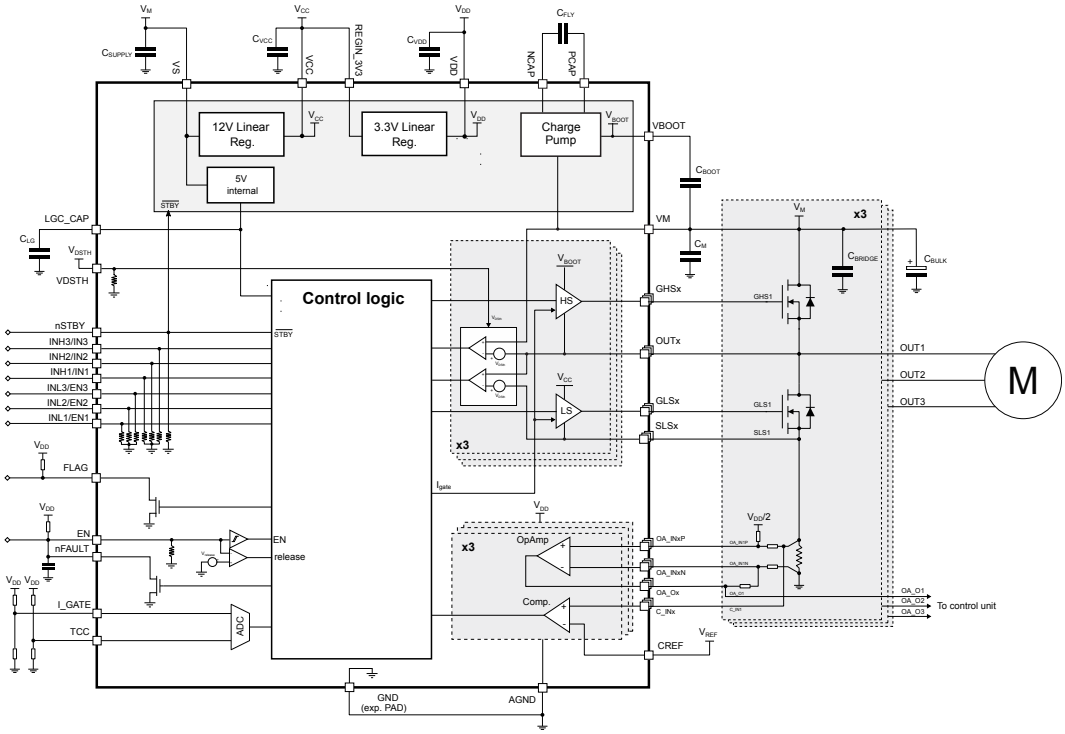
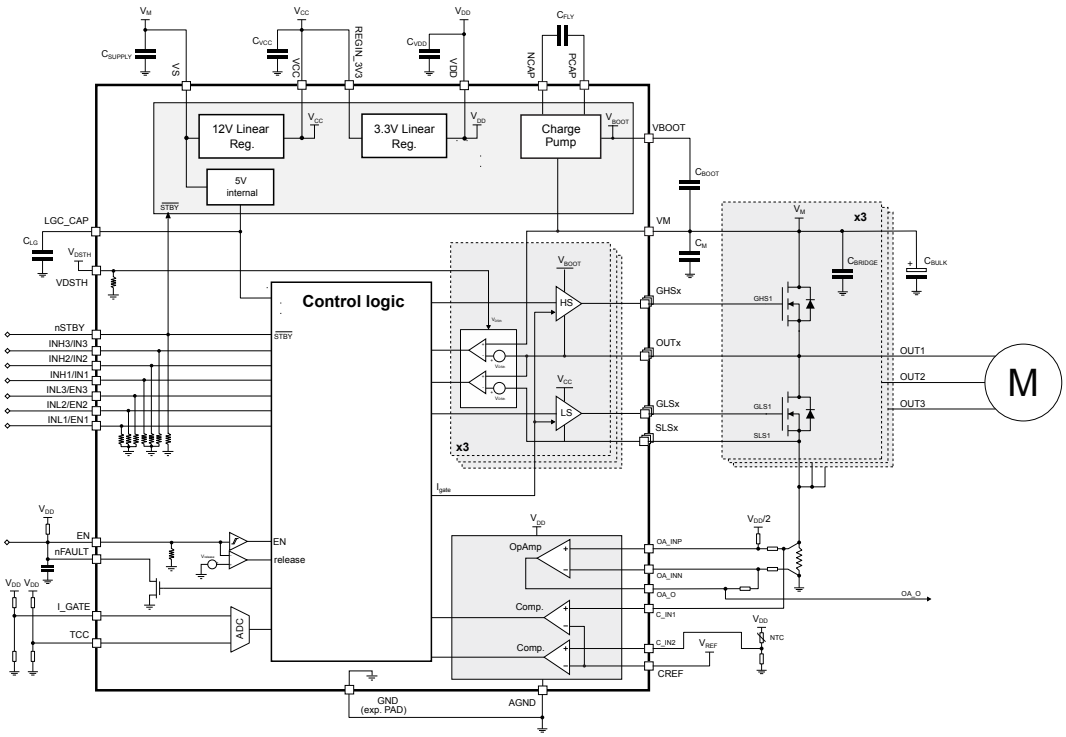


Figure 2. **STDRIVE102H block diagram**



2 Device ratings

2.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 1 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Two separated reference grounds are present in the device: GND and AGND. All voltages reported in Table 1 are considered shorting AGND and GND pins, unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
Power supply				
V_M	Motor supply voltage		-0.3 to 55	V
V_S	12 V LDO linear regulator input and main supply		-0.3 to 55	V
V_{CC}	12 V LDO linear regulator output and gate drivers supply voltage		-0.3 to 18	V
V_{REGIN_3V3}	3.3 V LDO linear regulator input		-0.3 to 18	V
V_{DD}	3.3 V LDO linear regulator output and analog front-end supply		-0.3 to 4	V
V_{NCAP}	Charge pump switching capacitor negative side		-0.3 to V_S+0.3	V
V_{PCAP}	Charge pump switching capacitor positive side		V_M-0.3 to V_{BOOT}+0.3	V
			65	V
V_{BOOT}	Charge pump output/ high-side boot supply		V_M-0.3 to V_M+18	V
			65	V
Gate drivers				
V_{SLSx}	Low-side reference pin voltage	DC	-2 to +2	V
		Transient pulse duration 200 ns Repetition frequency 20 kHz (1)	-8 to +8	V
V_{GLSx}	Low-side driver's output voltage		V_{SLSx}-0.3 to V_{CC}+0.3	V
V_{GS_LSx}	Differential voltage between low-side driver's output and its reference (V_{GLSx} - V_{SLSx})		-0.3 to 18	V
V_{supply_LS}	Supply rail of the low-side driver (V_{CC} - V_{SLSx})		-0.3 to 18	V
V_{OUTx}	OUTx pin voltage	DC	-4 to V_M+4	V
		Transient pulse duration between 200 ns and 5 µs Repetition frequency 20 kHz	-8 to V_M+8	V
		Transient pulse duration 200 ns Repetition frequency 20 kHz	-10 to V_M+10	V
V_{GHSx}	High-side driver's output		V_{OUTx} -0.3 to V_{BOOT}+0.3	V
V_{GO_HSx}	Differential voltage between high-side gate driver's output and its reference (V_{GHSx} - V_{OUTx})	(2)	-0.3 to 16	V

Symbol	Parameter	Test condition	Value	Unit
$V_{BO,x}$	Supply rail of the high-side driver (V_{BOOT} - V_{OUTx})		-0.3 to 65	V
Analog pins and digital I/O				
V_{IO}	Logic IO voltage (INHx/INx, INLx/ENx, nSTBY, EN pins)		-0.3 to 5.5	V
V_{in_analog}	Analog input pins for device configuration (IGATE, TCC, VDSTH)		-0.3 to 5.5	V
V_{OD}	Open-drain pins voltage (nFAULT, FLAG)		-0.3 to 5.5	V
V_{C_IN}	C_INx input		-0.3 to V_{DD}+0.3	V
V_{CREF}	CREF input		-0.3 to V_{DD}+0.3	V
V_{OA_INxP}	Operational amplifiers positive inputs		-0.3 to V_{DD}+0.3	V
V_{OA_INxN}	Operational amplifiers negative inputs		-0.3 to V_{DD}+0.3	V
V_{OA_Ox}	Operational amplifiers output		-0.3 to V_{DD}+0.3	V
Temperature				
T_{stg}	Storage temperature		-55 to 150	°C
T_j	Junction temperature		-40 to 150	°C
Reference grounds				
ΔV_{GND}	GND misalignment	AGND with respect to GND (exposed pad)	-0.3 to +0.3	V

1. *V_{supply_LS} AMR must be also considered.*
2. *Limit to avoid V_{GS} clamp turn-on.*

2.2 Recommended operating conditions

All voltages must be considered shorting AGND and GND pins.

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_M	Motor supply voltage		6		50	V
V_S	12 V LDO linear regulator input	(1)	V_{CC}		50	V
V_{CC}	VCC gate drivers' supply voltage	VCC supplied by internal linear regulator		12		V
		VS shorted to VCC and externally supplied	6		15	V
I_{CC}	12 V linear regulator output current	(1) (2)			50	mA
C_{VCC}	12 V LDO linear regulator output capacitor	(3)		4.7		µF
V_{BOOT}	Charge pump output voltage			V_M + V_{CC}		V
I_{BOOT}	Charge pump current	(2)			35	mA
V_{REGIN_3V3}	3.3 V LDO linear regulator input		V_{DD}		15	V
V_{DD}	3.3 V LDO linear regulator output	VDD supplied by internal linear regulator		3.3		V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	3.3 V LDO linear regulator output	REGIN_3V3 shorted to VDD and externally supplied	3.1	3.3	3.6	V
I_{DD}	3.3 V LDO linear regulator output current	(1) (2)			30	mA
C_{VDD}	3.3 V output capacitor	(3)		4.7		µF
C_{LG}	Output capacitor for internal logic supply regulator (LGC_CAP pin)	(3)		4.7		µF
dV_{OUTx}/dt	OUTx slew rate				2.5	V/ns
$V_{IN,logic}$	Logic input voltage (INHx/INx, INLx/ENx, nSTBY, EN pins)	(4)	0		5	V
$V_{IN,analog}$	Analog configuration pins (IGATE, TCC)		0		V_{DD}	V
V_{OD}	nFAULT, FLAG pins pull-up voltage	(4)	0		5	V
I_{OD}	nFAULT, FLAG pins sink current				8	mA
V_{DSTH}	V_{DS} monitoring reference voltage	Protection enabled	0.05		2	V
		Protection disabled	3		3.3	V
V_{SLSx}	LSx driver sense pin		-1		+1	V
V_{OA_INxP}	Operational amplifiers positive inputs		-0.2		V_{DD}+0.2	V
V_{OA_INxN}	Operational amplifiers negative inputs		-0.2		V_{DD}+0.2	V
$V_{OP,icm}$	Input common-mode voltage range		-0.2		V_{DD}+0.2	V
$R_{eqL,out}$	Equivalent load resistor connected to the operational amplifiers output	Resistor to AGND or to VDD	1			kΩ
V_{C_IN}	Comparator input (C_INx pins)		0		V_{DD}	V
V_{CREF}	CREF input		0		V_{DD}	V
T_{amb}	Operative ambient temperature	(1)	-40		85	°C

1. *Actual operative range can be limited by thermal shutdown.*
2. *Consumption of internal circuitry included.*
3. *An additional 100 nF low-ESR bypass capacitor could be added to improve the noise immunity.*
4. *All digital inputs are compliant with TTL/CMOS thresholds and 5 V tolerant. They can be biased within the respective AMR whatever the supply condition of the device (supplied, floating, or shorted to ground) without causing damage to the device.*

2.3 Thermal data

Thermal values are calculated by simulation.

Table 3. STDRIVE102BH thermal data (VFQFPN 48L, 6x6x1 mm)

Symbol	Parameter	Test condition	Value	Unit
R_{thJA}	Junction-to-ambient thermal resistance	Natural convection according to JESD51-2a	32.1	°C/W
$R_{thJCtop}$	Junction-to-case thermal resistance (top side)	Cold plate on top, according to JESD51-12	15.8	°C/W
$R_{thJCbot}$	Junction-to-case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-12	3.4	°C/W
R_{thJB}	Junction-to-board thermal resistance	According to JESD51-8	15.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	According to JESD51-2a	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	According to JESD51-2a	15	°C/W

Table 4. STDRIVE102H thermal data (VFQFPN 40L, 5x5x1 mm)

Symbol	Parameter	Test condition	Value	Unit
R_{thJA}	Junction-to-ambient thermal resistance	Natural convection according to JESD51-2a	36.3	°C/W
$R_{thJCtop}$	Junction-to-case thermal resistance (top side)	Cold plate on top, according to JESD51-12	19.5	°C/W
$R_{thJCbot}$	Junction-to-case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-12	4.0	°C/W
R_{thJB}	Junction-to-board thermal resistance	According to JESD51-8	18.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	According to JESD51-2a	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	According to JESD51-2a	17.7	°C/W

2.4 Electrical sensitivity characteristics

Table 5. ESD protection ratings

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human Body Model	Conforming to ANSI/ESDA/JEDEC JS-001-2017	2	2000	V
CDM	Charge Device Model	Conforming to ANSI/ESDA/JEDEC JS-002-2018	C3	1000	V

3 Electrical characteristics

Testing conditions: V_M = 24 V, V_S = 12 V, V_{CC} = 12 V, V_{REGIN_3V3} = 3.3 V, V_{DD} = 3.3 V, V_{DSTH} = 3.3 V, all gate drivers LOW (sinking current) unless otherwise specified.

Typical values are tested at T_j = 25 °C, minimum and maximum values are guaranteed by thermal characterization in the temperature range of -40 to 125 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply and UVLO protection						
$V_{CC(On)}$	V_{CC} UVLO turn-on threshold	V_{CC} rising		5.5	5.8	V
$V_{CC(Hyst)}$	V_{CC} UVLO hysteresis	V_{CC} falling		0.25		V
$V_{CC(Off)}$	V_{CC} UVLO turn-off threshold	V_{CC} falling	5.0	5.25		V
$V_{P\_GOOD(On)}$	V_{CC} power-good warning release threshold	V_{CC} rising		7.75		V
$V_{P\_GOOD(Hyst)}$	V_{CC} power-good warning hysteresis	V_{CC} falling		0.25		V
$V_{P\_GOOD(Off)}$	V_{CC} power-good warning threshold	V_{CC} falling		7.50		V
$V_{CPump(On)}$	V_{BOOT} - V_M UVLO turn-on threshold	'V_{BOOT} - V_M' rising		4.5	5.2	V
$V_{CPump(Hyst)}$	V_{BOOT} - V_M UVLO hysteresis	'V_{BOOT} - V_M' falling		0.2		V
$V_{CPump(Off)}$	V_{BOOT} - V_M UVLO turn-off threshold	'V_{BOOT} - V_M' falling	3.6	4.3		V
$V_{DD(On)}$	V_{DD} UVLO turn-on threshold	V_{DD} rising		2.6	2.9	V
$V_{DD(Hyst)}$	V_{DD} UVLO hysteresis	V_{DD} falling		0.2		V
$V_{DD(Off)}$	V_{DD} UVLO turn-off threshold	V_{DD} falling	2.2	2.4		V
I_{STBY}	Standby current consumption	V_M = V_S = 50 V T_j = 25 °C			50	nA
12 V LDO linear regulator						
V_{CC}	12 V linear regulator output	V_S = 15 V, I_{CC} = 40 mA	11.45	12	12.55	V
$I_{CC,lim}$	12 V linear regulator current limitation	V_{CC} shorted to AGND	55	85	115	mA
3.3 V LDO linear regulator						
V_{DD}	3.3 V linear regulator output	V_{REGIN_3V3} = 12 V I_{DD} = 25 mA	3.13	3.3	3.47	V
$I_{DD,lim}$	3.3 V linear regulator current limit	V_{DD} shorted to AGND	36	45	65	mA
Charge pump						
$f_{SW,CP}$	Charge pump switching frequency			90		kHz
Thermal shutdown						
$T_{j(THSD),rec}$	Thermal shutdown recovery temperature			135		°C
$T_{j(THSD)}$	Thermal shutdown temperature			150		°C
Gate drivers						
$I_{GATE,on}$	Gate driver source current capability	IGATE = V_{DD}		1000		mA
$I_{GATE,off}$	Gate driver sink current capability	IGATE = V_{DD}		2000		mA
$I_{hold,on}$	Gate driver hold current (source)			25		mA
$I_{hold,off}$	Gate driver hold current (sink)			50		mA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{clamp}	Gate driver clamp current			2140		mA
$t_{cc,on}$	Constant source current time	TCC at level 1, see Table 10		280		ns
		TCC at level 15, see Table 10		4800		ns
$t_{cc,off}$	Constant sink current time	TCC at level 1, see Table 10		140		ns
		TCC at level 15, see Table 10		2400		ns
$V_{GS,\ clamp}$	Clamping voltage protection on the high-side driver's output	$I_{GS,clamp}$ = 25 mA		17.5		V
$I_{OUTx,bias}$	OUTx bias current	$V_{OUTx} = V_M$ = 40 V IGATE = V_{DD}		300		µA
$t_{d,on}$	Turn-on propagation delay (input to output) (1)	C_{LOAD} = 1 nF, IGATE = V_{DD}		50		ns
$t_{d,off}$	Turn-off propagation delay (input to output) (1)	C_{LOAD} = 1 nF, IGATE = V_{DD}		45		ns
MT_{on-off}	Propagation delay matching between turn-on and off (2)	C_{LOAD} = 1 nF, IGATE = V_{DD}		5		ns
MT_{HL}	Propagation delay matching between HS and LS (3)	C_{LOAD} = 1 nF, IGATE = V_{DD}		7		ns
MT_{CH}	Propagation delay matching between channels (4)	C_{LOAD} = 1 nF, IGATE = V_{DD}		0		ns
V_{DS} monitoring protection						
$V_{DS,th}$	V_{DS} monitor protection threshold	VDSTH = 0.05 V	0.02	0.05	0.083	V
		VDSTH = 2 V	1.8	2	2.2	V
$V_{DSTH,en}$	V_{DS} monitor protection enable voltage				2.4	V
$V_{DSTH,dis}$	V_{DS} monitor protection disable voltage		3			V
$R_{PD,VDSTH}$	VDSTH pin pull-down resistor			450		kΩ
$t_{dg(VDS)}$	V_{DS} monitor protection deglitch filter time	TCC short to GND see Table 10		3.5		µs
Operational amplifiers						
$V_{OP,io}$	Input offset voltage		-5	0	5	mV
$I_{OP,ib}$	Input bias current	T_j = 25 °C (5)			100	pA
V_{OH}	High level output voltage (V_{DD} - V_{OA_Ox})	Output source current I_{OA_Ox} = +1 mA		30	100	mV
V_{OL}	Low level output voltage	Output sink current I_{OA_Ox} = -1 mA		30	100	mV
GBWP	Gain bandwidth product	R_L = 10kΩ, C_L = 100 pF		12		MHz
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF Buffer configuration		12		V/µs
Comparators						
$V_{COMP,io}$	Input offset voltage	CREF = 1.65 V	-15	0	15	mV
I_{CREF}	CREF pin input current	T_j = 25 °C (5)			1	nA
I_{C_IN}	C_INx pins input current	T_j = 25 °C (5)			1	nA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{dg(COMP)}$	Comparator deglitch filter time			1.3		µs
Logic inputs and outputs						
V_{IL}	Low logic input voltage				0.8	V
V_{IH}	High logic input voltage		2			V
$V_{IL,stby}$	nSTBY pin low logic input voltage				0.6	V
$V_{IH,stby}$	nSTBY pin high logic input voltage		2			V
$R_{PD,in}$	Input lines pull-down resistor (INHx/INx, INLx/ENx)			220		kΩ
$R_{PD,STBY}$	nSTBY pin pull-down resistor			440		kΩ
$R_{PD,EN}$	EN pin pull-down resistor			440		kΩ
$V_{OD,L}$	Open-drain output low voltage (nFAULT, FLAG)	I_{OD} = 8 mA			0.35	V
$V_{release}$	EN pin latch release threshold		0.37			V
$t_{EN,pulse\_rel}$	Latch release time		400			ns
t_{STBY}	Standby time	From nSTBY falling edge			100	µs
Analog control pins (IGATE and TCC pins)						
$\Delta V_{Actrl,in}$	Analog intervals			$V_{DD}/15$		V

1. *Refer to Figure 17, Figure 18, and Figure 19*
2. *The matching time, on the same driver, between the on and off transition is defined as* $|t_{d,on} - t_{d,off}|$
3. *The matching of the same parameter* ($t_{d,on}$ *or* $t_{d,off}$) *between the two drivers (HS and LS) of the same half-bridge is defined as*

   $|t_{d,on,HS} - t_{d,on,LS}|$ *or* $|t_{d,off,HS} - t_{d,off,LS}|$.
4. *The matching of the same parameter* ($t_{d,on}$ *or* $t_{d,off}$) *between the two drivers (HS and LS) of two different half-bridges (channels) "x" and "y" is defined as* $|t_{d,on,HSx} - t_{d,on,HSy}|$, $|t_{d,off,HSx} - t_{d,off,HSy}|$, $|t_{d,on,LSx} - t_{d,on,LSy}|$, $|t_{d,off,LSx} - t_{d,off,LSy}|$
5. *Guaranteed by design.*

4 Pin description

4.1 STDRIVE102BH pin description

Figure 3. **STDRIVE102BH pin description**

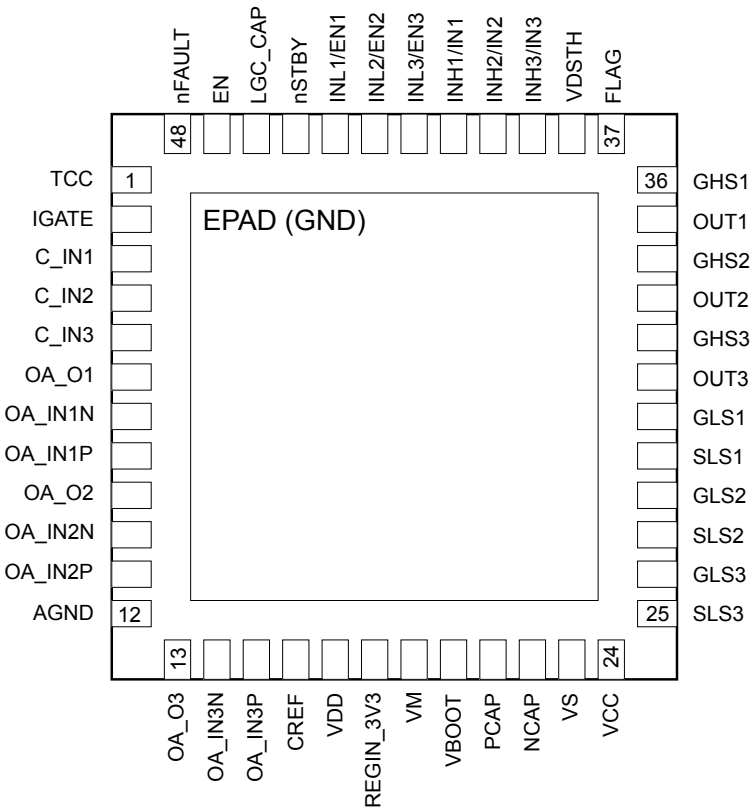


Table 7. **STDRIVE102BH pin list**

Pin N.	Name	Type	Function
1	TCC	Analog In	Analog input setting the constant-current time (refer to Section 5.2.1).
2	IGATE	Analog In	Analog input setting the gate drivers current (refer to Section 5.2.1).
3	C_IN1	Analog In	Non-inverting input of the comparator 1.
4	C_IN2	Analog In	Non-inverting input of the comparator 2.
5	C_IN3	Analog In	Non-inverting input of the comparator 3.
6	OA_O1	Analog Out	Output of the op amp 1.
7	OA_IN1N	Analog In	Inverting input of the op amp 1.
8	OA_IN1P	Analog In	Non-inverting input of the op amp 1.
9	OA_O2	Analog Out	Output of the op amp 2.
10	OA_IN2N	Analog In	Inverting input of the op amp 2.
11	OA_IN2P	Analog In	Non-inverting input of the op amp 2.
12	AGND	Power	Analog ground of the device. Connect this pin to EPAD or a suitable reference GND point.
13	OA_O3	Analog Out	Output of the op amp 3.
14	OA_IN3N	Analog In	Inverting input of the op amp 3.
15	OA_IN3P	Analog In	Non-inverting input of the op amp 3.

Pin N.	Name	Type	Function
16	CREF	Analog In	Common reference voltage for the three comparators (inverting input).
17	VDD	Power	3.3 V LDO linear regulator output and supply voltage of the Analog Front-End (AFE).
18	REGIN_3V3	Power	3.3 V LDO linear regulator input.
19	VM	Power	Motor supply voltage: reference for the internal charge pump and V_{DS} monitoring protection.
20	VBOOT	Power	Charge pump output voltage: high-side drivers supply.
21	PCAP	Power	Charge pump fly capacitor positive pin.
22	NCAP	Power	Charge pump fly capacitor negative pin.
23	VS	Power	Device power supply and 12 V LDO linear regulator input.
24	VCC	Power	12 V LDO linear regulator output and supply voltage of the low-side drivers.
25	SLS3	Analog	Phase 3 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 3).
26	GLS3	Analog	Phase 3 low-side driver output.
27	SLS2	Analog	Phase 2 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 2).
28	GLS2	Analog	Phase 2 low-side driver output.
29	SLS1	Analog	Phase 1 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 1).
30	GLS1	Analog	Phase 1 low-side driver output.
31	OUT3	Analog	Phase 3 high-side reference voltage (external half-bridge 3 output).
32	GHS3	Analog	Phase 3 high-side driver output.
33	OUT2	Analog	Phase 2 high-side reference voltage (external half-bridge 2 output).
34	GHS2	Analog	Phase 2 high-side driver output.
35	OUT1	Analog	Phase 1 high-side reference voltage (external half-bridge 1 output).
36	GHS1	Analog	Phase 1 high-side driver output.
37	FLAG	Digital Out	Open-drain pin for VCC warning event.
38	VDSTH	Analog In	V_{DS} monitoring threshold. Internal pull-down.
39	INH3/IN3	Digital In	Digital control signal for the high-side of the phase 3 or control of the OUT3 voltage level. Internal pull-down.
40	INH2/IN2	Digital In	Digital control signal for the high-side of the phase 2 or control of the OUT2 voltage level. Internal pull-down.
41	INH1/IN1	Digital In	Digital control signal for the high-side of the phase 1 or control of the OUT1 voltage level. Internal pull-down.
42	INL3/EN3	Digital In	Digital control signal for the low-side of the phase 3 or enable of the half-bridge on OUT3. Internal pull-down.
43	INL2/EN2	Digital In	Digital control signal for the low-side of the phase 2 or enable of the half-bridge on OUT2. Internal pull-down.
44	INL1/EN1	Digital In	Digital control signal for the low-side of the phase 1 or enable of the half-bridge on OUT1. Internal pull-down.
45	nSTBY	Digital In	Digital control for the standby mode (active low). Internal pull-down.
46	LGC_CAP	Power	Pin for external bypass capacitor – internal logic supply stabilization (not intended for external supply purposes).
47	EN	Digital In	Drivers enable with “FAULT release” feature. Internal pull-down.
48	nFAULT	Digital Out	Open-drain pin to signal failure/protection events.
EPAD	GND	Power	Ground.

4.2 STDRIVE102H pin description

Figure 4. **STDRIVE102H pin description**

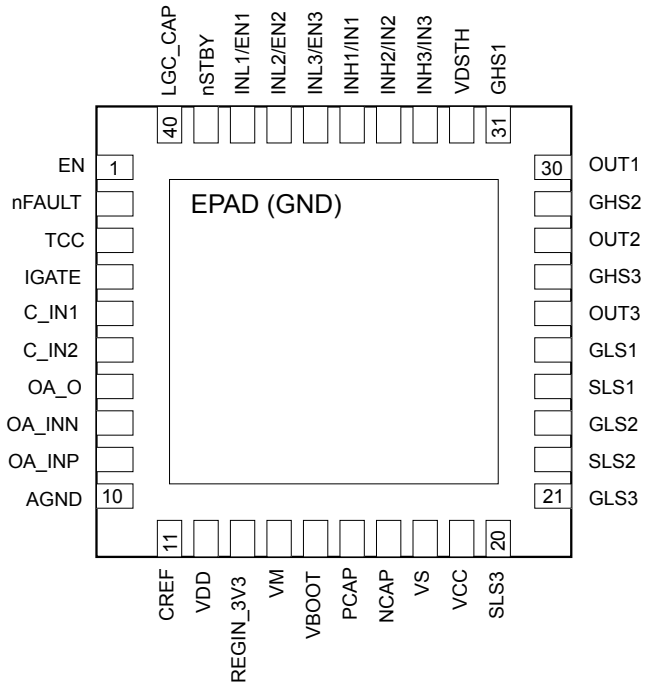


Table 8. **STDRIVE102H pin list**

Pin N.	Name	Type	Function
1	EN	Digital In	Drivers enable with “FAULT release” feature. Internal pull-down.
2	nFAULT	Digital Out	Open-drain pin to signal failure/protection events.
3	TCC	Analog In	Analog setting for the constant-current time (refer to Section 5.2.1).
4	IGATE	Analog In	Analog setting for the gate drivers current (refer to Section 5.2.1).
5	C_IN1	Analog In	Non-inverting input of the comparator 1.
6	C_IN2	Analog In	Non-inverting input of the comparator 2.
7	OA_O	Analog Out	Output of the op amp.
8	OA_INN	Analog In	Inverting input of the op amp.
9	OA_INP	Analog In	Non-inverting input of the op amp.
10	AGND	Power	Analog ground of the device. Connect this pin to EPAD or a suitable reference GND point.
11	CREF	Analog In	Common reference voltage for the two comparators (inverting input).
12	VDD	Power	3.3 V LDO linear regulator output and supply voltage of the Analog Front-End (AFE).
13	REGIN_3V3	Power	3.3 V LDO linear regulator input.
14	VM	Power	Motor supply voltage: reference for the internal charge pump and V_{DS} monitoring protection.
15	VBOOT	Power	Charge pump output voltage: high-side drivers supply.
16	PCAP	Power	Charge pump fly capacitor positive pin.
17	NCAP	Power	Charge pump fly capacitor negative pin.
18	VS	Power	Device power supply and 12 V LDO linear regulator input.
19	VCC	Power	12 V LDO linear regulator output and supply voltage of the low-side drivers

Pin N.	Name	Type	Function
20	SLS3	Analog	Phase 3 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 3).
21	GLS3	Analog	Phase 3 low-side driver output.
22	SLS2	Analog	Phase 2 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 2).
23	GLS2	Analog	Phase 2 low-side driver output.
24	SLS1	Analog	Phase 1 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 1).
25	GLS1	Analog	Phase 1 low-side driver output.
26	OUT3	Analog	Phase 3 high-side reference voltage (external half-bridge 3 output).
27	GHS3	Analog	Phase 3 high-side driver output.
28	OUT2	Analog	Phase 2 high-side reference voltage (external half-bridge 2 output).
29	GHS2	Analog	Phase 2 high-side driver output.
30	OUT1	Analog	Phase 1 high-side reference voltage (external half-bridge 1 output).
31	GHS1	Analog	Phase 1 high-side driver output.
32	VDSTH	Analog In	V_{DS} monitoring threshold. Internal pull-down.
33	INH3/IN3	Digital In	Digital control signal for the high-side of the phase 3 or control of the OUT3 voltage level. Internal pull-down.
34	INH2/IN2	Digital In	Digital control signal for the high-side of the phase 2 or control of the OUT2 voltage level. Internal pull-down.
35	INH1/IN1	Digital In	Digital control signal for the high-side of the phase 1 or control of the OUT1 voltage level. Internal pull-down.
36	INL3/EN3	Digital In	Digital control signal for the low-side of the phase 3 or enable of the half-bridge on OUT3. Internal pull-down.
37	INL2/EN2	Digital In	Digital control signal for the low-side of the phase 2 or enable of the half-bridge on OUT2. Internal pull-down.
38	INL1/EN1	Digital In	Digital control signal for the low-side of the phase 1 or enable of the half-bridge on OUT1. Internal pull-down.
39	nSTBY	Digital In	Digital control for the standby mode (active low). Internal pull-down.
40	LGC_CAP	Power	Pin for external bypass capacitor – internal logic supply stabilization (not intended for external supply purposes).
EPAD	GND	Power	Ground.

5 Device description

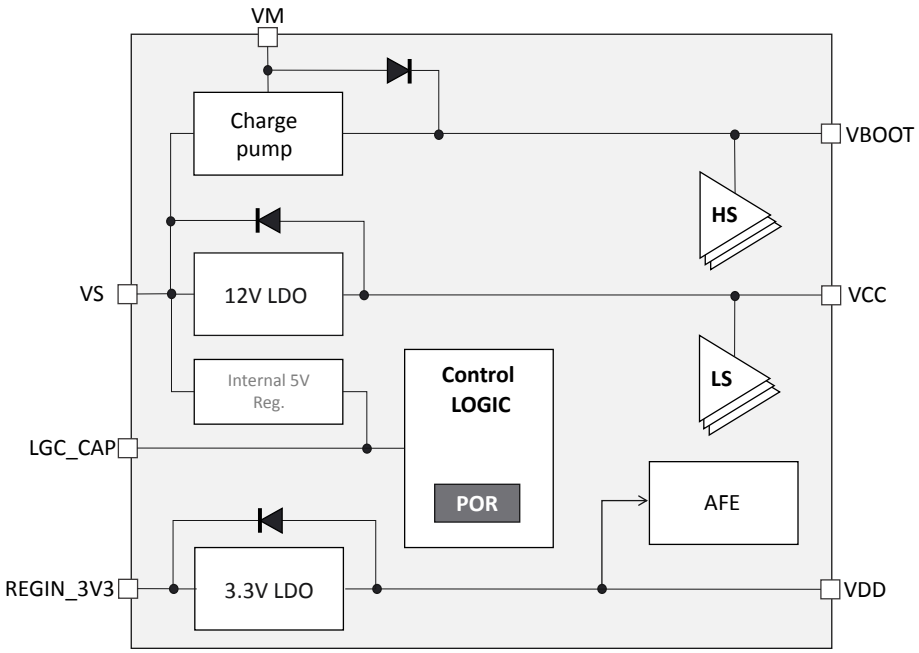
The STDRIVE102BH and the STDRIVE102H are triple half-bridge gate drivers suitable for 3-phase brushless motor driving. From now on the naming convention STDRIVE102BH/H is adopted to indicate indistinctly one or the other.

5.1 Power management section

The power management section of the STDRIVE102BH/H (Figure 5) is composed by:

- One LDO linear regulator with 12 V output; it is used to generate the VCC for the gate drivers' supply. Its input VS can be connected to VM or to an external voltage (up to 50 V operative).
- One LDO linear regulator, which generates the 3.3 V supply (VDD). Its input REGIN_3V3 ranges between 3.6 V and 15 V. It can also be connected to the VCC or be fed by an external supply.
- One internal regulator, which supplies the STDRIVE102BH/H control logic at 5 V. This voltage is for internal use only: no external load or circuitry can be connected to the LGC_CAP pin, which must be used only to connect an external decoupling capacitor (low-ESR ceramic, 4.7 µF / 16 V). This capacitor stabilizes all the internal control circuits, including the power-on reset (POR).
- A charge pump, supplied by VS and referenced to VM, which generates the VBOOT supply rail for the high side gate drivers.

Figure 5. Power management block diagram

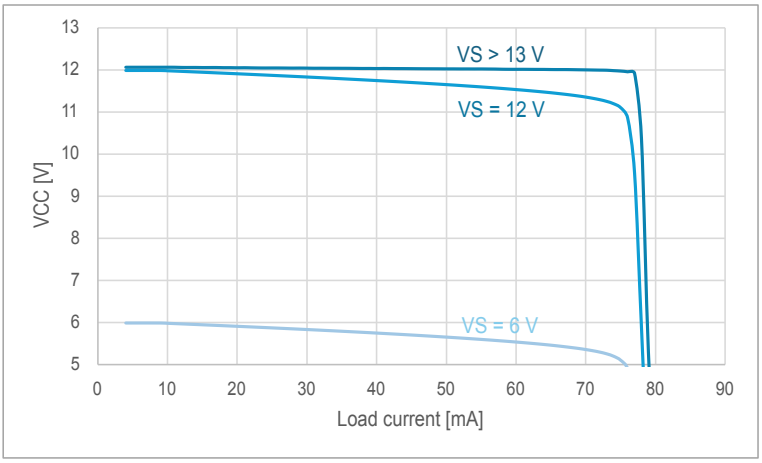


5.1.1 12 V LDO linear regulator

This regulator generates the voltage on the VCC pin, which is the supply of the low-side gate drivers and the set point for the 'V_{BOOT} - V_M' voltage provided by the charge pump (refer to Section 5.1.3). A low ESR ceramic capacitor of 4.7 µF, 25 V must be placed as close as possible to the VCC pin, to ensure the stability of the V_{CC} and support the currents required by the low-side gate drivers.

In addition, external loads can be connected to VCC pin, taking care to stay within the operating range. The output current of the regulator is limited at $I_{CC,lim}$ protecting it against short circuit and overload. The overall consumption of the external loads plus the drivers must be smaller than this current limitation.

Figure 6. 12 V LDO output according to the current load at different VS input



The linear regulator input is connected to the main supply VS. The regulator can be bypassed by connecting the VCC and the VS together and forcing an external voltage equal to the target VCC value, which must be in any case within the operative range of the VCC pin.

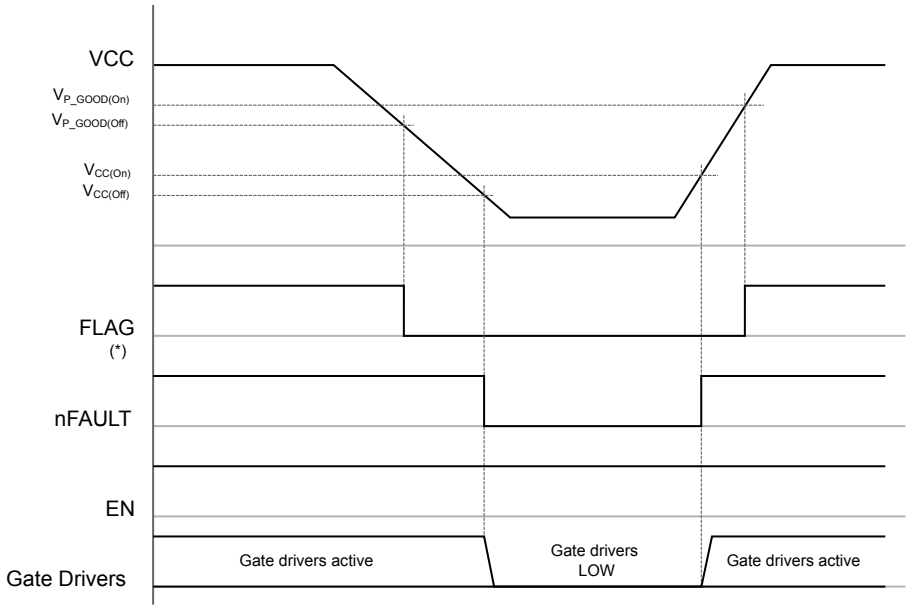
The regulator is disabled in standby mode in order to reduce the current consumption.

In case the VCC voltage falls below the UVLO threshold ($V_{CC(Off)}$), the gate drivers turn off all the external MOSFETs, forcing the power stage into a safe condition. Concurrently, the nFAULT open-drain pin is forced low to signal that the UVLO protection has been triggered. As soon as the VCC voltage rises above the $V_{CC(On)}$ threshold, the nFAULT is released and the drivers return to an active condition, according to the status of the digital inputs.

In the STDRIVE102BH only when the VCC voltage falls below the “power-good” threshold ($V_{P\_GOOD(Off)}$), the FLAG open-drain pin is forced low, but there are no other effects on the functional blocks of the devices. The FLAG pin is then released as soon as the VCC voltage rises above the $V_{P\_GOOD(On)}$ threshold.

An example of the V_{CC} thresholds management is shown in Figure 7.

Figure 7. V_{CC} thresholds (power-good and UVLO)



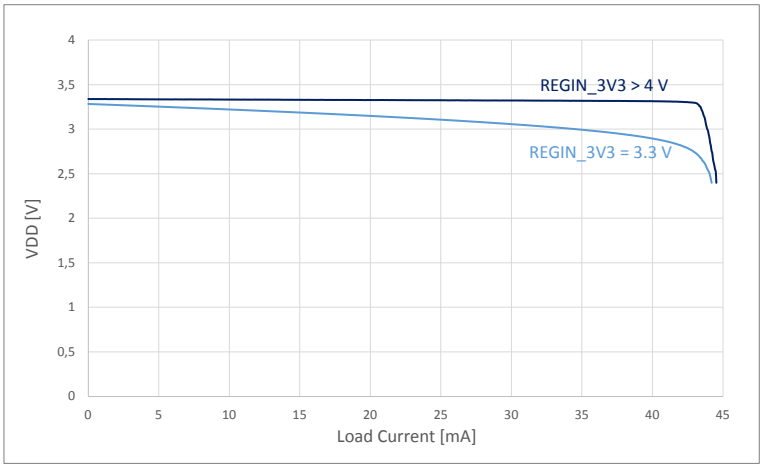
Note: (*) The FLAG pin is available only in the STDRIVE102BH.

5.1.2 3.3 V LDO linear regulator

The device integrates a 3.3 V regulator, which supplies the embedded analog front-end (AFE). In addition, external loads can be connected to the VDD pin, taking care to stay within the operating range. It is recommended to place a low ESR ceramic capacitor of 4.7 µF 16 V as close as possible to the VDD pin, to guarantee the stability of the VDD voltage.

The output current of the regulator is limited at $I_{DD,lim}$, protecting it against short-circuit and overload. The overall consumption of the external loads plus the AFE must be smaller than this current limitation.

Figure 8. 3.3 V LDO output according to the current load at different REGIN_3V3 input



The regulator is disabled in standby mode in order to reduce the current consumption.

The regulator can be bypassed by connecting the VDD and the REGIN_3V3 pins together and forcing externally a voltage equal to the target VDD value, and in any case within the operative range of the VDD pin.

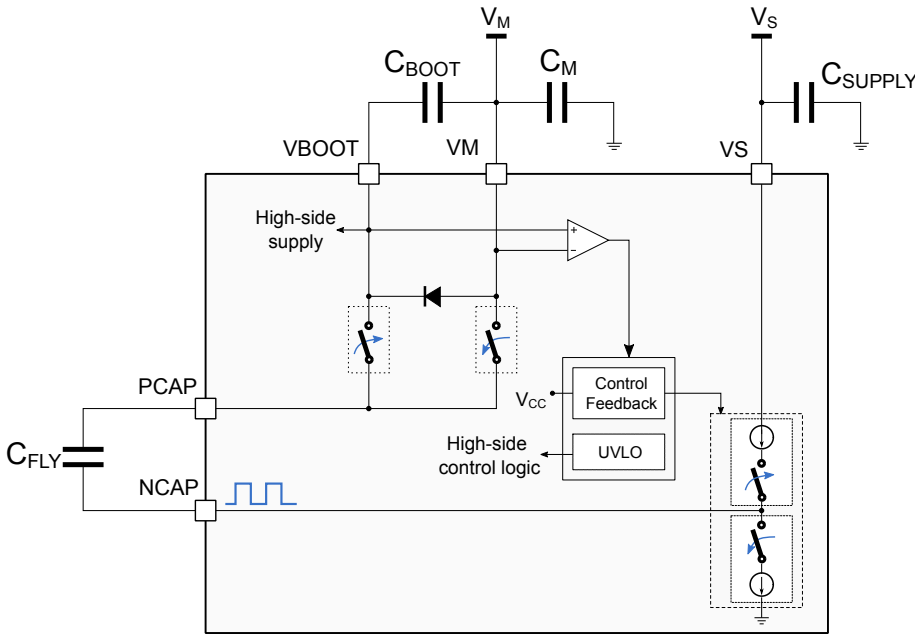
The 3.3 V regulator has a dedicated UVLO protection. The UVLO helps to avoid unexpected behavior related to all the circuitries supplied by the VDD, in particular it avoids spurious events coming from the AFE comparators and unstable sampling of the TCC and/or IGATE pins.

In case of UVLO condition (VDD falls below the $V_{DD(off)}$ threshold), the drivers turn off all the external MOSFETs, forcing the power stage into a safe condition. Concurrently, the nFAULT open-drain pin is forced low. As soon as the VDD voltage rises above the $V_{DD(On)}$ threshold, the nFAULT is released and the drivers return to an active condition, depending on the status of the digital inputs.

5.1.3 Charge pump

The embedded charge pump supplies the high-side gate drivers and ensures an unlimited on-time of the high-side MOSFETs and a PWM duty cycle of 100%.

Figure 9. Charge pump simplified block diagram



The charge pump is supplied directly by the VS pin and generates the voltage V_{BOOT} referenced to the motor supply V_M. The V_{BOOT} is the supply of the three high-side gate drivers and it must be greater than V_M to properly turn on the high-side MOSFETs. The internal feedback circuit of the charge pump tracks the value of the voltage on the VCC pin and regulates the V_{BOOT} to be equal to 'V_M + V_{CC}'. In this way, both the low-side and the high-side MOSFETs are driven with the same V_{GS}, thus ensuring a more balanced behavior of the power stage.

The circuit on the NCAP pin charges the capacitor C_{FLY}; the charge is then transferred to the C_{BOOT} capacitor through the PCAP pin. The amount of charge stored in the C_{FLY} capacitor is controlled by the internal feedback, in order to meet the target voltage on VBOOT pin.

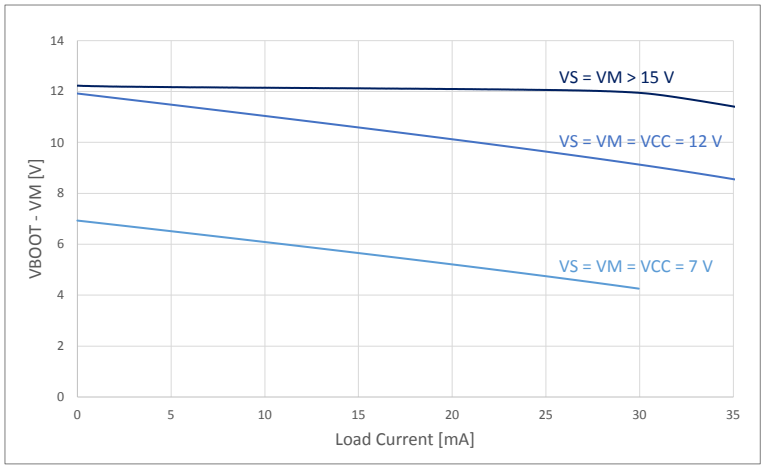
The drop between the target value of V_{BOOT} and its actual value depends on the voltage on the VS pin and the average load current required by the high-side drivers. The drop increases for lower V_S and higher current load. Figure 10 shows the charge pump output voltage with respect to the load current at T_{amb} = 25 °C, using the recommended values for C_{FLY} = 220 nF and C_{BOOT} = 1 µF.

The pulsed current required by the high-side drivers is provided by the C_{BOOT} capacitor. This capacitor should be sized according to the maximum allowed ripple and total gate charge of the external MOSFETs. A ceramic low ESR capacitor of the same value of C_{BOOT} must be placed close to the VM pin and the exposed pad (GND) of the STDRIVE102BH/H.

The high-side drivers are connected to VBOOT by an internal connection: for no reason can other external loads be connected to the VBOOT pin. The VBOOT pin is referred to the VM pin: any external event forcing a 'V_{BOOT} - V_M' voltage below the limit reported in Table 1. Absolute maximum ratings, results in the device breakdown.

In case of undervoltage ('V_{BOOT} - V_M ' < $V_{CPump(Off)}$), the UVLO protection turns off the high-side MOSFETs, while the low-side drivers keep on operating. The high-side drivers return operative when 'V_{BOOT} - V_M' > $V_{CPump(On)}$.

Figure 10. **Charge pump output voltage with respect to the load current**



5.2 Gate drivers

The gate drivers use a constant-current approach enabling the following advantages:

- No external components are required between the MOSFETs' gates and the drivers.
- The slew rate of the half-bridge outputs is better controlled.

The high-side drivers (Figure 11) and the low-side drivers (Figure 12) have a similar structure:

- A reference pin for the low level (OUTx for the high-side and SLSx for the low-side).
- The output pin (GHSx for the high-side or GLSx for the low-side), which directly drives the external MOSFET's gate.
- The supply pin (VBOOT in common to the three high side drivers and VCC in common to the three low side drivers).

When the driver is not operative (for example, in standby mode or for very low supply), an equivalent 100 kΩ resistor keeps the external MOSFETs off. In normal conditions, the gate driver must force a voltage on the gate of its respective MOSFET, in order to keep it in a well-defined state. This datasheet adopts the following definitions:

- Setting HIGH the gate driver means that the driver sources a controlled current to increase the V_{GS} of the MOSFET and turn it on. The gate current comes from the supply VCC in case of the low-side driver or from VBOOT in case of the high-side driver.
- Setting LOW the gate driver means that the driver sinks a controlled current from the gate of the MOSFET to turn it off. The sink circuitry of the driver is referred to the OUTx pin for the high-side, and to the SLSx pin for the low-side. This approach ensures that the MOSFET is kept off, even in the presence of below-GND transients.

In normal mode operation, when a high-side driver is set HIGH, the voltage on the GHSx pin increases up to its target level V_{BOOT} . At the same time the OUTx voltage increases up to V_M, so that the V_{GS} of the external MOSFET is kept under control (less or equal to V_{CC}). In case the OUTx pin cannot follow the GHSx pin, the gate driver protects the gate of the external MOSFET from breakdown clamping the V_{GS} at $V_{GS,\ clamp}$.

The six gate drivers (three low-side and three high-side) are controlled by six digital inputs, INH1/IN1, INH2/IN2, INH3/IN3, INL1/EN1, INL2/EN2, INL3/EN3. Each digital input has an internal pull-down resistor $R_{PD,in}$. Each half-bridge (driven by a low-side driver and a high-side driver) is controlled by a couple of inputs: for example, INH1/IN1 and INL1/EN1 refer to half-bridge 1. The label INHx/INx or INLx/ENx can be used to indicate one of the three half-bridges, with no specific reference to a particular channel. Note that the terms "channel" or "phase" could be used similarly to refer to the half-bridge output.

The STDRIVE102BH/H implements two control modes: the enable/input mode (EN/IN) or the direct mode (INH/INL), respectively explained in Section 5.2.1.1 and Section 5.2.1.2. The digital inputs assume a different function according to the input mode selected:

- In case the device is configured in Enable/Input mode:
  - INHx/INx → INx
  - INLx/ENx → ENx
- In case the device is configured in Direct mode:
  - INHx/INx → INHx
  - INLx/ENx → INLx

In addition to the six digital inputs mentioned above, another digital input named EN (pin 47 for the STDRIVE102BH and pin 1 for the STDRIVE102H) is used as general enable: in case it is forced to 0, all the six gate drivers are set LOW, turning off all the external power MOSFETs. Setting EN to 1 activates the gate drivers, which behave according to their related digital inputs. The EN pin also integrates an analog threshold $V_{release}$, to release the latched condition after a FAULT event (refer to Section 5.6.1).

Figure 11. High-side driver simplified block diagram

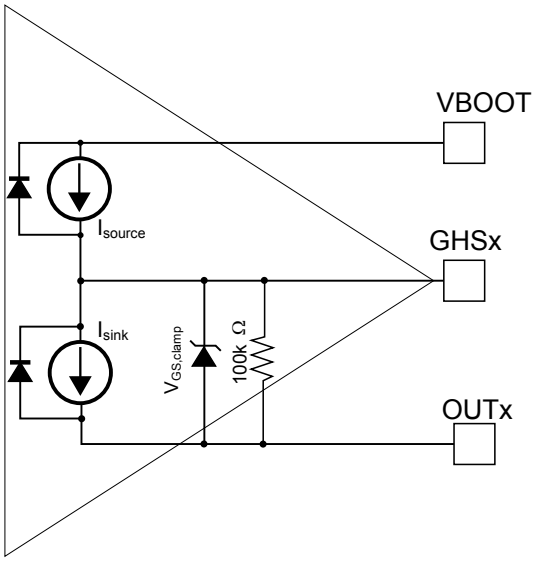
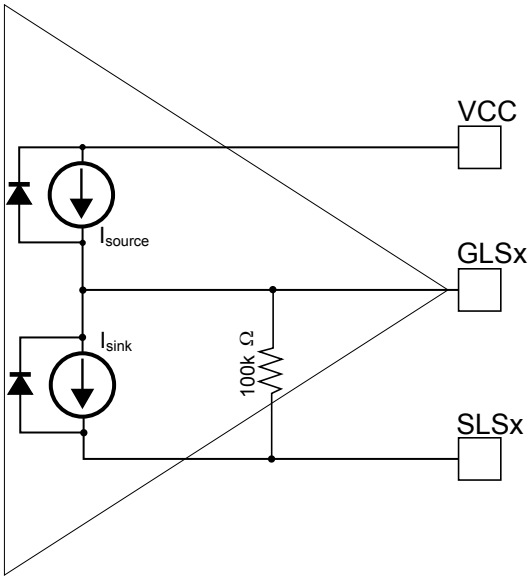


Figure 12. Low-side driver simplified block diagram



5.2.1 Driving current management

The gate driver turns on the respective MOSFET by sourcing the programmed current $I_{GATE,on}$ for a time equal to the programmed $t_{cc,on}$ time. After this time, the MOSFET's gate should be completely charged, so the driver reduces the source current to a holding value $I_{hold,on}$.

The gate driver turns off the respective MOSFET by sinking the programmed current $I_{GATE,off}$ for a time equal to the programmed $t_{cc,off}$ time. After this time, the MOSFET's gate should be completely discharged, so the driver reduces the sink current to a holding value $I_{hold,off}$.

To avoid induced turn-on effects, during the turn-on phase of a MOSFET (that is, when a driver is forcing $I_{GATE,on}$) the complementary driver sinks the maximum available current I_{clamp} for the entire $t_{cc,on}$ duration.

Note that the current capability is the maximum current that the driver is able to source/sink: when the gate of the external MOSFET is completely charged/discharged the driver is no longer able to source/sink current.

The current levels can be summarized as below:

- The value of the source current and the sink current is set by the analog voltage on IGATE input (see Table 9).
- The $I_{hold,on}$ current is 25 mA typical value.
- The $I_{hold,off}$ current is 50 mA typical value.
- The I_{clamp} current is 2140 mA typical value.

Table 9. Programmable gate current typical values

IGATE level refer to Table 11	$I_{GATE,on}$ (source) [mA]	$I_{GATE,off}$ (sink) [mA]
0 (GND)	25	50
1	75	150
2	150	300
3	250	500
4	300	600
5	350	700
6	400	800
7	500	1000
8	550	1100
9	600	1200
10	650	1300
11	700	1400
12	800	1600
13	850	1700
14	900	1800
15 (VDD)	1000	2000

The turn-on and turn-off timings (respectively $t_{cc,on}$ and a $t_{cc,off}$) are set by the voltage on TCC input (see Table 10).

Moreover, the input mode and the deglitch filter time of the V_{DS} monitoring protection ($t_{dg(VDS)}$) are adjusted according to the configuration of the TCC (see Section 5.2.3).

Table 10. Programmable constant-current time (TCC) typical values

TCC level refer to Table 11	Input mode	$t_{cc,on}$ [ns]	$t_{cc,off}$ [ns]	$t_{dg[VDS]}$ [µs]
0 (GND)	INH/INL mode (refer to Section 5.2.1.2)	2240	1120	3.5
1	EN/IN mode (refer to Section 5.2.1.1)	280	140	3.5
2		560	280	3.5
3		840	420	3.5
4		1120	560	3.5
5		1400	700	3.5
6		1680	840	3.5
7		1960	980	3.5
8		2240	1120	3.5
9		2520	1260	4.5
10		2800	1400	4.5
11		3080	1540	4.5
12		3360	1680	6
13		3800	1900	6
14		4400	2200	7
15 (VDD)		4800	2400	7

The IGATE level and the TCC level reported in Table 9 and in Table 10 refer to an analog voltage that is a fraction of V_{DD}. Therefore, the selected level on the pins can be configured by two resistor dividers, one for IGATE and one for TCC.

Figure 13. TCC and IGATE level selection example

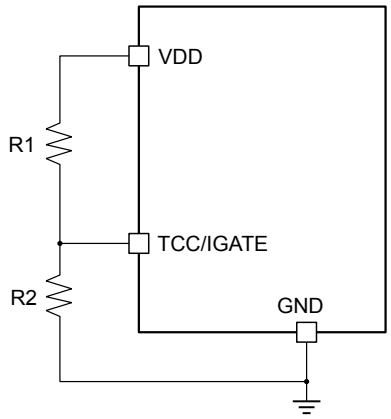


Table 11 summarizes the V_{DD} ratio for each level and a suggested pair of standard resistor values suitable for each configuration, the R1 and R2 resistors are defined as shown in Figure 13.

Table 11. Analog levels for TCC and IGATE pins and suggested resistor divider

ADC level	VDD ratio	R1 suggested value	R2 suggested value
0	GND	No resistor	0 (short to GND)
1	1/15 V_{DD}	105 kΩ	7.5 kΩ
2	2/15 V_{DD}	130 kΩ	20 kΩ
3	3/15 V_{DD}	30 kΩ	7.5 kΩ
4	4/15 V_{DD}	33 kΩ	12 kΩ
5	5/15 V_{DD}	30 kΩ	15 kΩ
6	6/15 V_{DD}	33 kΩ	22 kΩ
7	7/15 V_{DD}	34 kΩ	30 kΩ
8	8/15 V_{DD}	30 kΩ	34 kΩ
9	9/15 V_{DD}	22 kΩ	33 kΩ
10	10/15 V_{DD}	15 kΩ	30 kΩ
11	11/15 V_{DD}	12 kΩ	33 kΩ
12	12/15 V_{DD}	7.5 kΩ	30 kΩ
13	13/15 V_{DD}	20 kΩ	130 kΩ
14	14/15 V_{DD}	7.5 kΩ	105 kΩ
15	V_{DD}	0 (short to V_{DD})	No resistor

5.2.1.1 *Enable/input mode (EN/IN)*

When enable/input mode is selected, the six digital inputs are managed as described in Table 12, where x = 1, 2, 3 refers to the half-bridge driven, the digital input INHx/INx is simply indicated as INx and INLx/ENx as ENx. The half-bridge x is enabled by setting ENx = 1, otherwise when ENx = 0 the half-bridge is left in high impedance. When enabled, the half-bridge status is determined by the INx input: INx = 0 sets the state low (OUTx at GND), INx = 1 sets the state high (OUTx = VM). The general EN pin is also reported in Table 12.

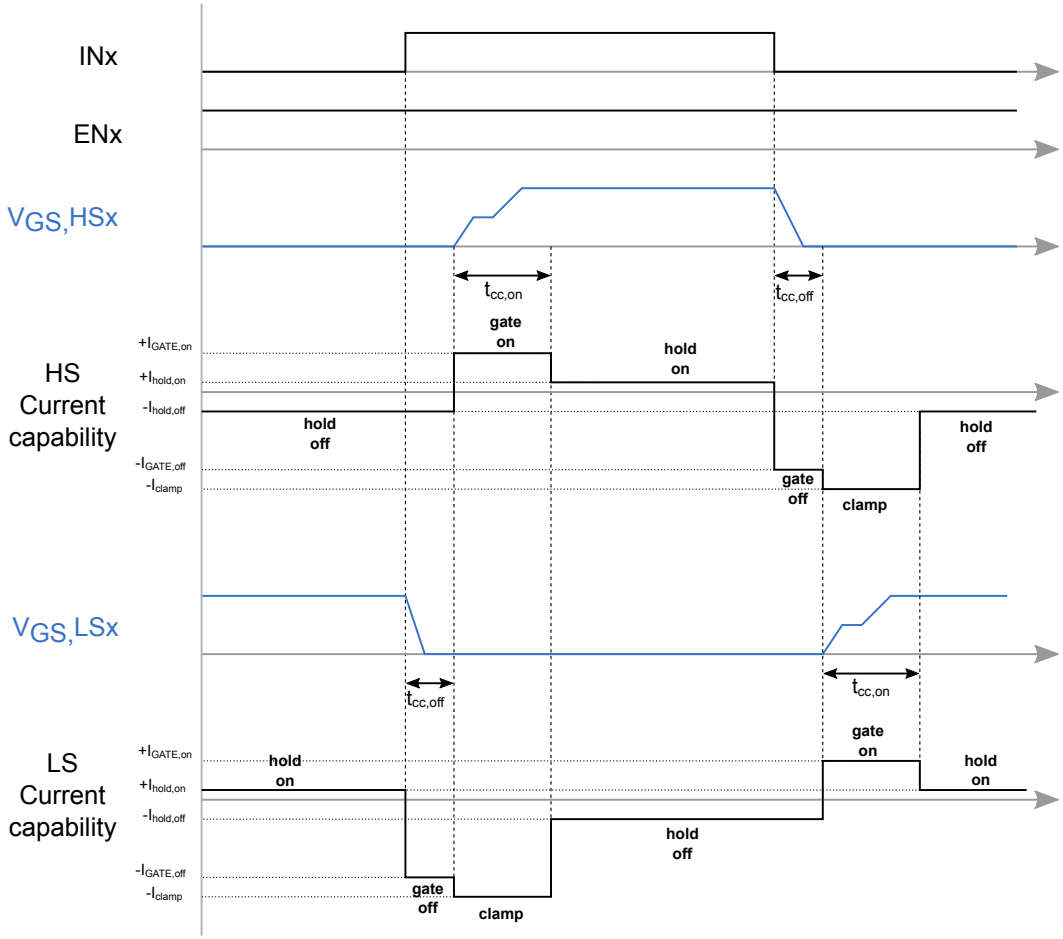
Table 12. Truth table for the enable/input mode

EN	ENx	INx	GLSx	GHSx	OUTx Half-bridge status
0	Do not care	Do not care	All GLSx sink current All drivers' status LOW All the low-side MOSFETs OFF	All GHSx sink current All drivers' status LOW All the high-side MOSFETs OFF	All three phases are in high impedance
1	0	Do not care	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx in high impedance
1	1	0	GLSx source current Driver *x* status HIGH Low-side MOSFET *x* ON	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx at GND
1	1	1	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx source current Driver *x* status HIGH High-side MOSFET *x* ON	OUTx at VM

When INx is toggled, the logic changes the state of both the high-side x and the low-side x with a specific sequence: the driver that is currently HIGH is set LOW; then, after a deadtime, the complementary driver is set HIGH.

The deadtime is necessary to avoid dangerous cross-conductions. The deadtime is managed by the internal logic, according to the device's setting. Since the time required to completely discharge the gate of the external MOSFET is $t_{cc,off}$, it is also equivalent to the deadtime (Figure 14).

Figure 14. Current management using EN/IN mode



The current and the timing of the driver are strictly related: they must be configured by the user through the TCC and IGATE pins, according to the external power MOSFET and the slew rate required by the application.

The IGATE level must be chosen according to Table 9 and considering the gate-drain charge Q_{gd} of the driven MOSFET and the rising time/fall time and thus the slew rate of the OUTx pin of the half-bridge.

Equation 1

$$I_{GATE,on/off} \cong \frac{Q_{gd}}{t_{sw}} \quad (1)$$

The current to be considered, whether $I_{GATE,on}$ or $I_{GATE,off}$ depends on which MOSFET of the half-bridge is hard-switching. Eq. (1) provides an indication to select a suitable driving current for the application; however, it must be considered that C_{gd} varies with the V_{DS} of the MOSFET, therefore some margins must be taken.

The t_{sw} in Eq. (1) represents the switching time of the half-bridge OUTx and it is strictly related to the slew rate.

Equation 2

$$SR_{OUTx} \cong \frac{V_M}{t_{sw}} \quad (2)$$

For a given couple of values of $I_{GATE,on}$ or $I_{GATE,off}$ a couple of $t_{cc,on}$ and $t_{cc,off}$ can be selected among the values of Table 10. In this case the total gate charge $Q_{g,tot}$ of the external MOSFET must be considered, in order to ensure the complete charge/discharge of the gate within the t_{cc} time selected.

Equation 3

$$t_{cc,on} > \frac{Q_{G,tot}}{I_{GATE,on}} \quad , \quad t_{cc,off} > \frac{Q_{G,tot}}{I_{GATE,off}} \tag{3}$$

The condition reported in Eq. (3) allows to completely turn off one MOSFET before turning on the complementary one, thus leading to the insertion of an adequate deadtime and preventing the risk of cross conduction.

Since the $I_{GATE,on}$ is half of the $I_{GATE,off}$, the relation reported in Eq. (3) brings to a $t_{cc,on}$ that is twice the $t_{cc,off}$. For this reason, the STDRIVE102BH/H imposes this relation as shown in Table 10.

Section 5.2.1.3 shows a practical example on how to select IGATE and TCC settings, based on what is described in this section.

5.2.1.2 *Direct mode (INH/INL)*

In direct mode, each digital input is directly related to the state of each driver. The digital input INHx/INx (simply indicated as INHx) controls directly the high-side driver; the INLx/ENx (simply indicated as INLx) controls the low-side driver. High digital input implies the gate driver turns on the respective MOSFET; low digital input turns it off. The six digital inputs are managed as reported in Table 13, where x = 1, 2, 3 refers to the half-bridge driven.

As shown in Table 13, whenever INHx and INLx are set high together, both drivers turn off their respective MOSFET. This logic configuration is referred to as interlocking and it is implemented to prevent both the power MOSFETs of the same half-bridge from turning on together, avoiding any dangerous cross-conduction.

Table 13. Truth table for the direct mode

EN	INLx	INHx	GLSx	GHSx	OUTx Half-bridge status
0	Do not care	Do not care	All GLSx sink current All drivers' status LOW All the low-side MOSFETs OFF	All GHSx sink current All drivers' status LOW All the high-side MOSFETs OFF	All three phases are in high impedance
1	0	0	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx in high impedance
1	0	1	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx source current Driver *x* status HIGH High-side MOSFET *x* ON	OUTx at VM
1	1	0	GLSx source current Driver *x* status HIGH Low-side MOSFET *x* ON	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx at GND
1	1	1	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx in high impedance Interlocking

In direct mode, the driver timings are set to a fixed value $t_{cc,on}$ = 2240 ns and $t_{cc,off}$ = 1120 ns. These timings can ensure the complete charge or discharge of the gate for a wide range of external MOSFETs: referring to Equation 2, the maximum total gate charge supported by the drivers is 2240 nC.

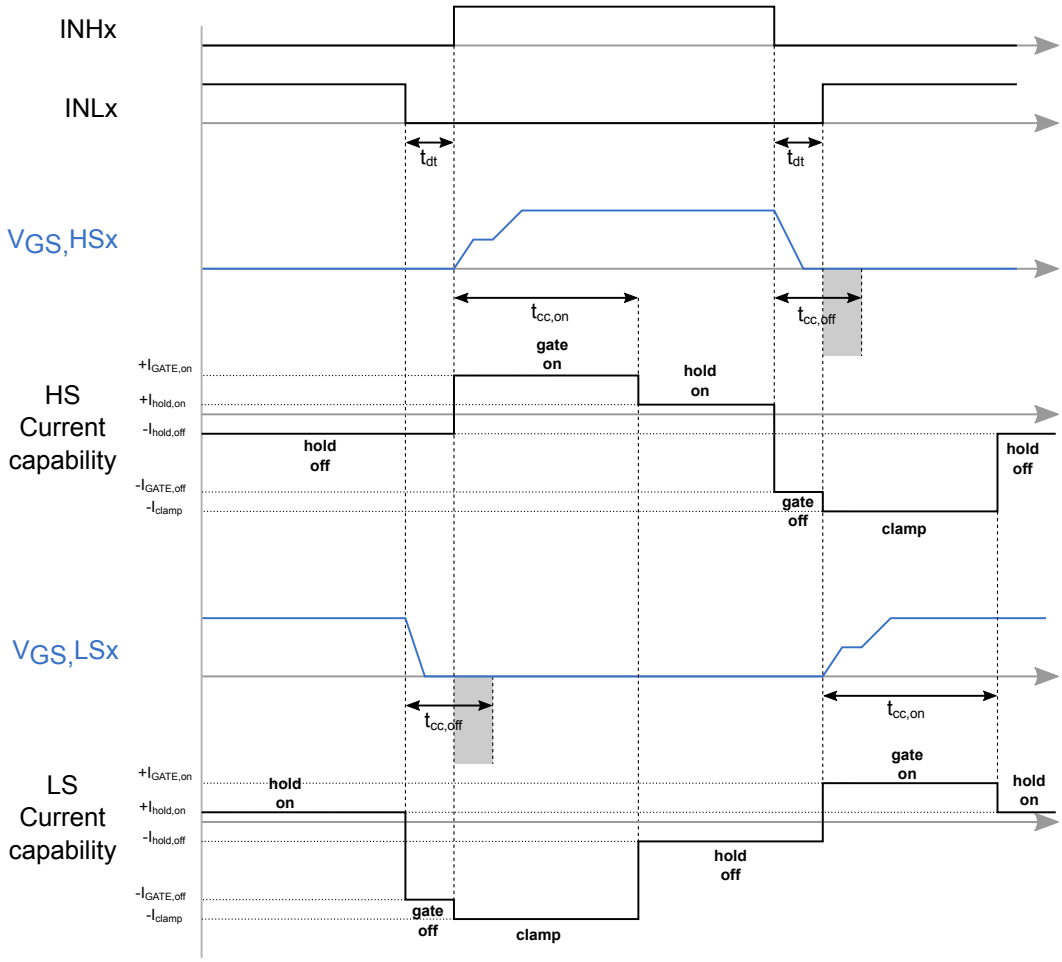
The deadtime between the turn-off of one driver and the turn-on of the complementary one is introduced by the user on the input signals INHx and INLx (Figure 15).

The direct mode implies that the turn-on of one driver occurs always before that the $t_{cc,off}$ of the complementary one is completed: the deadtime t_{DT} on the control signals must be chosen to be smaller than the $t_{cc,off}$ hence t_{DT} < 1120 ns. On the other hand, the user must select a proper deadtime, according to the total gate charge and the driving current configured in the driver. The deadtime t_{DT} must be chosen ensuring that the V_{GS} of the MOSFET that is turning off is equal to 0 V, before turning on the complementary MOSFET in the half-bridge. The criteria used should follow what has already been explained in Section 5.2.1.1, thus considering the total gate charge $Q_{G,tot}$ and the $I_{GATE,off}$ selected.

Equation 4

$$t_{DT} > \frac{Q_{G,tot}}{I_{GATE,off}} \quad (4)$$

Figure 15. Current management using direct mode INH/INL

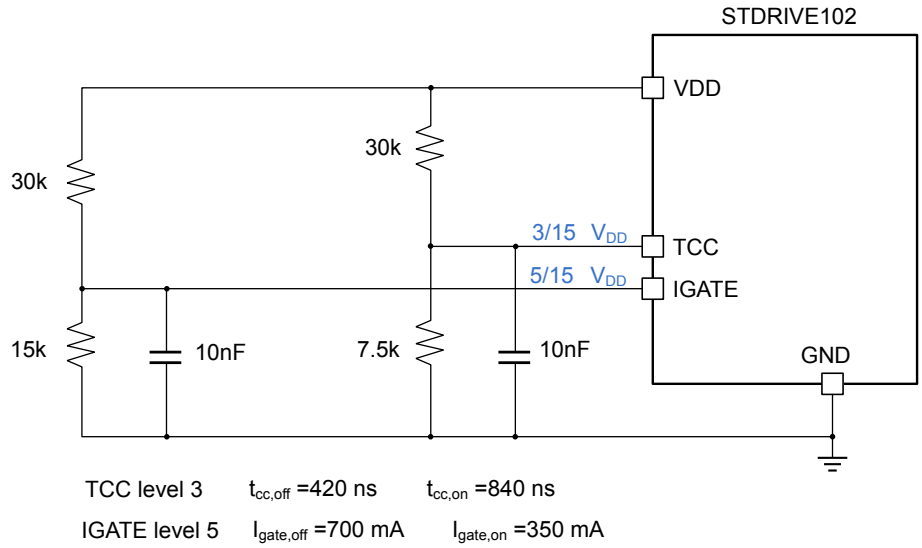


5.2.1.3 *TCC and IGATE configuration example*

Figure 16 shows an example of how to configure TCC and IGATE considering that each driver drives a target MOSFET with a total gate charge $Q_{G,tot}$ = 120 nC at 12 V of V_{GS}. Using $I_{gate,on}$ = 350 mA and $I_{gate,off}$ = 700 mA allows to complete the charge of the gate in less than 350 ns and a discharge in less than half of the time. Therefore, selecting a $t_{cc,off}$ = 420 ns and $t_{cc,on}$ = 840 ns provides enough margin for a safe operation of the power stage.

Using EN/IN mode allows the device to manage the deadtime that is 420 ns, equal to the $t_{cc,off}$. According to Table 9, Table 10, and Table 11 it is possible to select the resistors to be connected to the TCC and IGATE pins, as shown in Figure 16.

Figure 16. **Example of TCC and IGATE pin configuration**



An optional filter capacitor can be added to each pin in order to filter noise injection, which can alter the status of the configuration pins. The filter capacitor can be chosen as a trade-off between the filtering capability and the time required for stabilization at startup.

5.2.2 Propagation delays

The propagation delays between the edges of the digital inputs and the actuation of the gate drivers are represented in Figure 17, Figure 18, and Figure 19.

Figure 17. **Propagation delay in enable/input mode, ENx pin high**

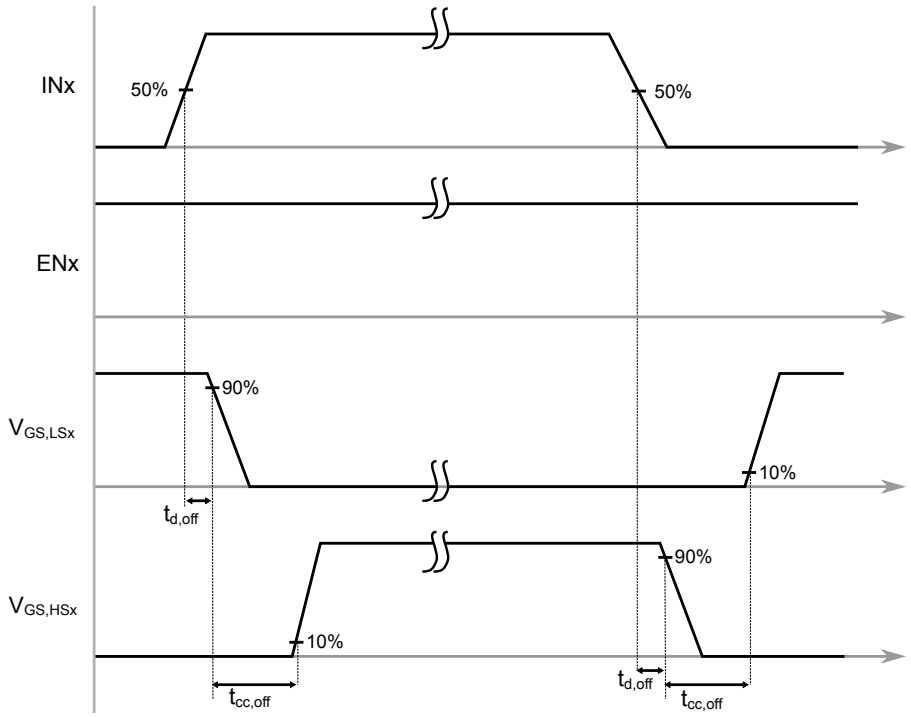


Figure 18. **Propagation delay in enable/input mode, ENx pin switching**

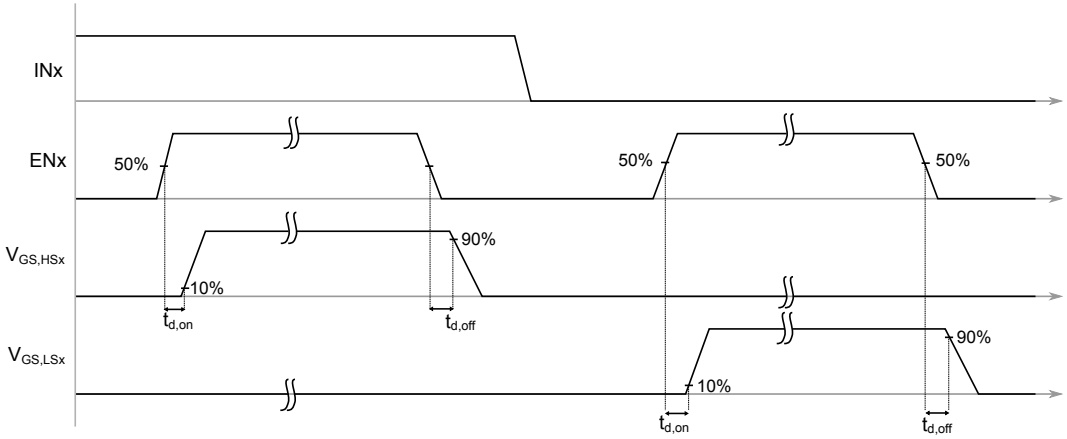
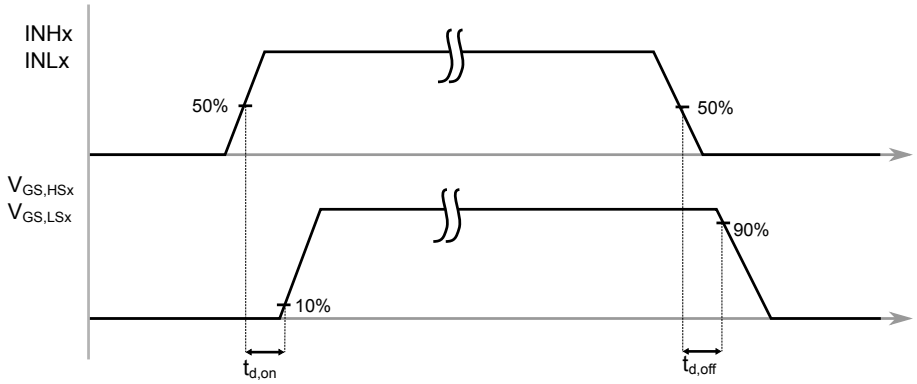


Figure 19. **Propagation delay in direct mode (INHx/INLx)**



5.2.3 V_{DS} monitoring

The STDRIVE102BH/H implements a monitoring of the drain-source voltage drop (V_{DS}) of each MOSFET. During all the time the MOSFET is on, it is expected that the V_{DS} keeps below a threshold, which depends on the $R_{DS,on}$ and the current flowing in the MOSEFT. If the V_{DS} exceeds the threshold value set on the VDSTH analog pin (refer to Figure 20), the device triggers a FAULT condition:

- The power stage is disabled: all the gate drivers are set LOW with the soft-off feature (see Section 5.4). This safe state is latched until a release request occurs (see below).
- The nFAULT pin is forced low.

To return in normal operation, the latched failure condition must be cleared in one of the following ways:

- Set the standby state by forcing the nSTBY pin low (refer to Section 5.8).
- Set the voltage on the EN pin lower than $V_{release}$ for at least $t_{EN,pulse\_rel}$ time.

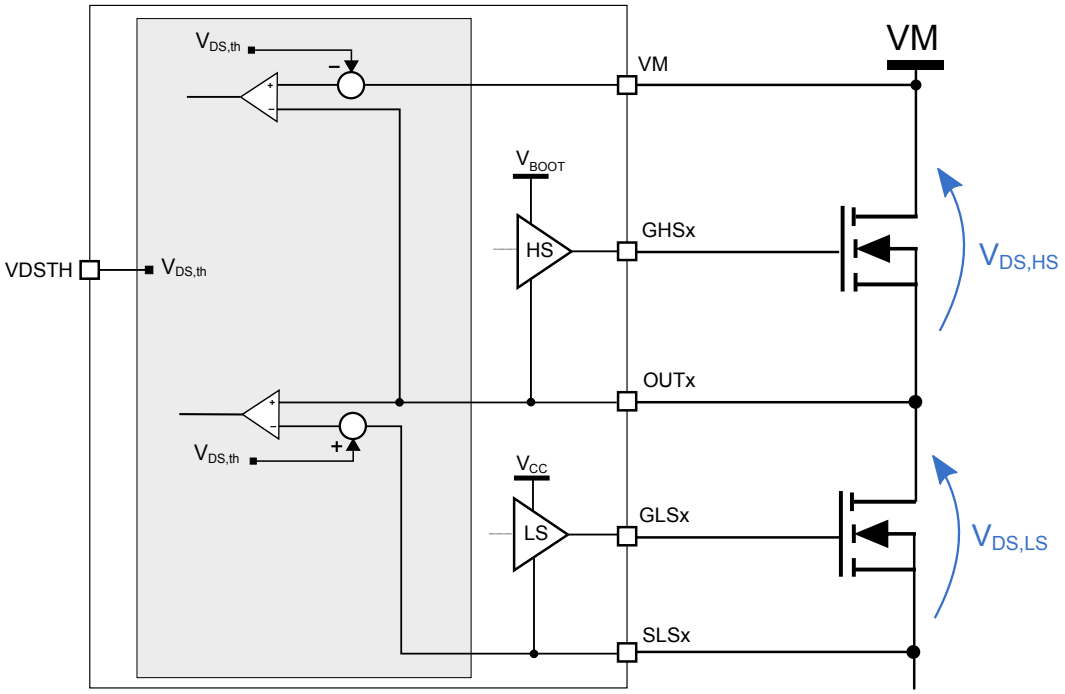
Note that the threshold voltage is an analog value, so it can be set to any value between the recommended ones.

The protection can be disabled setting a voltage on VDSTH pin higher than $V_{DSTH,dis}$.

To avoid unexpected triggering of the protection during the transients of the power stage, a deglitch filter is present. To trigger the protection, the V_{DS} must exceed the threshold for a time longer than the deglitch time $t_{dg(VDS)}$, which depends on the setting of the TCC pin (see Table 10).

Since the three high-side MOSFETs are supposed to be connected to the same supply V_M, the three different V_{DS} are monitored referring them to the same VM pin.

Figure 20. V_{DS} monitoring basic diagram



The V_{DS} monitoring protection can detect different failures related to the power stage:

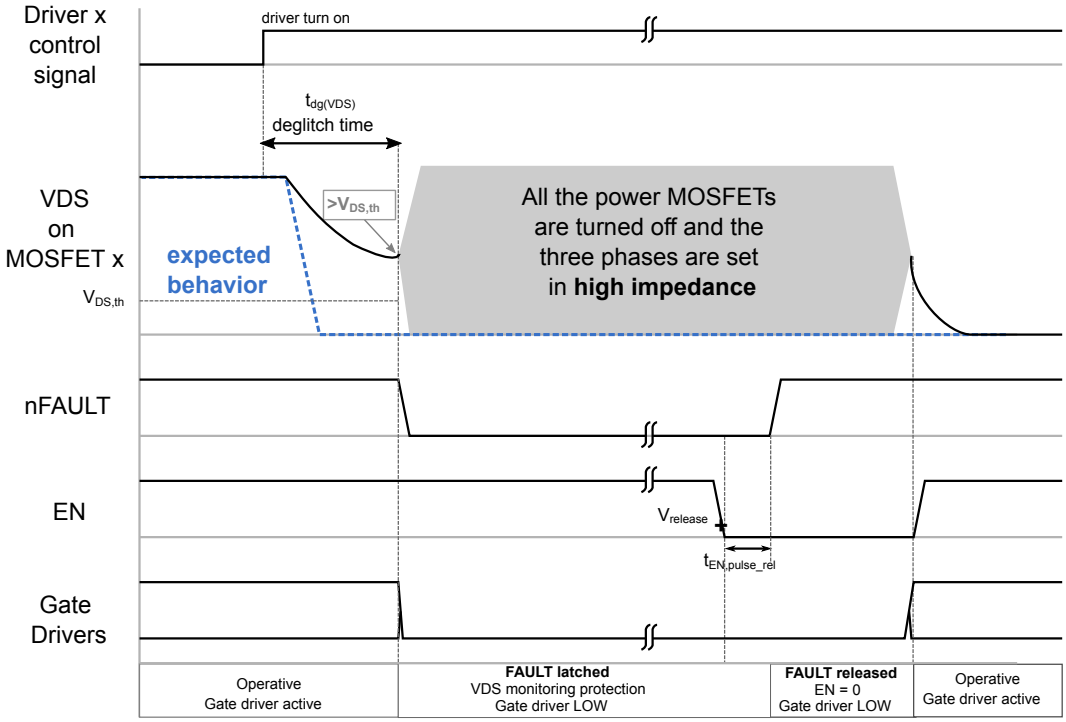
- Gate open. The gate connection is missing, or the gate is damaged.
- Gate short. The gate is damaged and there is a short between the gate and source.
- OUT short. The OUT pin can be shorted to another motor phase, to GND or to VM.

In all these cases, the MOSFET does not turn on and its V_{DS} does not fall below the expected threshold (set on the VDSTH pin).

In other cases, the MOSFETs turn on and work correctly, but unexpected behavior can be detected as well by the V_{DS} monitoring.

- Overload. In the case of current overload on the motor, the V_{DS} on the MOSFET can increase and become higher than the threshold. Moreover, the temperature increase due to higher current can also lead to an increase of the $R_{DS,on}$ of the MOSFET and thus a further increase of the V_{DS} measured.
- TCC/IGATE configuration: if the driver current $I_{GATE,on}$ or the time $t_{cc,on}$ are too small, the external MOSFET turns on too slowly or with higher $R_{DS,on}$ and its V_{DS} could not fall below the expected $V_{DS,th}$ threshold within the $t_{dg(VDS)}$ time.

Figure 21. **V_{DS} monitoring example**



The example in Figure 21 shows how the V_{DS} monitoring protection works. When the driver turns on, it is expected that the V_{DS} of the respective MOSFET falls below the threshold (as shown by the dotted line). In case the V_{DS} stays above the threshold $V_{DS,th}$ for a time longer than the deglitch time $t_{dg(VDS)}$, then the protection is triggered.

The V_{DS} monitoring protection stays latched until it is released, forcing the EN pin below the $V_{release}$ voltage for a time longer than $t_{EN,pulse\_rel}$. The drivers are enabled again when the EN pin goes high.

5.3 Analog Front-End (AFE)

The STDRIVE102BH integrates three operational amplifiers and three comparators (Figure 22), while the STDRIVE102H integrates one operational amplifier and two comparators (Figure 23).

Figure 22. **STDRIVE102BH AFE block diagram**

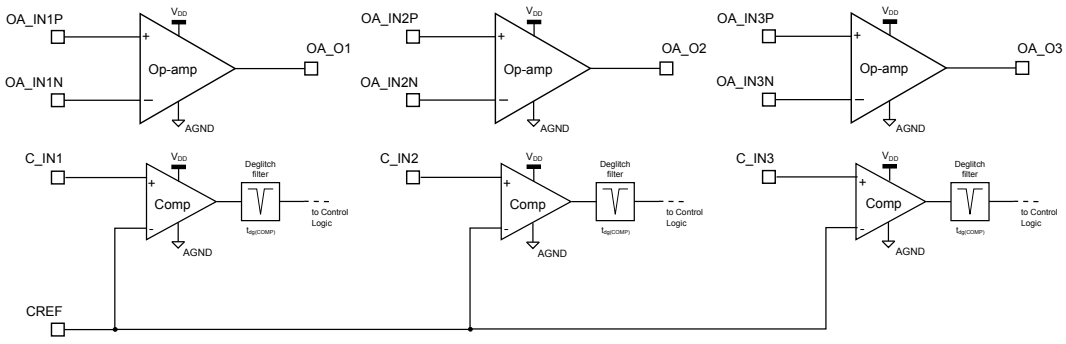
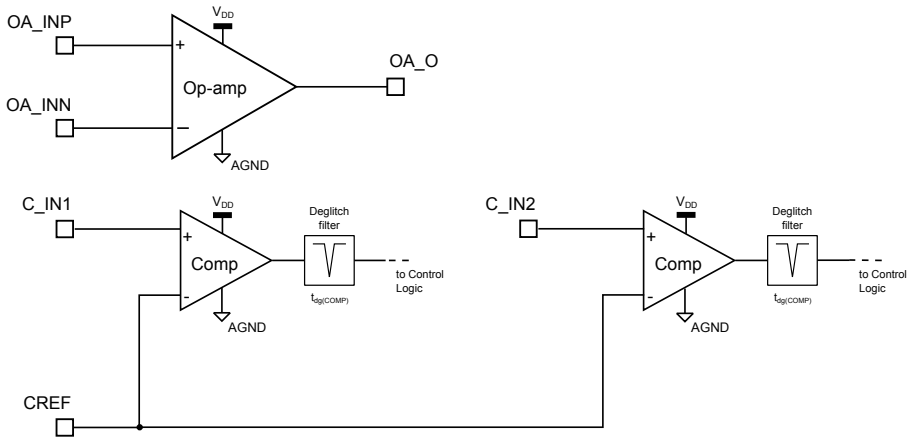


Figure 23. **STDRIVE102H AFE block diagram**

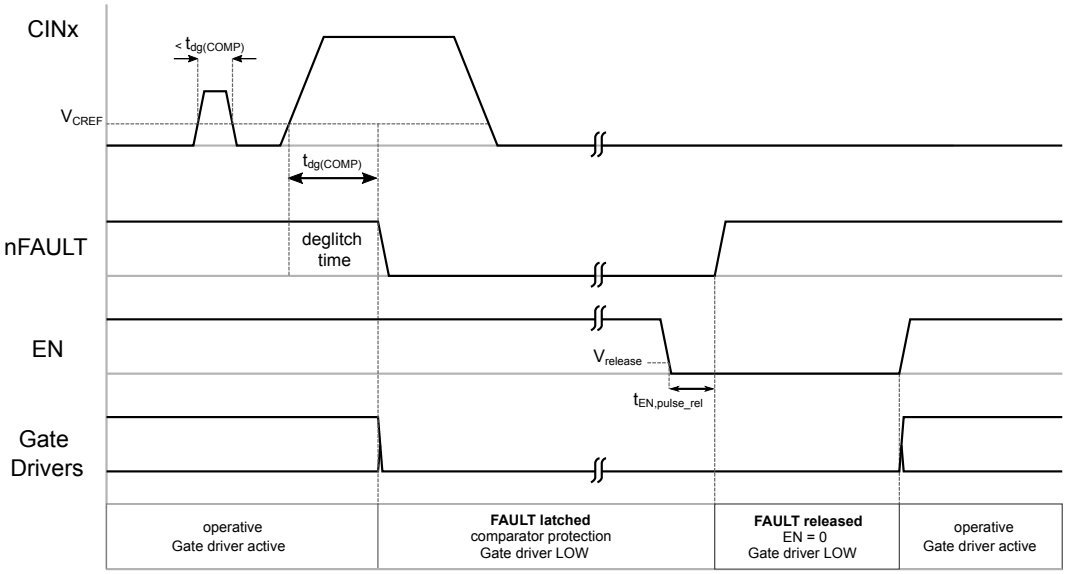


The operational amplifiers are unity-gain stable for load capacitors up to 100 pF and have a low input bias current. They provide a rail-to-rail input and output operation, a wide bandwidth, and a fast recovery of the output after saturation. The operational amplifiers are totally uncommitted, so they can be used as general-purpose components within their operative range (between 0 V and V_{DD}). As an example of typical configuration, the operational amplifiers can be used to amplify the voltage drop across the shunt resistors placed on the low-side half-bridge, in order to implement a current sense on each phase. Therefore, the STDRIVE102BH is suitable for triple shunt applications, while the STDRIVE102H is suitable for single shunt applications.

The comparators in the AFE, three in the STDRIVE102BH and two in the STDRIVE102H, have a single CREF pin, in common to all the negative inputs as shown in Figure 22 and Figure 23. The positive input of each comparator has a dedicated pin (C_INx). As an example of typical configuration, the comparators can be used to implement an overcurrent protection, an overvoltage protection or an overtemperature protection for the application, in case an external temperature sensor is present in the application.

When the voltage on the positive input of one comparator (C_INx) exceeds the voltage on CREF for a time longer than the deglitch time ($t_{dg(COMP)}$), the comparator's output triggers the protection circuitry and raises a FAULT event, which forces the nFAULT pin low. At the same time, the power stage is disabled turning off all the external MOSFETs with the soft-off feature (see Section 5.4). The FAULT condition triggered by the comparators is latched: the normal operation is restored bringing the EN pin below the $V_{release}$ threshold for a time longer than $t_{EN,pulse\_rel}$ (refer to Figure 24).

Figure 24. **AFE comparator example**



The AFE is supplied by the VDD pin (internally connected) and it is referred to the AGND pin, to improve immunity against ground noise.

The current consumption of the operational amplifiers slightly depends on the voltage of its output stage (V_{OA_Ox}): the consumption is maximum when the output is in the middle of its operating range ($V_{DD}/2$), and is minimum when the output is saturated (V_{OA_Ox} = GND or V_{OA_Ox} = V_{DD}).

The overall current consumption of the AFE is part of the overall current availability of the 3.3 V internal LDO (I_{DD}), when using external loads connected to VDD.

5.4 Soft turn-off

When the V_{DS} monitoring protection or the AFE comparators are triggered, it could indicate a severe overcurrent event on the power stage (for example, short-circuit). In this case, the soft turn-off function reduces the sink current of the gate drivers, avoiding a fast dI/dt transition on the power stage.

The drivers turn off the power MOSFET using the current $I_{GATE,off(SO)}$ listed in Table 14 and the $t_{cc,off(SO)}$ is increased by about 8 times the normal $t_{cc,off}$ to ensure a correct discharge of the MOSFETs' gates (refer to Table 15).

Table 14. Soft-off gate currents (according to the nominal gate current IGATE level)

IGATE level Refer to Table 11	$I_{GATE,off}$ [mA]	$I_{GATE,off(SO)}$ [mA]
0 (GND)	50	50
1	150	50
2	300	50
3	500	150
4	600	150
5	700	150
6	800	150
7	1000	300
8	1100	300
9	1200	300
10	1300	300
11	1400	300
12	1600	500
13	1700	500
14	1800	500
15 (VDD)	2000	500

Table 15. **Soft-off constant-current time (according to the nominal TCC level)**

TCC level Refer to Table 11	$t_{cc,off}$ [ns]	$t_{cc,off(SO)}$ [µs]
0 (GND)	1120	9.0
1	140	1.1
2	280	2.2
3	420	3.4
4	560	4.5
5	700	5.6
6	840	6.7
7	980	7.8
8	1120	9.0
9	1260	10.1
10	1400	11.2
11	1540	12.3
12	1680	13.4
13	1900	15.2
14	2200	17.6
15 (VDD)	2400	19.2

5.5 Thermal shutdown

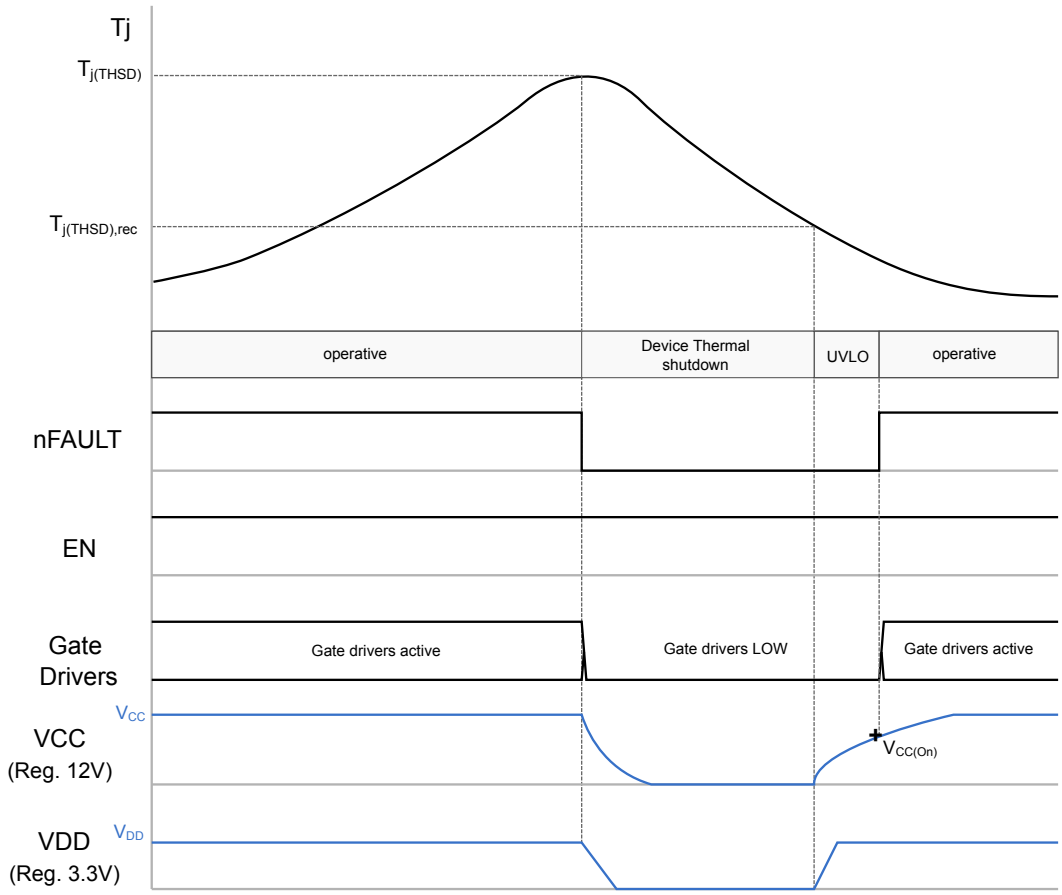
The STDRIVE102BH/H has a thermal shutdown protection: if the junction temperature of the device exceeds the thermal shutdown threshold $T_{j(THSD)}$, the driver turns off the external power MOSFETs and after a $t_{cc,off}$ the linear regulators and the charge pump are disabled. The nFAULT pin is forced low (refer to Figure 25).

Note that the blocks generating the supply of the drivers (V_{CC} and V_{BOOT}) are turned off: therefore, the supplies slowly decrease according to the external capacitor present on the VCC and VBOOT pins. When the capacitors are fully discharged, the external MOSFETs are kept off only by the 100 kΩ resistors present on each driver's output.

Turning off the 12 V regulator results in the turn off of the UVLO and power good circuitry. As a consequence, the nFAULT is forced low together with the FLAG pin (for the STDRIVE102BH only), regardless the actual voltage on VCC pin.

As soon as the temperature of the device decreases below the $T_{j(THSD),rec}$ temperature, all the functional blocks are enabled again. According to the duration of the thermal transient, the regulators and their different supplies (V_{BOOT}, V_{CC} and V_{DD}) can decrease below the UVLO threshold. In this case the drivers are enabled and the nFAULT pin is released as soon as all the UVLO condition is released. In the STDRIVE102BH, the FLAG pin is released according to the power-good circuitry (refer to Table 16 in the next section).

Figure 25. STDRIVE102BH/H thermal thresholds



5.6 Protections management summary

A summary of the protections and the effects on the functional blocks of the device can be found in Table 16. The protections embedded in the STDRIVE102BH/H ensure a safe operation for the gate drivers and the external power stage. The protections include:

- Undervoltage lock-out (UVLO) for:
  - 12 V LDO regulator: V_{CC} supply (Section 5.1.1)
  - 3.3 V LDO regulator: V_{DD} supply (Section 5.1.2)
  - Charge pump: V_{BOOT} - V_M supply (Section 5.1.3)
- V_{DS} monitor protection (Section 5.2.3)
- AFE comparators protection (Section 5.3)
- Thermal shutdown protection (Section 5.5)

When a protection is triggered, the nFAULT pin is kept low as long as the FAULT condition is released. Depending on the fault condition one or more functional blocks are disabled.

In addition to the protections listed above, the STDRIVE102BH reports a warning event on the FLAG pin, in case the V_{CC} supply of the drivers falls below the power-good threshold $V_{P\_GOOD(Off)}$. The FLAG pin provides the indication that the V_{CC} is low and the drivers are operating with a reduced voltage. The FLAG pin is intended to be an early warning before the actual protection that is the UVLO on the VCC pin. When V_{CC} falls below the $V_{P\_GOOD(Off)}$ threshold, the open-drain FLAG pin is set low and it is released when the V_{CC} rises above the $V_{P\_GOOD(On)}$ threshold (refer to Figure 7). The power-good warning does not impact on the drivers operation, which continue working according to their driving input signals.

During the thermal shutdown, as the power-good monitoring turns off together with the VCC linear regulator, the FLAG open-drain pin is forced low. Even if the VCC pin is forced by an external voltage higher than the $V_{P\_GOOD(On)}$ threshold, the FLAG pin is forced low, because the circuitry controlling the power-good signal is disabled. After the thermal shutdown, the regulator is enabled again and the FLAG pin is released as soon as the V_{CC} increases above the $V_{P\_GOOD(On)}$ threshold.

Table 16. Device protections summary

Protection	Condition	Driver HS	Driver LS	12 V LDO	3.3 V LDO	Charge pump	Release condition	Notes
UVLO V_{CC}	$V_{CC} < V_{CC(Off)}$	LOW	LOW	Active	Active	Active	$V_{CC} > V_{CC(On)}$	
UVLO V_{DD}	$V_{DD} < V_{DD(Off)}$	LOW	LOW	Active	Active	Active	$V_{DD} > V_{DD(On)}$	The AFE could not work properly, drivers are disabled
Charge pump UVLO	$(V_{BOOT} - V_M) < V_{CPump(Off)}$	LOW	Active	Active	Active	Active	$(V_{BOOT} - V_M) > V_{CPump(On)}$	
Thermal shutdown	$T_j > T_{j(THSD)}$	LOW (1)	LOW (1)	Disable	Disable	Disable	$T_j < T_{j(THSD),rec}$	Both nFAULT and FLAG are forced low
V_{DS} monitor	$V_{DS} > V_{DS,th}$	LOW	LOW	Active	Active	Active	Standby or EN forced low (< $V_{release}$)	
AFE comparators	$V_{C\_INx} > V_{CREF}$	LOW	LOW	Active	Active	Active	Standby or EN forced low (< $V_{release}$)	
Warning on V_{CC} (2)	$V_{CC} < V_{P\_GOOD(Off)}$	Active	Active	Active	Active	Active	$V_{CC} > V_{P\_GOOD(On)}$	Warning only, it is reported on FLAG pin

1. *The drivers can force LOW the MOSFETs' gates only if V_{CC} and V_{BOOT} supplies are present. Thermal shutdown turns off both the 12 V regulator and the charge pump, so the gate drivers' ability to turn off the MOSFET could be affected.*
2. *Avaialble only for STDRIVE102BH.*

Referring to Table 16, the state of the functional blocks can assume three different conditions:

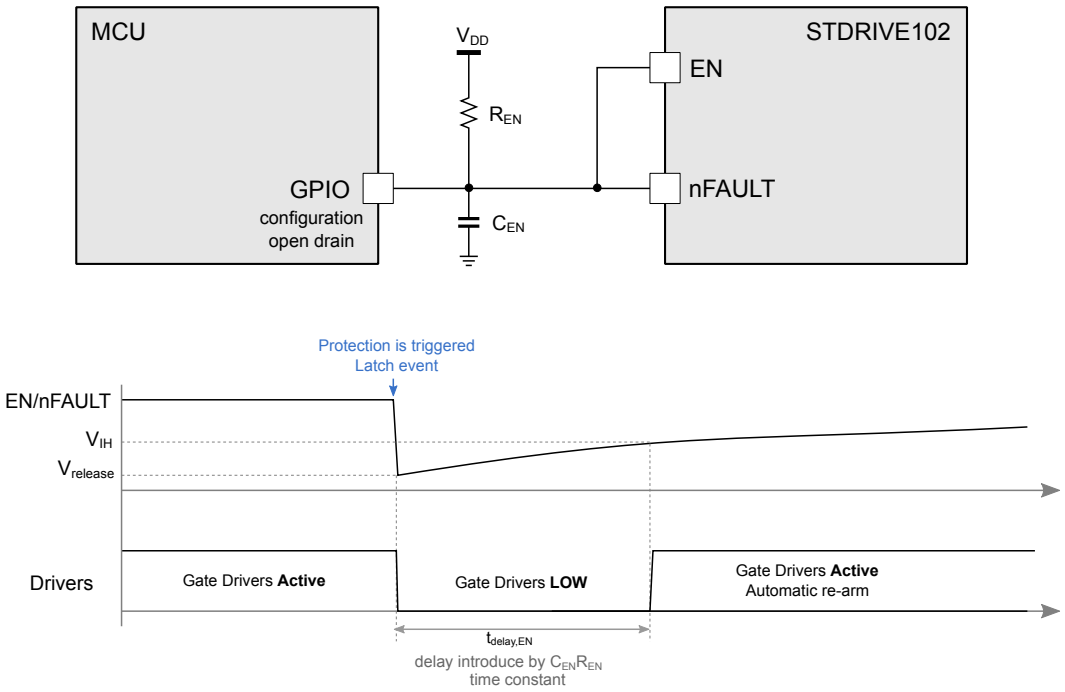
- **Active**: the block is fully operative.
- **LOW** (gate drivers only): despite the digital inputs, the drivers are set LOW and they sink current. Therefore, the external power MOSFET is turned off regardless of the digital input applied.
- **Disable**: the functional block is disabled.

5.6.1 Automatic re-arm using the nFAULT pin

The V_{DS} monitoring protection and the AFE comparators protection are latched: in case one of these protections is triggered, the device latches and it cannot operate until the FAULT condition is released.

The release condition can be forced by applying a low pulse on the EN pin. Otherwise, the latch can be released automatically, connecting together the EN and the nFAULT pins as shown in Figure 26.

Figure 26. Automatic re-arm using EN and nFAULT pins



When a protection is triggered, the nFAULT open-drain drives low the EN pin and its voltage falls below the $V_{release}$ threshold: the latch is then released. To avoid an immediate re-arm of the power stage, a delay can be introduced using a capacitor C_{EN} together with the pull-up resistor R_{EN}. The time required to reach the digital threshold V_{IH} increases, due to the smooth rising slope of the EN pin, thus delaying the re-arm of the drivers.

If a microcontroller is also connected to the EN pin, care must be taken to use an open-drain configuration for the GPIO to avoid any conflict.

It is important to consider that the EN pin has an internal pull-down resistor $R_{PD,EN}$ so the voltage of the EN pin at the end of the rising transient is:

Equation 5

$$V_{EN,high} = V_{DD} \cdot \frac{R_{PD,EN}}{R_{PD,EN} + R_{EN}} \quad (5)$$

The time constant of the rising transient is:

Equation 6

$$\tau_{EN} = \frac{R_{EN} \cdot R_{PD,EN}}{R_{EN} + R_{PD,EN}} \cdot C_{EN} \quad (6)$$

Using the values calculated in Eq. (5) and in Eq. (6), it is possible to find the delay time required to re-arm the power MOSFETs, after a FAULT condition:

Equation 7

$$t_{delay,EN} = \tau_{EN} \cdot ln\left(\frac{V_{EN,high} - V_{release}}{V_{EN,high} - V_{IH}}\right) \quad (7)$$

According to Eq. (5), the value of R_{EN} should be chosen to be several times smaller than $R_{PD,EN}$ to avoid an excessive drop of the high level on the EN pin ($V_{EN,high}$). In this hypothesis, it is possible to approximate Eq. (7) as:

Equation 8

$$t_{delay,EN} \cong R_{EN} \cdot C_{EN} \cdot ln\left(\frac{V_{DD} - V_{release}}{V_{DD} - V_{IH}}\right) \quad (8)$$

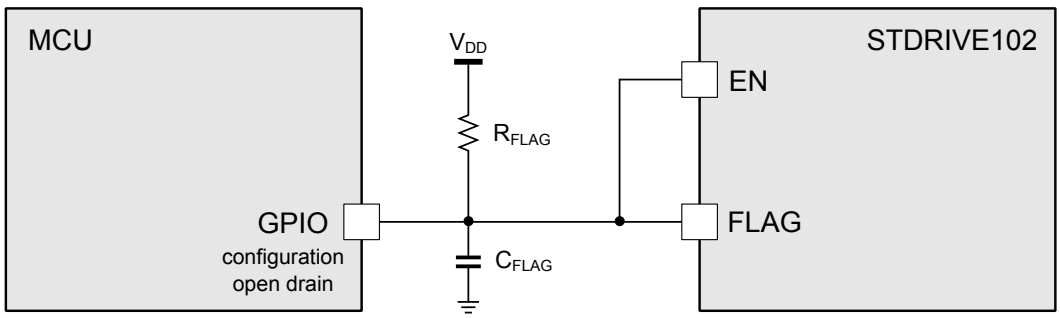
5.6.2 FLAG pin (STDRIVE102BH only)

Unlike the UVLO protection on the V_{CC}, the warning on the V_{CC} supply does not disable or limit the drivers and the device functionalities. The only effect is that the FLAG pin is forced low. The external microcontroller can detect this condition and manage it by modifying the control algorithm of the driver.

In case a hardwired solution is required to disable the drivers at a higher threshold than the V_{CC} UVLO threshold, connect together the EN and the FLAG pins.

A capacitor can be added as shown in Figure 27 to provide an extra delay for the enabling of the drivers: the delay is determined by the time constant $\tau_{FLAG} \cong R_{FLAG} \cdot C_{FLAG}$, explained in the previous Section 5.6.1.

Figure 27. FLAG and EN management



5.7 Device power-up

The power-up sequence starts at the rising edge of the main supply applied on the VS pin, supposing that the nSTBY pin is forced high. In case the VM and VS pins are supplied by different voltage sources, the VM voltage must be applied before the VS voltage. This sequence is not important if the nSTBY pin is kept low and it is raised after the supplies are stable.

The internal 5 V regulator begins to charge the capacitor on the LGC_CAP pin. When the POR threshold is met, the internal logic starts to operate and initialize all the internal circuits. During this phase the nFAULT signal is kept low.

Then, the regulators are enabled and they can charge their external bypass capacitors: most of the time required by the device to be operative is due to the charge of the external bypass capacitor. Depending on the capacitor value and the current capability of the LDO regulators and the charge pump, this time can last hundreds of microseconds.

The typical sequence for the supplies is:

- VDD UVLO is released (V_{DD} > $V_{DD(On)}$): the analog voltage on TCC/IGATE is now valid and the AFE is operative. The internal ADC can acquire the TCC/IGATE configuration, taking approximately 100 µs.
- VCC UVLO is released (V_{CC} > $V_{CC(On)}$): the low-side drivers are operative.
- Charge pump UVLO is released (V_{BOOT} - V_M > $V_{CPump(On)}$): the high-side drivers are operative.

Following the release of all the UVLO protections, the nFAULT pin is set high by the external pull-up resistor.

5.8 Standby and wake-up

The standby pin is active low (nSTBY = 0: standby mode, nSTBY = 1: normal mode). The standby mode strongly reduces the current consumption down to $I_{STBY.}$ The commutation to standby mode, which takes a t_{STBY} to be completed, follows a sequence of steps managed by the internal logic:

1. Before being disabled, all the drivers turn off the external MOSFETs. Then, the V_{GS} of the external MOSFET is kept low by the internal 100 kΩ pull-down resistor, present on the GHSx/GLSx pins.
2. The AFE is disabled.
3. Both the linear regulators and the charge pump are switched off to reduce current consumption.
4. Open-drain pins are released.
5. The internal logic enters the standby state, and most of its circuitries are disabled.

It is always preferable to force nSTBY = 0 before removing the main supply VS in the turn-off sequence of the device.

When the nSTBY pin returns high, the device leaves the standby mode following the wake-up sequence:

1. Internal logic is initialized.
2. The linear regulators and the charge pump are turned on.
3. The AFE becomes active.

The device can be considered operative as soon as its supplies (V_{CC}, V_{DD}, and V_{BOOT}) are stable above the respective UVLO thresholds (nFAULT open-drain released).

6 Application examples

6.1 3-phase brushless motor application with triple shunt current sensing based on STDRIVE102BH

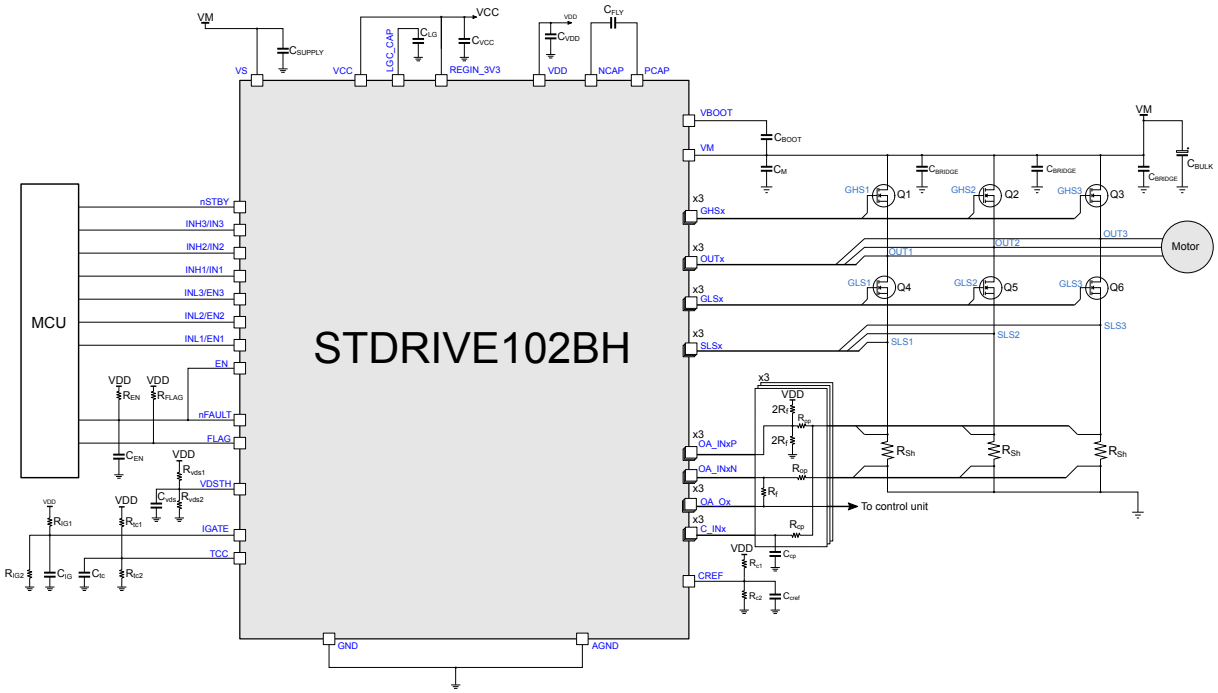
Figure 28 shows an application example using the STDRIVE102BH to drive a 3-phase motor with triple shunt configuration. The list of components is summarized in Table 17.

The values reported in Table 17 refer to a generic example. The actual components' values must be chosen in order to fit the specific application requirements. The value of the resistors on the IGATE, TCC, and VDSTH pins must be sized according to the specific power stage. The values of the components connected to the operational amplifiers and the shunt resistors must be sized according to the current rating of the application.

Table 17. List of components

	Value
C_{BRIDGE}	220 nF (to be tuned according to current rating of the power stage)
C_{BULK}	470 µF (to be tuned according to current rating of the power stage)
C_M	1 µF low ESR to be placed close to the driver
R_{sh}	According to the current rating of the application (for example 2 mΩ)
R_{op}, R_f	According to op amp gain (for example 1 kΩ, 15 kΩ: Gain = 15)
R_{cp}	4.7 kΩ
R_{c1}, R_{c2}	According to the CREF threshold (for example 100 kΩ, 7.5 kΩ: V_{CREF} = 230 mV)
C_{cp}	10 nF / 16 V
R_{IG1} , R_{IG2}	1% precision, values according to drivers' current selection (for example R_{IG1} = 30 kΩ, R_{IG2} = 15 kΩ; see Figure 16)
C_{IG}	10 nF /16 V
R_{tc1}, R_{tc2}	1% precision, values according to t_{cc} timing selection (for example R_{tc1} = 30 kΩ, R_{tc2} = 7.5 kΩ ; see Figure 16)
C_{tc}	10 nF / 16 V
R_{vds1} , R_{vds2}	1% precision, values according to V_{DS} monitoring threshold (for example R_{vds1} = 220 kΩ, R_{vds2} = 15 kΩ: V_{DSTH} = 210 mV)
C_{vds}	10 nF / 16 V
R_{EN} , C_{EN}	According to target disable time (for example 33 kΩ, 47 nF: $t_{delay,EN}$ ≈ 1.25 ms)
R_{FLAG}	33 kΩ
C_{SUPPLY}	1 µF low ESR to be placed close to the driver
C_{LG}	4.7 µF / 16 V
C_{VCC}	4.7 µF / 25 V
C_{VDD}	4.7 µF / 16 V
C_{BOOT}	1 µF / 25 V
C_{FLY}	220 nF (according to V_M rating)

Figure 28. **STDRIVE102BH typical application example**



6.2 3-phase brushless motor application with single shunt current sensing based on STDRIVE102H

Figure 29 shows an application example using STDRIVE102H to drive a 3-phase motor with single shunt configuration. The list of components is summarized in Table 18.

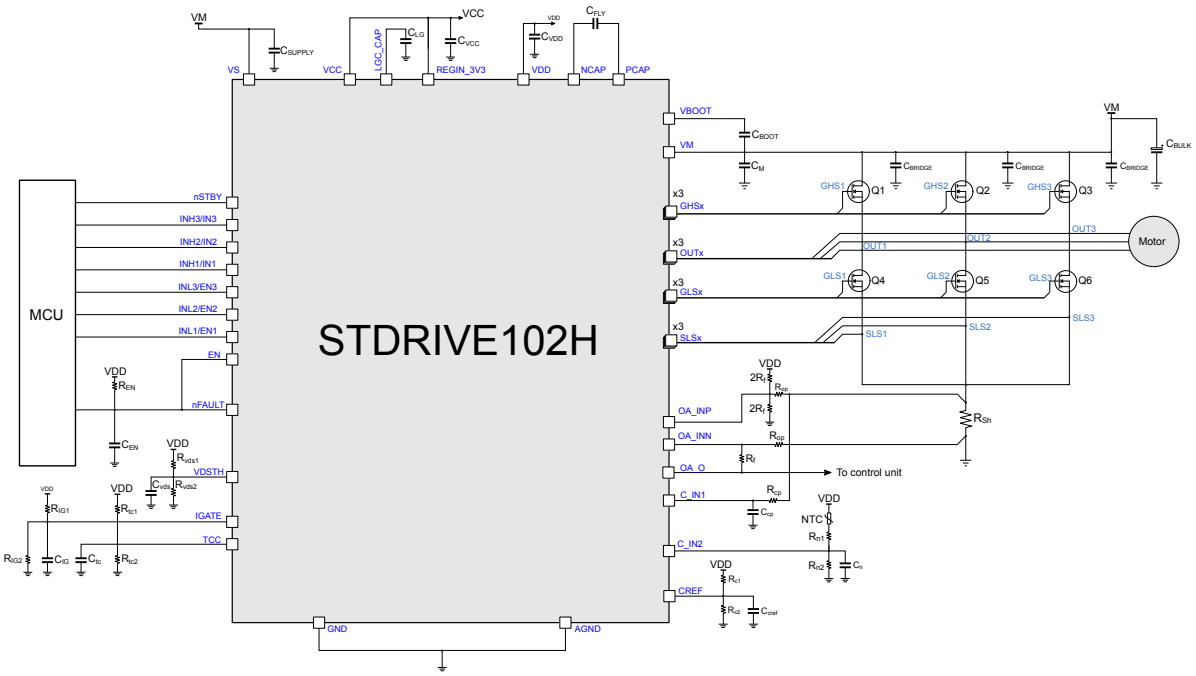
Values reported in Table 18 refer to a generic example. The actual components' values must be chosen in order to fit the specific application requirements. The value of the resistors on the IGATE, TCC and VDSTH pins must be sized according to the specific power stage. The values of the components connected to the operational amplifier and the shunt resistor must be sized according to the current rating of the application.

Table 18. **STDRIVE102H list of components**

	Value
C_{BRIDGE}	220 nF (to be tuned according to current rating of the power stage)
C_{BULK}	470 µF (to be tuned according to current rating of the power stage)
C_M	1 µF low ESR to be placed close to the driver
R_{sh}	According to the current rating of the application (for example 2 mΩ)
R_{op}, R_f	According to op amp gain (for example 1 kΩ, 15 kΩ: Gain = 15)
R_{cp}	4.7 kΩ
R_{c1}, R_{c2}	According to the CREF threshold (for example 100 kΩ, 7.5 kΩ: V_{CREF} = 230 mV)
C_{cp}	10 nF / 16 V
NTC	10 kΩ at 25 °C
R_{n1}, R_{n2}	According to temperature threshold (for example R_{n1} = 910 Ω, R_{n2} = 120 Ω)
C_n	220 nF
R_{IG1} , R_{IG2}	1% precision, values according to drivers' current selection (for example R_{IG1} = 30 kΩ, R_{IG2} = 15 kΩ; see Figure 16)
C_{IG}	10 nF /16 V

	Value
R_{tc1}, R_{tc2}	1% precision, values according to t_{cc} timing selection (for example R_{tc1} = 30 kΩ, R_{tc2} = 7.5 kΩ ; see Figure 16)
C_{tc}	10 nF / 16 V
R_{vds1} , R_{vds2}	1% precision, values according to V_{DS} monitoring threshold (for example R_{vds1} = 220 kΩ, R_{vds2} = 15 kΩ: V_{DSTH} = 210 mV)
C_{vds}	10 nF / 16 V
R_{EN} , C_{EN}	According to target disable time (for example 33 kΩ, 47 nF: $t_{delay,EN}$ ≈ 1.25 ms)
C_{SUPPLY}	1 µF low ESR to be placed close to the driver
C_{LG}	4.7 µF / 16 V
C_{VCC}	4.7 µF / 25 V
C_{VDD}	4.7 µF / 16 V
C_{BOOT}	1 µF / 25 V
C_{FLY}	220 nF (according to V_M rating)

Figure 29. STDRIVE102H typical application example



7 Layout recommendations and guidelines

7.1 Power stage layout

It is very important to minimize the overall parasitic inductance of the paths connecting the power MOSFETs and the gate drivers. Higher inductance can introduce ringing on the gate signals and increase induced turn-on effects. In order to minimize inductance:

- The traces between the STDRIVE102BH/H and the MOSFETs must be as short and straight as possible.
- The traces should avoid multiple transitions between PCB layers.
- When moving away from the STDRIVE102BH/H pads, increase the trace width (at least 0.5 mm).
- Each couple of traces GHSx/OUTx and GLSx/SLSx must follow the same path and should be routed one close to the other to minimize their loop area.
- Place a ground plane with no discontinuities underneath the power stage, to provide the shortest return path for the gate currents (see Section 7.2).

A wide copper area must connect the drains of the three high-side MOSFETs, the motor's supply V_M and the bulk capacitors. The area can be replicated in the inner layers of the PCB; all of them can be connected using multiple vias. This approach decreases the overall impedance and improves the thermal dissipation of the high-side section of the power stage. Extend the V_M copper area underneath the gate driver traces, then connect it to the VM pin of the STDRIVE102BH/H; this ensures a return path for the currents provided by the charge pump. Moreover, the VM pin is also used to sense the high-side drains for the V_{DS} monitoring protection: wider copper areas help to reduce the voltage drop along this path. A low ESR ceramic capacitor must be placed close to the VM pin (see Section 7.3).

The high-side source and the low-side drain in each half-bridge should be connected with a dedicated copper area, which then connects to each motor's phase. Similarly, the low-side source and the shunt resistor in each half-bridge should be connected with a dedicated copper area. Each copper area can be replicated on different layers; all of them must be connected with an adequate number of vias. Vias concentration should be higher close to the pads of the power components (MOSFETs and shunt resistors). This allows to have a low impedance path for the load currents and helps to dissipate the heat.

Do not use the same trace to connect different branches, even if they share the same net: for example, SLSx coming from the STDRIVE102BH/H needs a dedicated trace, which directly connects the source of the low-side MOSFET. Then a wide copper area must connect the source of the low-side MOSFET and the shunt resistor. Eventually, another dedicated pair of differential traces is routed from the two pads of the shunt resistor to the readout circuitry.

Other signals not directly related to the power stage should be routed in a different area of the PCB, to avoid any noise coupling due to high dV/dt and dI/dt transients.

7.2 Grounding

One inner layer of the PCB should be dedicated only for grounding. The layer should be divided in two planes: one for the power part and another for the low-voltage signal part. The two planes are tied together in correspondence with the STDRIVE102BH/H, which should be placed in the middle of the two. Power ground plane must be connected to the exposed pad (GND) of the STDRIVE102BH/H, while the signal ground plane should be connected to the AGND pin. The junction between AGND and the exposed pad (GND) must be done as close as possible to the STDRIVE102BH/H in order to minimize grounds misalignment. Exposed pad must have an adequate number of vias to transfer heat to the other layers, down to the bottom layer of the PCB, in order to dissipate heat.

Therefore, the PCB can be divided in two main areas, delimited by each plane: the power area and the signal area. Routing of the components related to the operational amplifiers and in general to the circuitries related to VDD, including the resistors' divider for TCC and IGATE pins, must be placed in the signal ground area. On the other hand, the power ground area should be dedicated only to the power stage, the gate drivers' traces, the copper plane of the V_M supply, the bulk capacitor and all the ceramic capacitors connected to each half-bridge.

7.3 Power supply decoupling capacitors

The STDRIVE102BH/H has different supply pins and every pin requires a decoupling capacitor, to be placed as near as possible to the pin. All the capacitors should have a low ESR.

A capacitor between the VS pin and the GND (exposed pad) is required for the main supply of the device and to provide a part of the charge pump switching current.

A capacitor between VCC and the GND (exposed pad) is required for the supply for the low-side drivers. Its value should be at least 4.7 µF / 25 V to ensure the stability of the V_{CC} when a pulsed current is required by the low-side drivers. Note that, according to the total gate charge of the low-side MOSFET and their switching frequency, the value of this capacitor should be increased. Moreover, an optional 100 nF or smaller capacitor can be added in parallel to filter high frequency noise.

A capacitor between the LGC_CAP pin and the GND (exposed pad) is required to filter all the internal rails of the device and avoid any malfunctioning on the internal logic even in case of strong variation on V_S supply. Use a 4.7 µF / 16 V capacitor. An optional 100 nF or small capacitor can be added in parallel to filter high frequency noise.

A 4.7 µF / 16 V capacitor between VDD and AGND pins is required to ensure stability of the AFE supply.

The two capacitors of the charge pump, C_{FLY} between the NCAP and PCAP and C_{BOOT} between VBOOT and VM, must be placed on the same layer of the STDRIVE102BH/H. They must be connected directly to the pins avoiding any via. The rated voltage of C_{FLY} must be compliant with the V_M voltage, while C_{BOOT} can be rated 25 V. The values of both capacitors depend on the high-side driver average current, which eventually depends on the total gate charge and the switching frequency of the high-side MOSFETs.

The power stage and the motor supply need one or more electrolytic bulk capacitors: their value depends on some parameters mainly related to the current required by the motor and the ripple allowed on the VM supply. In addition, a smaller ceramic capacitor must be added for each half-bridge, to provide the pulsed currents required by the power stage and the gate drivers. Another capacitor must be placed close to the VM pin to filter the switching noise introduced by the charge pump, as reported in Section 7.3. This capacitor should have the same value C_{BOOT} and a voltage rating according to the value of V_M. All these capacitors are in parallel and should be referred to the GND power plane described in Section 7.2.

8 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 VFQFPN 48L 6x6x1 mm, pitch 0.4 mm package information

Figure 30. VFQFPN 48L 6x6x1 mm, pitch 0.4 mm package outline

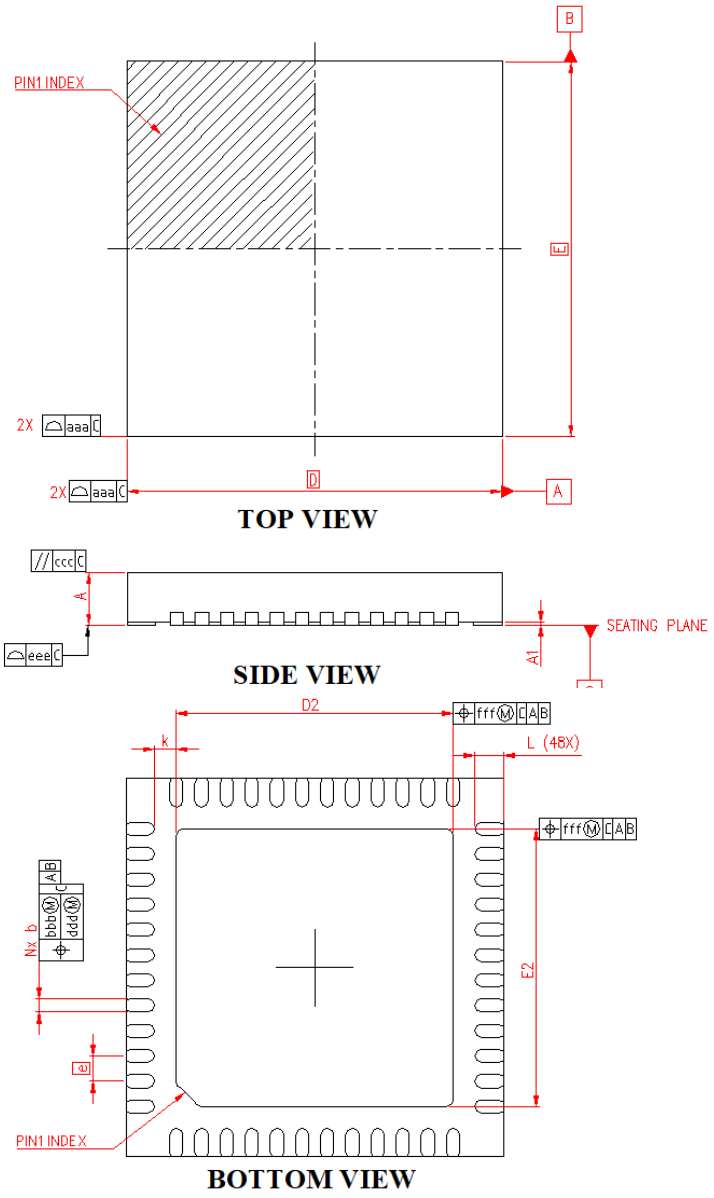
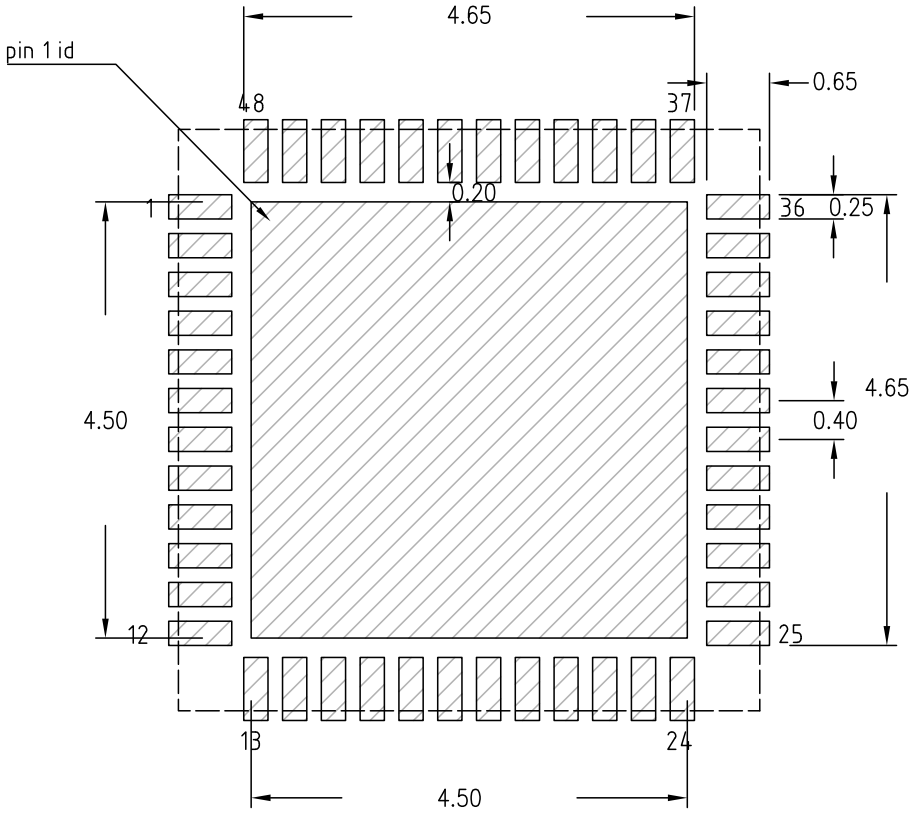


Table 19. **VFQFPN 48L 6x6x1 mm, pitch 0.4 mm package mechanical data**

Symbol	Dimensions [mm]		
	Min.	Typ.	Max.
A	0.80	0.85	1.00
A1	0.00	-	0.05
b	0.17	0.21	0.25
D		6.0 BSC	
D2	4.3	4.4	4.5
e		0.4 BSC	
E		6.0 BSC	
E2	4.3	4.4	4.5
L	0.35	0.45	0.55
K	0.24		
N		48	
Tolerance			
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

8.1.1 Suggested footprint

Figure 31. **VFQFPN 48L 6x6x1 mm, pitch 0.4 mm suggested footprint**



8.2 VFQFPN 40L 5x5x1 mm, pitch 0.4 package information

Figure 32. **VFQFPN 40L 5x5x1 mm, pitch 0.4 package outline**

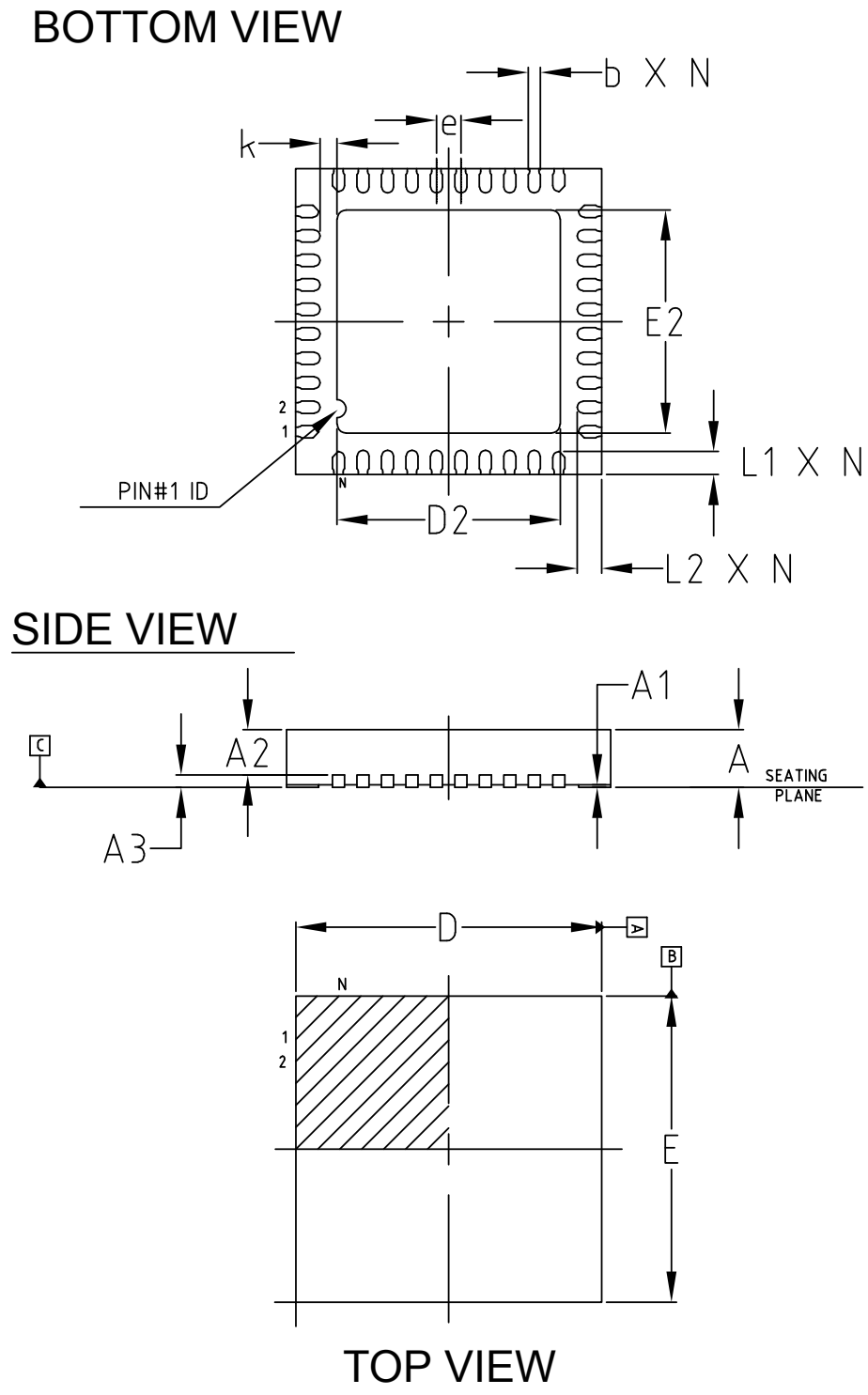
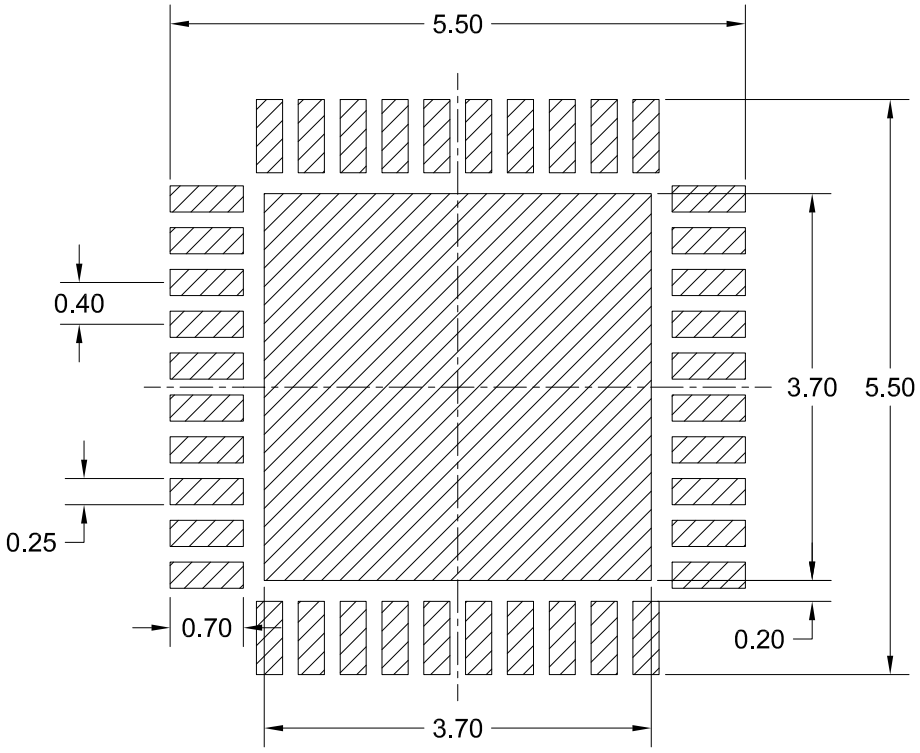


Table 20. **VFQFPN 40L 5x5x1 mm, pitch 0.4 package mechanical data**

Symbol	Dimensions [mm]		
	Min.	Typ.	Max.
A	0.80	0.85	1.00
A1	0.00	-	0.05
A2	0.55	0.65	0.75
A3		0.20 REF	
b	0.15	0.20	0.25
D		5.00 BSC	
D2	3.55	3.65	3.75
e		0.40 BSC	
E		5.00 BSC	
E2	3.55	3.65	3.75
L1	0.277	0.377	0.477
L2	0.30	0.40	0.50
k	0.2	-	-
N		40	
Tolerance			
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.05	
eee		0.10	

8.2.1 Suggested footprint

Figure 33. **VFQFPN 40L 5x5x1 mm, pitch 0.4 mm suggested footprint**



9 Ordering information

Table 21. **Order code**

Order code	Package	Package marking	Packing
STDRIVE102BH	VFQFPN 48L 6x6x1 mm, pitch 0.4 mm	DRV102BH	Tray
STDRIVE102BHTR	VFQFPN 48L 6x6x1 mm, pitch 0.4 mm	DRV102BH	Tape and reel
STDRIVE102H	VFQFPN 40L 5x6x1 mm, pitch 0.4 mm	DRV102H	Tray
STDRIVE102HTR	VFQFPN 40L 5x6x1 mm, pitch 0.4 mm	DRV102H	Tape and reel

Revision history

Table 22. **Document revision history**

Date	Version	Changes
24-Mar-2025	1	Initial release.

Contents

List of tables

List of figures