FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C90 • MM74C93
4-Bit Decade Counter • 4-Bit Binary Counter

General Description

The MM74C90 decade counter and the MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The 4-bit decade counter can reset to zero or preset to nine by applying appropriate logic level on the R_{01}, R_{02}, R_{91} and R_{92} inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02}, and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

All inputs are protected against static discharge damage.

Features

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power compatibility:
  Fan out of 2 TTL driving 74L
- The MM74C93 follows the MM74L93 Pinout

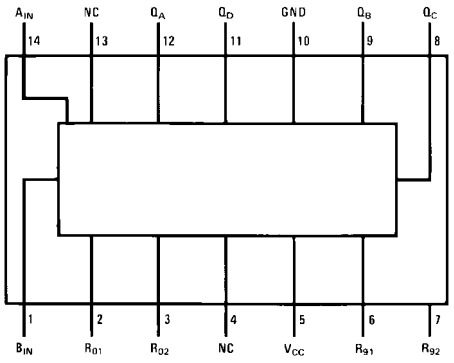
Ordering Code:

Order Number	Package Number	Package Description
MM74C90N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C93N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagrams

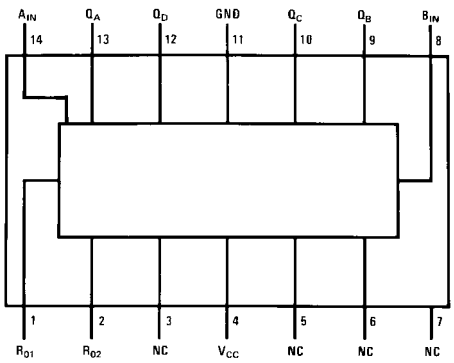
Pin Assignments for DIP

MM74C90



Top View

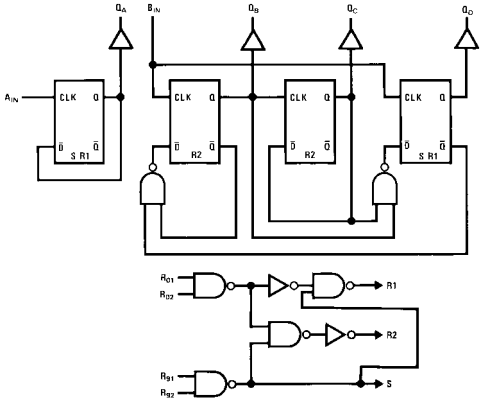
MM74C93



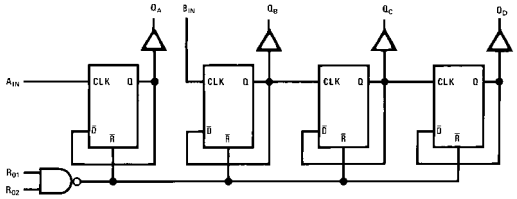
Top View

Logic Diagrams

MM74C90



MM74C93



Truth Tables

MM74C90 4-Bit Decade Counter BCD Count Sequence

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Output Q_A is connected to Input B for BCD count.
H = HIGH Level
L = LOW Level
X = Irrelevant

MM74C93 4-Bit Binary Counter Binary Count Sequence

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B for binary count sequence.
H = HIGH Level
L = LOW Level
X = Irrelevant

Function Tables

Reset/Count Function Table

Reset Inputs				Output			
R_{01}	R_{02}	R_{91}	R_{92}	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

Reset/Count Function Table

Reset Inputs		Output			
R_{01}	R_{02}	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature Range (T_A)	
MM74C90, MM74C93	−40°C to +85°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = +10 μA			0.5	V
		V_{CC} = 10V, I_O = +10 μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM74C90, MM74C93	V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM74C90, MM74C93	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage					
	MM74C90, MM74C93	V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM74C90, MM74C93	V_{CC} = 4.75V, I_O = −360 μA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, V_{OUT} = 0V	−1.75	−3.3		mA
	(P-Channel)	T_A = 25°C				
I_{SOURCE}	Output Source Current	V_{CC} = 10V, V_{OUT} = 0V	−8.0	−15		mA
	(P-Channel)	T_A = 25°C				
I_{SINK}	Output Sink Current	V_{CC} = 5V, V_{OUT} = V_{CC}	1.75	3.6		mA
	(N-Channel)	T_A = 25°C				
I_{SINK}	Output Sink Current	V_{CC} = 10V, V_{OUT} = V_{CC}	8.0	16		mA
	(N-Channel)	T_A = 25°C				

AC Electrical Characteristics (Note 2)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time	$V_{CC} = 5V$		200	400	ns
	from A_{IN} to Q_A	$V_{CC} = 10$		80	150	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from	$V_{CC} = 5V$		450	850	ns
	A_{IN} to Q_B (MM74C93)	$V_{CC} = 10V$		160	300	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from	$V_{CC} = 5V$		450	800	ns
	A_{IN} to Q_B (MM74C90)	$V_{CC} = 10V$		160	300	ns
t_{pd0}, t_{pd1}	Propagation Delay Time	$V_{CC} = 5V$		500	1050	ns
	from A_{IN} to Q_C (MM74C93)	$V_{CC} = 10$		200	400	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from	$V_{CC} = 5V$		500	1000	ns
	A_{IN} to Q_C (MM74C93)	$V_{CC} = 10V$		200	400	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from	$V_{CC} = 5V$		600	1200	ns
	A_{IN} to Q_D (MM74C93)	$V_{CC} = 10V$		250	500	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from	$V_{CC} = 5V$		450	800	ns
	A_{IN} to Q_D (MM74C90)	$V_{CC} = 10V$		160	300	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from	$V_{CC} = 5V$		150	300	ns
	R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D	$V_{CC} = 10V$		75	150	ns
	(MM74C93)					
t_{pd0}, t_{pd1}	Propagation Delay Time from	$V_{CC} = 5V$		200	400	ns
	R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D	$V_{CC} = 10V$		75	150	ns
	(MM74C90)					
t_{pd0}, t_{pd1}	Propagation Delay Time from	$V_{CC} = 5V$		250	500	ns
	R_{91} or R_{92} to Q_A or Q_D	$V_{CC} = 10V$		100	200	ns
	(MM74C90)					
t_{PW}	Min. R_{01} or R_{02} Pulse Width	$V_{CC} = 5V$	600	250		ns
	(MM74C93)	$V_{CC} = 10V$	30	125		ns
t_{PW}	Min. R_{01} or R_{02} Pulse Width	$V_{CC} = 5V$	600	250		ns
	(MM74C90)	$V_{CC} = 10V$	300	125		ns
t_{PW}	Min. R_{91} or R_{92} Pulse Width	$V_{CC} = 5V$	500	200		ns
	(MM74C90)	$V_{CC} = 10V$	250	100		ns
t_r, t_f	Maximum Clock Rise	$V_{CC} = 10V$			15	µs
	and Fall Time	$V_{CC} = 10V$			5	µs
t_W	Minimum Clock Pulse Width	$V_{CC} = 5V$	250	100		ns
		$V_{CC} = 10V$	100	50		ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$	2			MHz
		$V_{CC} = 10V$	5			MHz
C_{IN}	Input Capacitance	Any Input (Note 3)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		45		pF

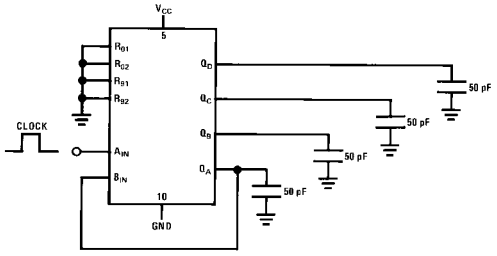
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see Family Characteristics application note—AN-90.

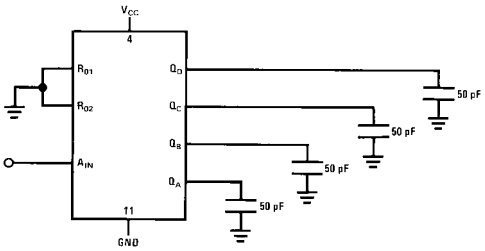
AC Test Circuits

MM74C90



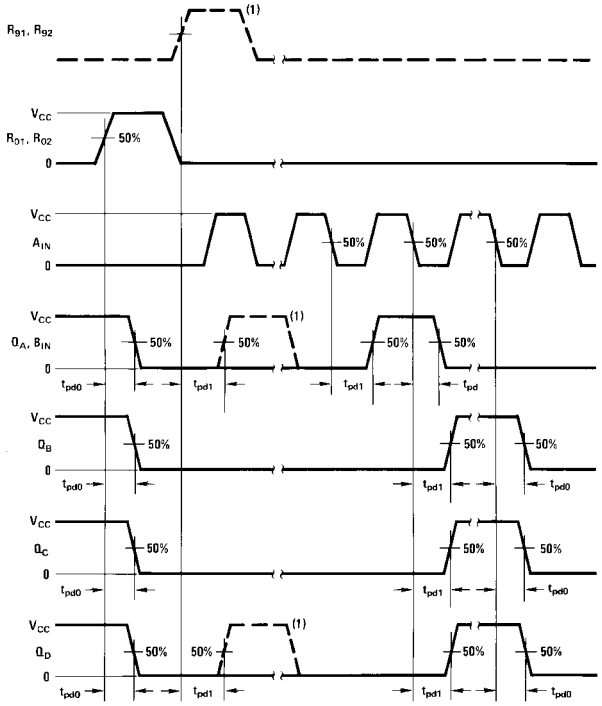
Clock rise and fall time $t_r = t_f = 20$ ns

MM74C93



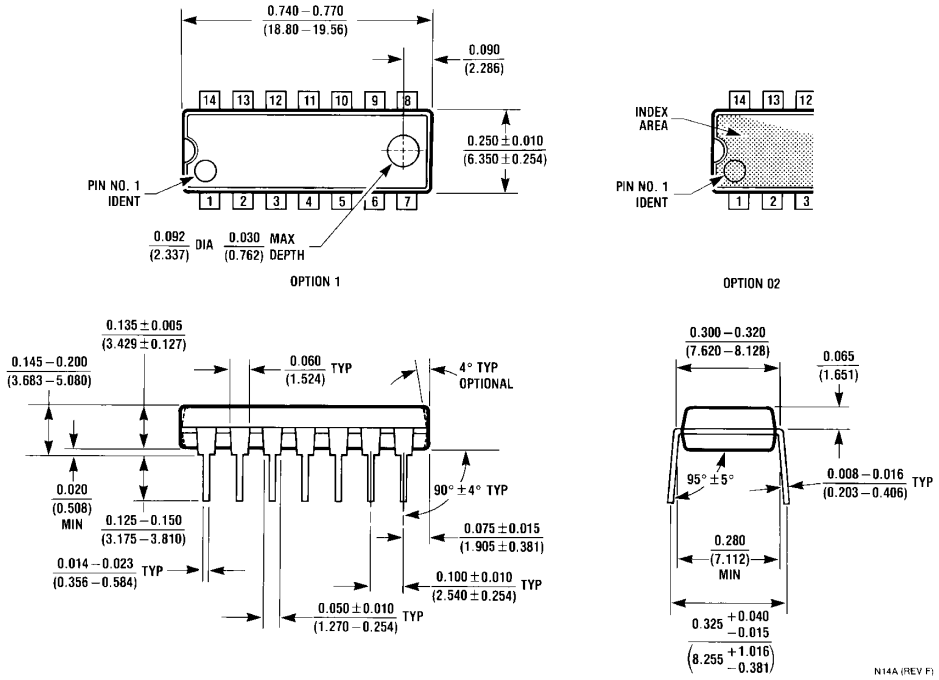
Clock rise and fall time $t_r = t_f = 20$ ns

Switching Time Waveforms



MM74C90 and MM74C93 are solid line waveforms. Dashed line waveforms are for MM74C90 only.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A